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S1D13771 TV Out Graphics Engine

S5U13771P00C100 Evaluation Board User Manual

Document Number: X82A-G-003-01

Status: Revision 1.0

Issue Date: 2007/07/04

Evaluation Board/Kit and Development Tool Important Notice

1. This evaluation board/kit or development tool is designed for use for engineering evaluation, demonstration, or development purposes only. Do not use it for other purposes. It is not intended to meet the requirements of design for finished products.
2. This evaluation board/kit or development tool is intended for use by an electronics engineer and is not a consumer product. The user should use it properly and in a safe manner. Seiko Epson does not assume any responsibility or liability of any kind of damage and/or fire caused by the use of it. The user should cease to use it when any abnormal issue occurs even during proper and safe use.
3. The part used for this evaluation board/kit or development tool may be changed without any notice.

NOTICE

Table of Contents

1 Introduction

This manual describes the setup and operation of the S5U13771P00C100 Evaluation Board. The evaluation board is designed as an evaluation platform for the S1D13771 TV-Out Graphics Engine.

The S5U13771P00C100 evaluation board can be used with many native platforms via the host connectors which provide the appropriate signals to support a variety of CPUs. The S5U13771P00C100 evaluation board can also connect to the S5U13U00P00C100 USB Adapter board so that it can be used with a laptop or desktop computer, via USB 2.0.

This user manual is updated as appropriate. Please check the Epson Research and Development Website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Features

The S5U13771P00C100 Evaluation Board includes the following features:

- 64-pin W-CSP S1D13771 TV-Out Graphics Engine
- Header with all S1D13771 Host Bus Interface signals
- Headers for connection to the S5U13U00P00C100 USB Adapter board
- Composite video out connector
- Header for S1D13771 GPIO pins (optional)
- On-board 27MHz oscillator
- 14-pin DIP socket (if a clock other than 27MHz must be used)
- 3.3V input power
- On-board voltage regulators

3 Installation and Configuration

The S5U13771P00C100 evaluation board incorporates jumpers and 0 ohm resistors which allow it to be used with a variety of different configurations.

3.1 Configuration Jumpers

The S5U13771P00C100 has 5 jumpers which allow current measurement and selection of the IOVDD source. The jumper positions for each function are shown below.

Table 3-1: Configuration Jumper Summary

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	COREVDD	Normal	—	COREVDD current measurement
JP2	PLLVDD	Normal	—	PLLVDD current measurement
JP3	DACVCC	Normal	—	DACVCC current measurement
JP4	IOVDD	Normal	—	IOVDD current measurement
JP5	IOVDD Source	H1 connector, pin 9	3.3VDD	—

= Required setting when using the S5U13U00P00C100 USB Adapter board

JP1-JP4 - Power Supplies for the S1D13771

JP1-JP4 can be used to measure current consumption of each S1D13771 power supply.
When the jumper is at position 1-2, normal operation is selected.
When no jumper is installed, the current consumption for each power supply can be measured by connecting an ammeter to pin 1 and 2 of the jumper.

The jumper associated with each power supply is as follows:

JP1 for COREVDD
JP2 for PLLVDD
JP3 for DACVCC
JP4 for IOVDD

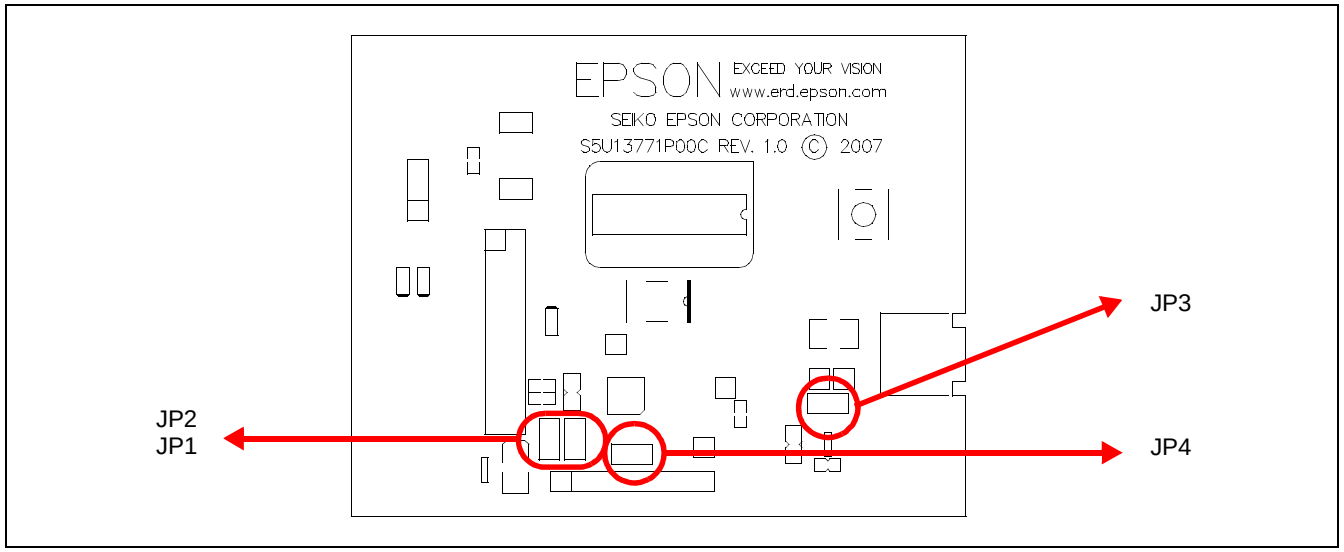

Figure 3-1: Configuration Jumper Locations (JP1-JP4)

JP5 - IOVDD Source

JP5 is used to select the source for the IOVDD supply voltage.
When the jumper is at position 1-2, the IOVDD voltage source is pin 9 of the H1 connector.
When the jumper is at position 2-3, the IOVDD voltage source is the 3.3V input power supply.

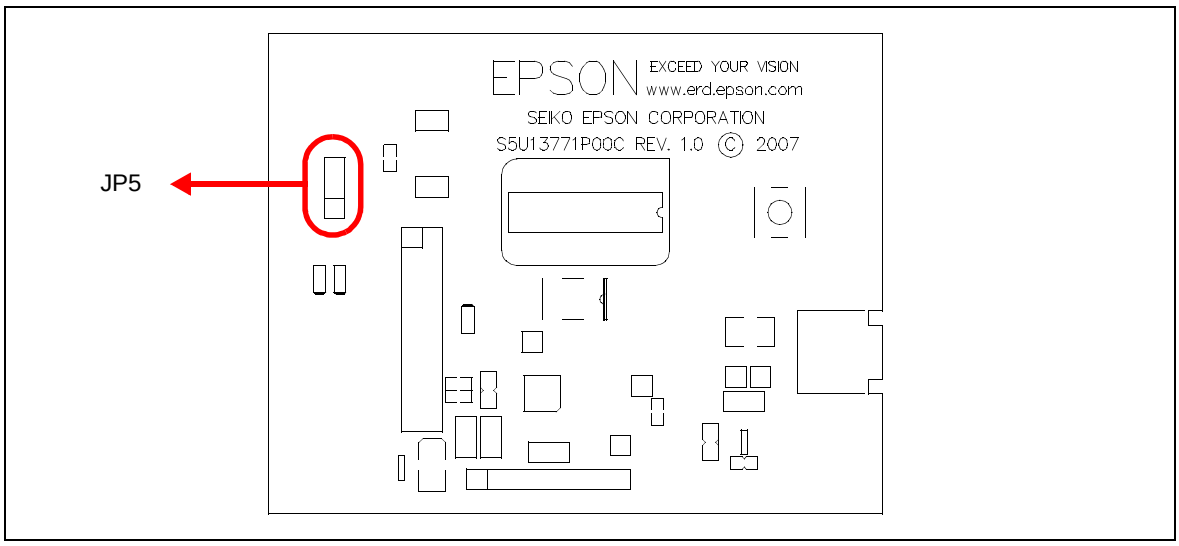

Figure 3-2: Configuration Jumper Location (JP5)

4 Technical Description

4.1 Power

4.1.1 Power Requirements

The S5U13771P00C100 evaluation board requires an external regulated power supply (3.3V / 0.5A). The power is supplied to the evaluation board through pin 1 of the H1 header, or pin 5 of the P2 header.

The green LED '3.3V Power' is turned on when 3.3V power is applied to the board.

4.1.2 Voltage Regulators

The S5U13771P00C100 evaluation board has on-board linear regulators to provide the 1.5V power and 3.0V power required by the S1D13771 TV-Out Graphics Engine.

4.1.3 S1D13771 Power

The S1D13771 TV-Out Graphics Engine requires 1.5V, 3.0V, and 1.65~3.6V power supplies.

1.5V power for COREVDD and PLLVDD is provided by an on-board linear voltage regulator.

3.0V power for DACVCC is provided by the on-board linear voltage regulator.

IOVDD can be in the range of 1.65~3.6V. When JP5 is set to the 2-3 position, IOVDD is connected to 3.3V. If a different voltage is required for IOVDD, set JP5 to the 1-2 position and connect the desired power supply to pin 9 of connector H1.

Note
If the IOVDD voltage is less than 3.0V, an oscillator working at the selected IOVDD voltage must be used.

4.2 Clocks

The clock for the S1D13771 TV-Out Graphics Engine is provided by a 27MHz oscillator.

The S5U13771P00C100 evaluation board has a DIP14 footprint for an optional second oscillator, Y2. This is provided for cases requiring a different clock frequency for the S1D13771 TV-Out Graphics Engine. To use Y2, an oscillator must be populated in the Y2 footprint and the following board modifications must be made:

1. remove R17 (33 ohm resistor, size 0402) to cut the output of Y1
2. populate R20 with a 33 ohm resistor, size 0402, to connect the output of Y2 to the CLKI input of the S1D13771 TV-Out Graphics Engine

Note
If the board is configured for an IOVDD voltage below 3.0V, an oscillator working at the selected IOVDD voltage must be used at Y2. The on-board 27MHz oscillator is not specified to work below 3.0V supply voltage.

4.3 Reset

The S1D13771 TV-Out Graphics Engine on the S5U13771P00C100 evaluation board can be reset using a push-button (SW1), or via an active low reset signal from the host development platform (pin 10 on connector H1).

4.4 LCDCS# Output and CS#SEL Signals

The S1D13771 TV-Out Graphics Engine may output the status of CS# input on the LCDCS# output pin. LCDCS# output is controlled by the CS#SEL input pin and S1D13771 register settings (REG[2Eh] bit 4). By default, the CS#SEL pin is pulled high, so the CS# signal is passed to internal the S1D13771 circuitry and LCDCS# output is controlled by the S1D13771 register setting.

4.5 Host Interface

4.5.1 Direct Host Bus Interface Support

All S1D13771 host interface pins are available on connector H1 which allows the S5U13771P00C100 evaluation board to be connected to a variety of development platforms.

The following figure shows the location of host bus connector H1. H1 is a 0.1x0.1" 20-pin header (10x2).

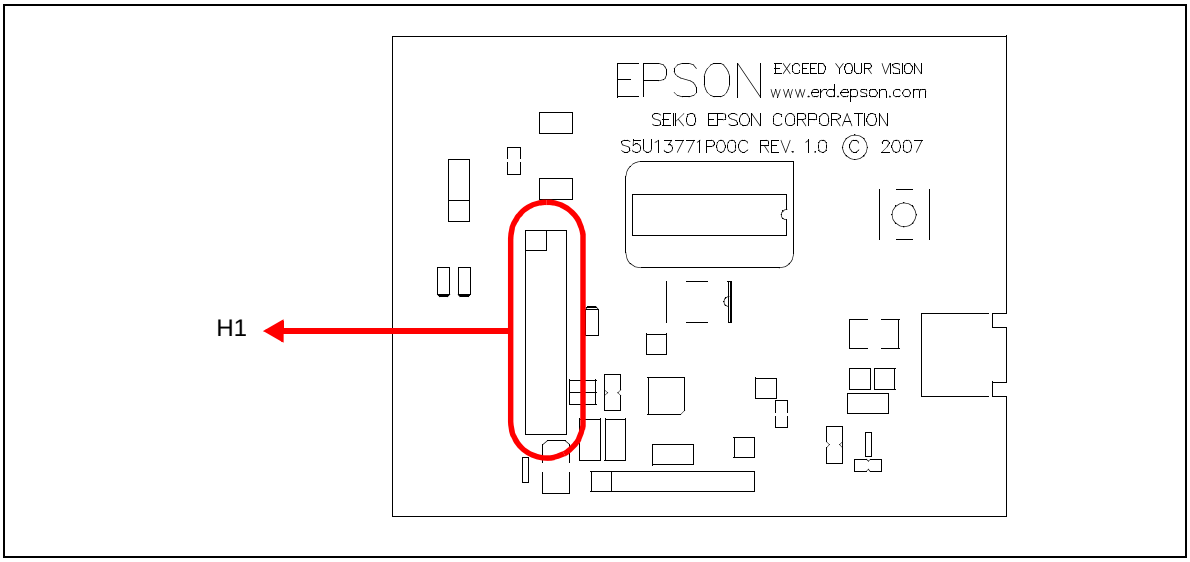

Figure 4-1: Host Bus Connector Location (H1)

For the pinout of connector H1, see "Schematic Diagrams" on page 18.

4.5.2 Connecting to the Epson S5U13U00P00C100 USB Adapter Board

The S5U13771P00C100 evaluation board is designed to connect to a S5U13U00P00C100 USB Adapter Board. The USB adapter board provides a simple connection to any computer via a USB 2.0 connection. The S5U13771P00C100 directly connects to the USB adapter board through connectors P1 and P2.

The USB adapter board also supplies the 3.3V power required by the S5U13771P00C100. IOVDD should be selected for 3.3V and JP5 should be set to the 2-3 position.

The following diagram shows the location of connectors P1 and P2. P1 and P2 are 40-pin headers (20x2).

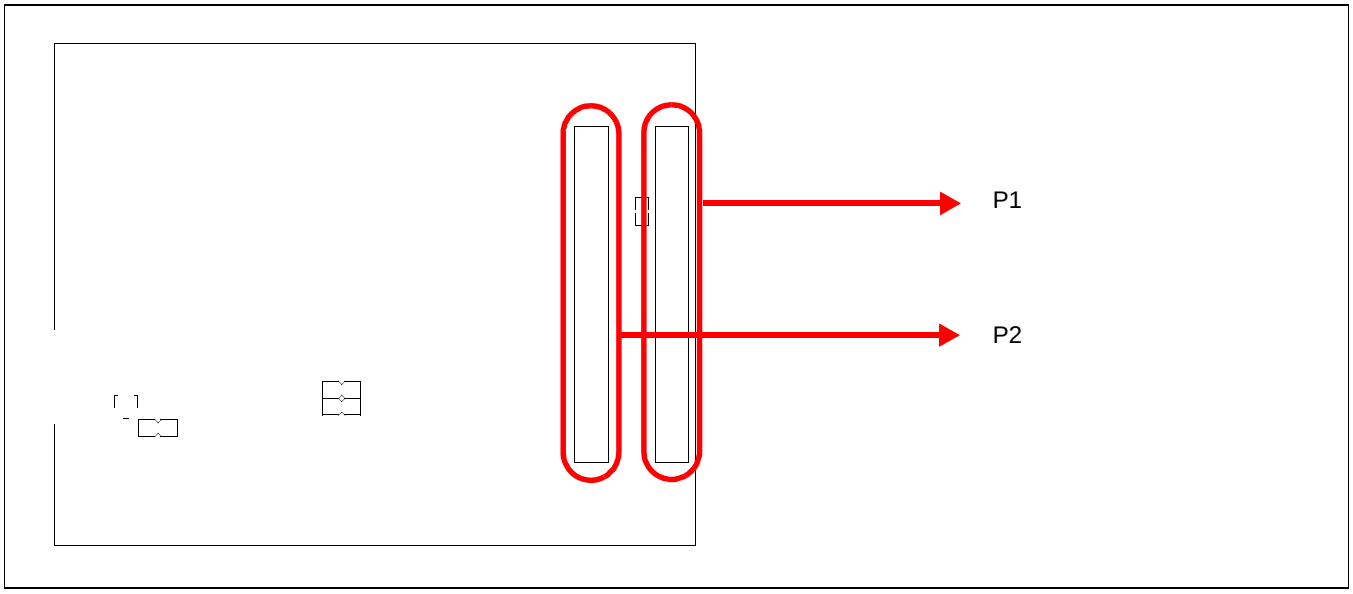

Figure 4-2: USB Adapter Connector Locations (P1 and P2)

For the pinout of connectors P1 and P2, see “Schematic Diagrams” on page 18.

Note

A windows driver must be installed on the PC for use of the S5U13U00P00C100 USB Adapter Board. The S1D13xxxUSB driver is available from www.erd.epson.com.

4.6 TV Output

The S1D13771 TV-Out Graphics Engine outputs a composite video signal. The S5U13771P00C100 evaluation board includes a standard TV composite video connector.

The S5U13771P00C100 board design includes an external TV output filter as described in the *S1D13771 Hardware Functional Specification*, document number X82A-A-001-xx.

The filter consists of components C30, C31, C32, and L3. To bypass the filter, remove resistors R8 and R9 (0 ohm resistors) and populate resistors R4 and R5 with 0 ohm resistors, size 0402. For circuit configuration, refer to "Schematic Diagrams" on page 18.

By default, the S1D13771 DAC is configured to use internal VREF. If an external VREF must be used, then a 1.23V reference must be provided to the TP1 VREF test point on the evaluation board. For further information, refer to the *S1D13771 Hardware Functional Specification*, document number X82A-A-001-xx.

The following figure shows the location of the TV out connector, CN1.

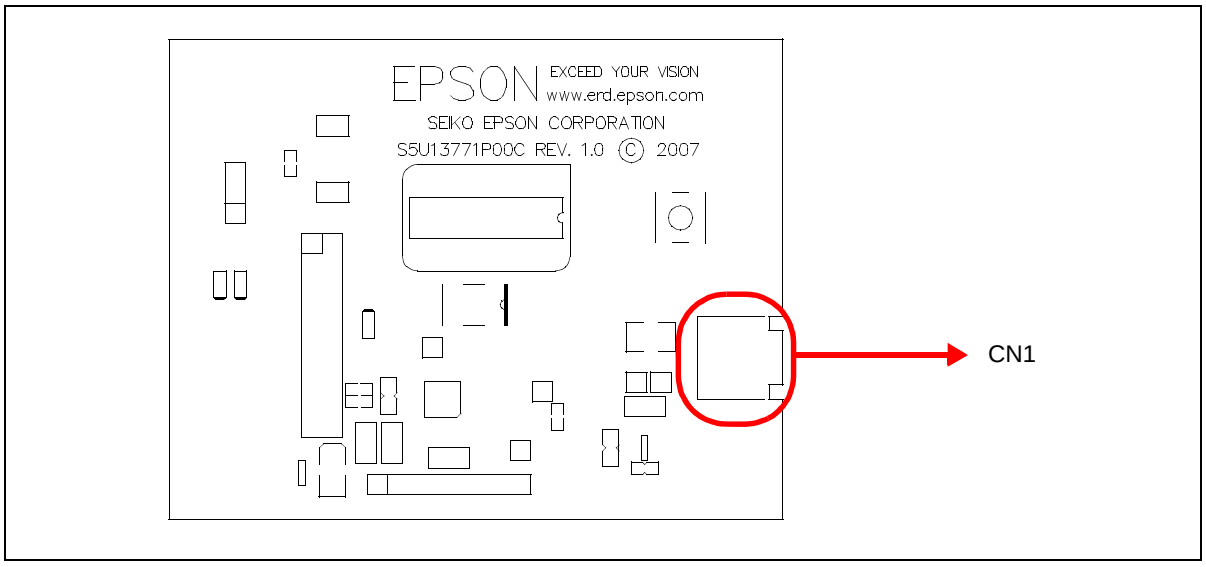

Figure 4-3: TV Out Connector Location (CN1)

For the pinout of connector CN1, see "Schematic Diagrams" on page 18.

4.7 GPIO Connections

The S1D13771 TV-Out Graphics Engine has 4 GPIO pins. All the GPIO pins are routed to the optional connector H2. Note that connector H2 is not populated on the S5U13771P00C100 evaluation board.

The following figure shows the location of the GPIO connector, H2.

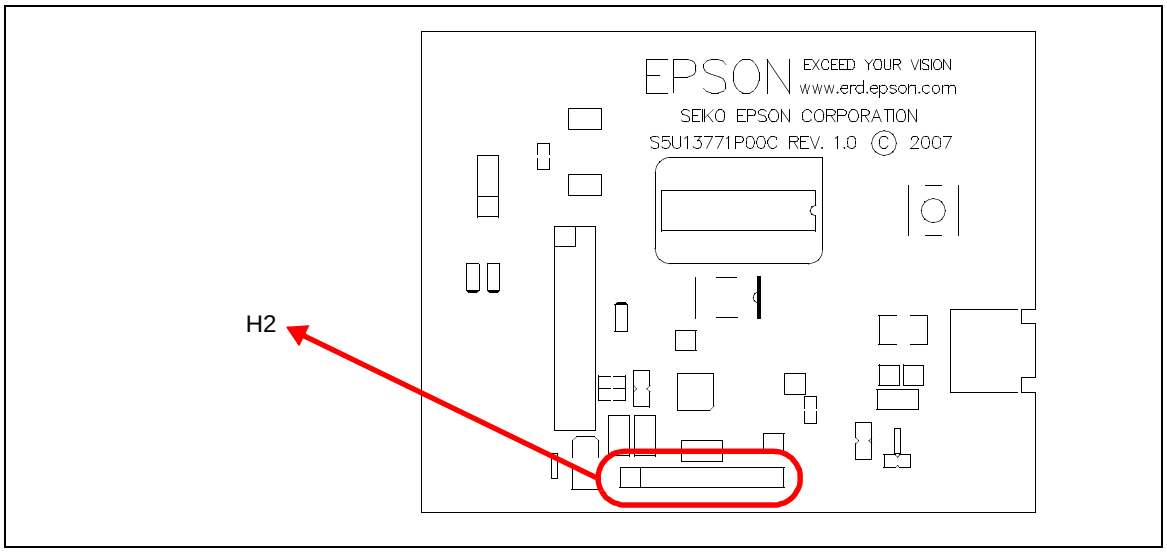

Figure 4-4: GPIO Connector Location (H2)

For the pinout of connector H2, see “Schematic Diagrams” on page 18.

5 Parts List

Table 5-1: Parts List

Item	Qty	Reference	Part	Description	Mfg / Mfg PN
1	1	CN1	VIDEO	CONN RCA JACK R/A YELLOW PCB	CUI Inc. RCJ-044
2	18	C1, C2, C3, C4, C5, C6, C14, C16, C18, C19, C20, C21, C22, C23, C33, C35, C36, C38	0.1uF		Yageo America 04022F104Z7B20D
3	1	C7	1nF		Yageo America 04022R102K9B20D
4	4	C8, C15, C17, C40	10uF		Panasonic - ECG ECJ-CV50J106M
5	12	C9, C10, C11, C12, C13, C24, C25, C26, C27, C28, C29, C42	0.01uF		Yageo America 0402ZRY5V7BB103
6	1	C30	33pF		Panasonic-ECG ECJ-0EC1H330J
7	1	C31	100pF		Murata Electronics GRM1555C1H101JZ01D
8	1	C32	270pF		Murata Electronics GRM155R71H271KA01D
9	2	C34, C39	0.01uF		Kemet C0402C103K4RACTU
10	1	C37	100uF 4V T		Kemet T494B107M004AS
11	1	C41	1uF		Murata Electronics GRM21BR71H105KA12L
12	1	C43	0.01uF		TDK C1608C0G1E103J
13	1	D1	BAT54S	DIODE SCHOTTKY DUAL 30V SOT23	ON Semiconductor BAT54SLT1G
14	1	D4	3.3V Power	LED GREEN SS TYPE LOW CUR SMD	Panasonic - SSG LNJ308G8LRA
15	1	H1	HEADER_10X2		Samtec TSW-110-07-G-D
16	0	H2	HEADER_8		Samtec TSW-108-07-G-D
17	4	JP1, JP2, JP3, JP4		CONN HEADER VERT 2POS .100 TIN or GENERIC	
18	1	JP5	IOVDD SOURCE	CONN HEADER VERT 3POS .100 TIN or GENERIC	
19	2	L1, L2	Ferrite	FERRITE 200MA 938 OHMS 0603 SMD	Steward HZ0603B751R-10
20	1	L3	1.8uH	INDUCTOR 1.8UH 290MA 1210 10%	Epcos B82422A1182K100
21	2	P1, P2	HEADER_20X2		3M 151240-8422-RB
22	2	R1, R21	1.5k 1%		

Table 5-1: Parts List

Item	Qty	Reference	Part	Description	Mfg / Mfg PN
23	1	R2	560 1%		
24	8	R3, R8, R9, R10, R15, R16, R19, R23	0		
25	0	R4, R5, R18, R20	NP		
26	3	R6, R11, R24	0		
27	1	R7	75 1%		
28	1	R14	270 1%		
29	1	R17	33 1%		
30	1	R22	10k		
31	5	SH1, SH2, SH3, SH4, SH5	.100 in. Jumper Shunt	JUMPER SHORTING TIN	Sullins Electronics Corp. STC02SYAN
32	1	SW1	SW TACT-SPST	SWITCH TACT SILVER PLT GULLWING	ITT Industries KSC241GLFS
33	2	TPGND1, TP3.3VDD1	TP_SMT	PC TEST POINT MINIATURE SMT	Keystone 5015
34	1	U1	S1D13771		
35	1	U2	TPS76915DBVT	IC 1.5V 100MA LDO REG SOT-23-5	Texas Instruments TPS76915DBVT
36	1	U3	LP3965		National Semiconductor LP3985IM5-3.0/NOPB
37	1	Y1	27M OSC	OSC 27MHz 3.3V 25ppm SMD	Connor-Winfield CWX813-27.0M
38	0	Y2	14-Pin DIP		AMP 2-641609-1

6 Schematic Diagrams

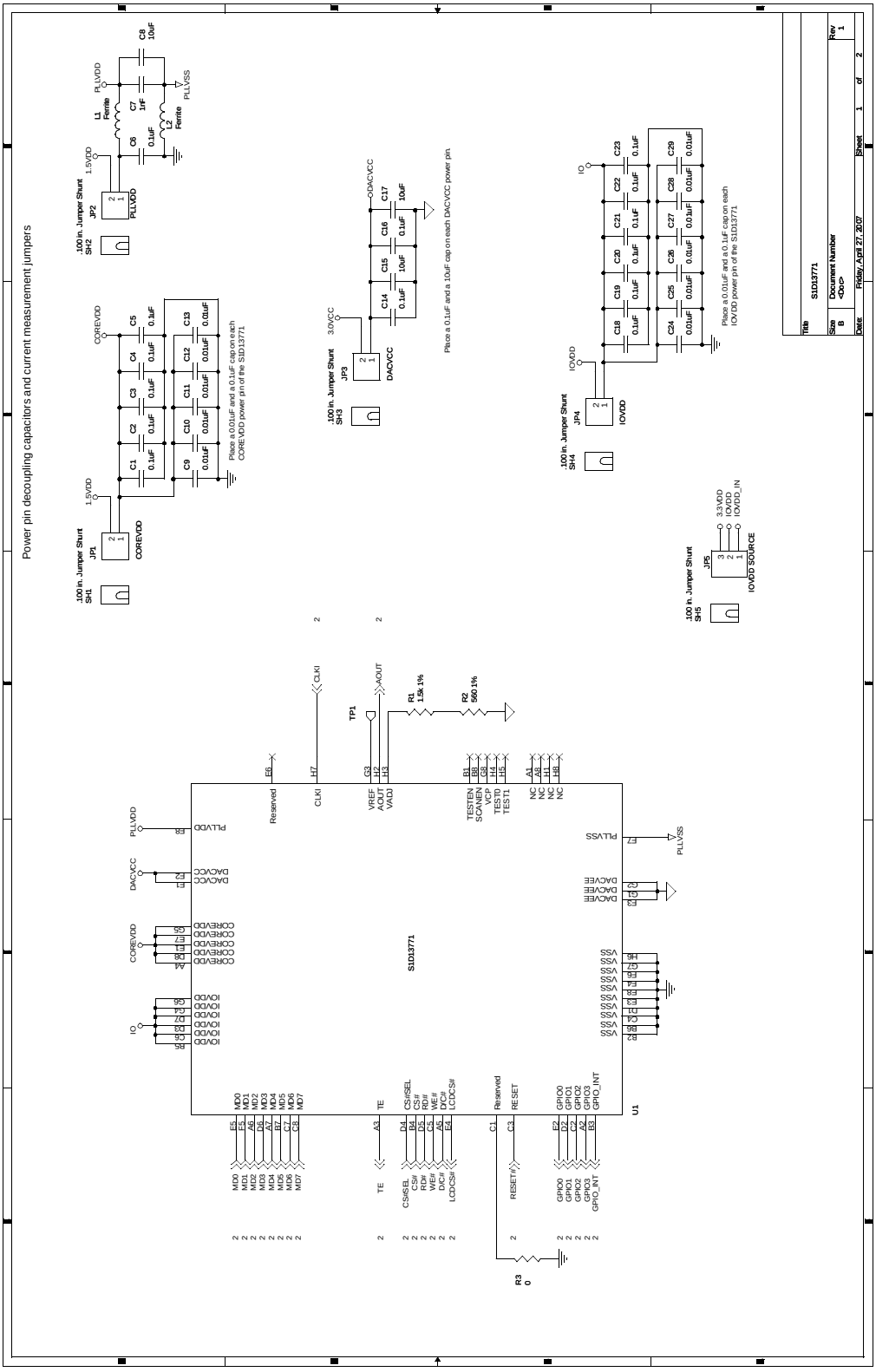

Figure 6-1: S5U13771P00C100 Schematics (1 of 2)

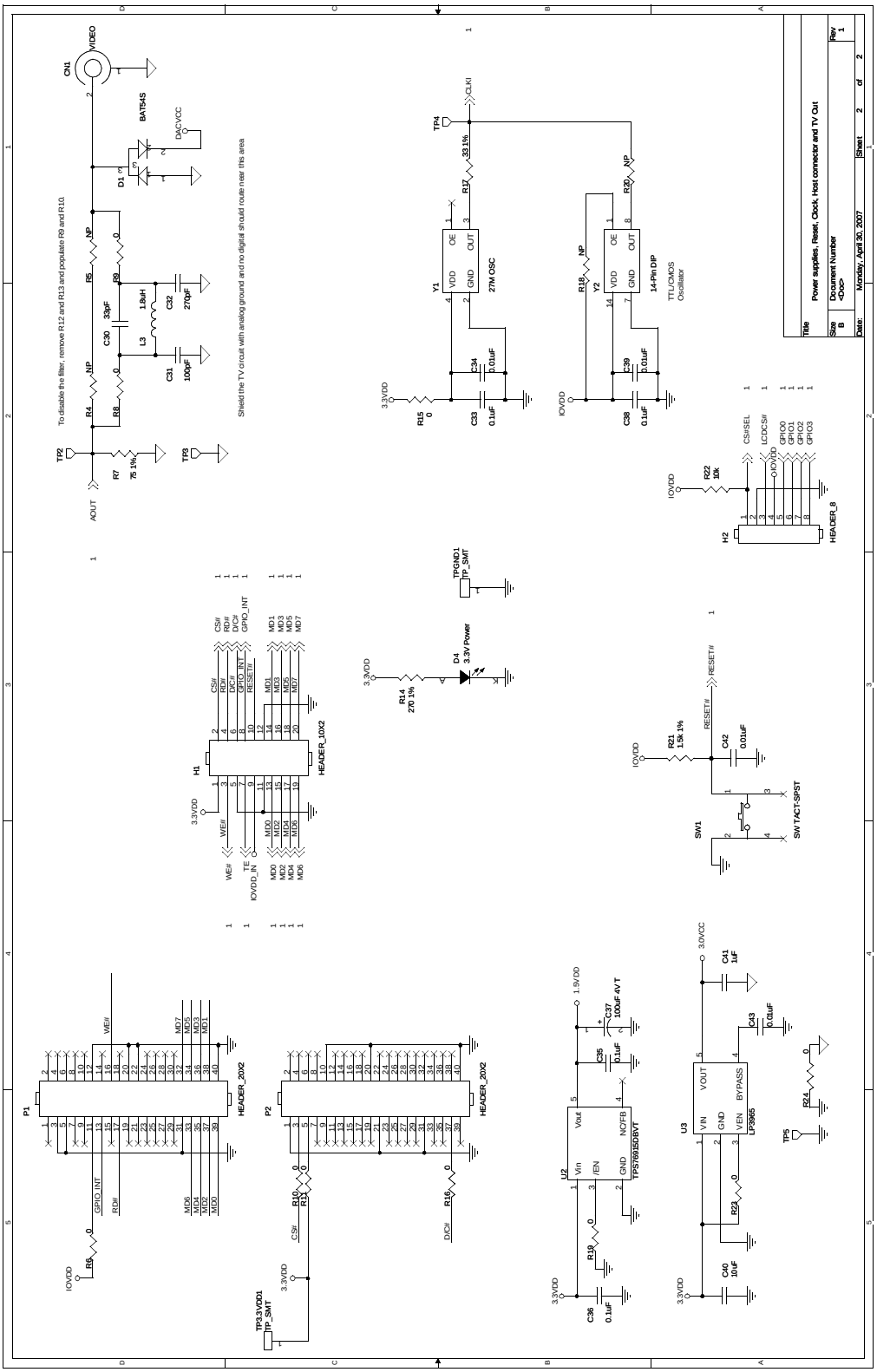

Figure 6-2: S5U13771P00C100 Schematics (2 of 2)

7 Board Layout

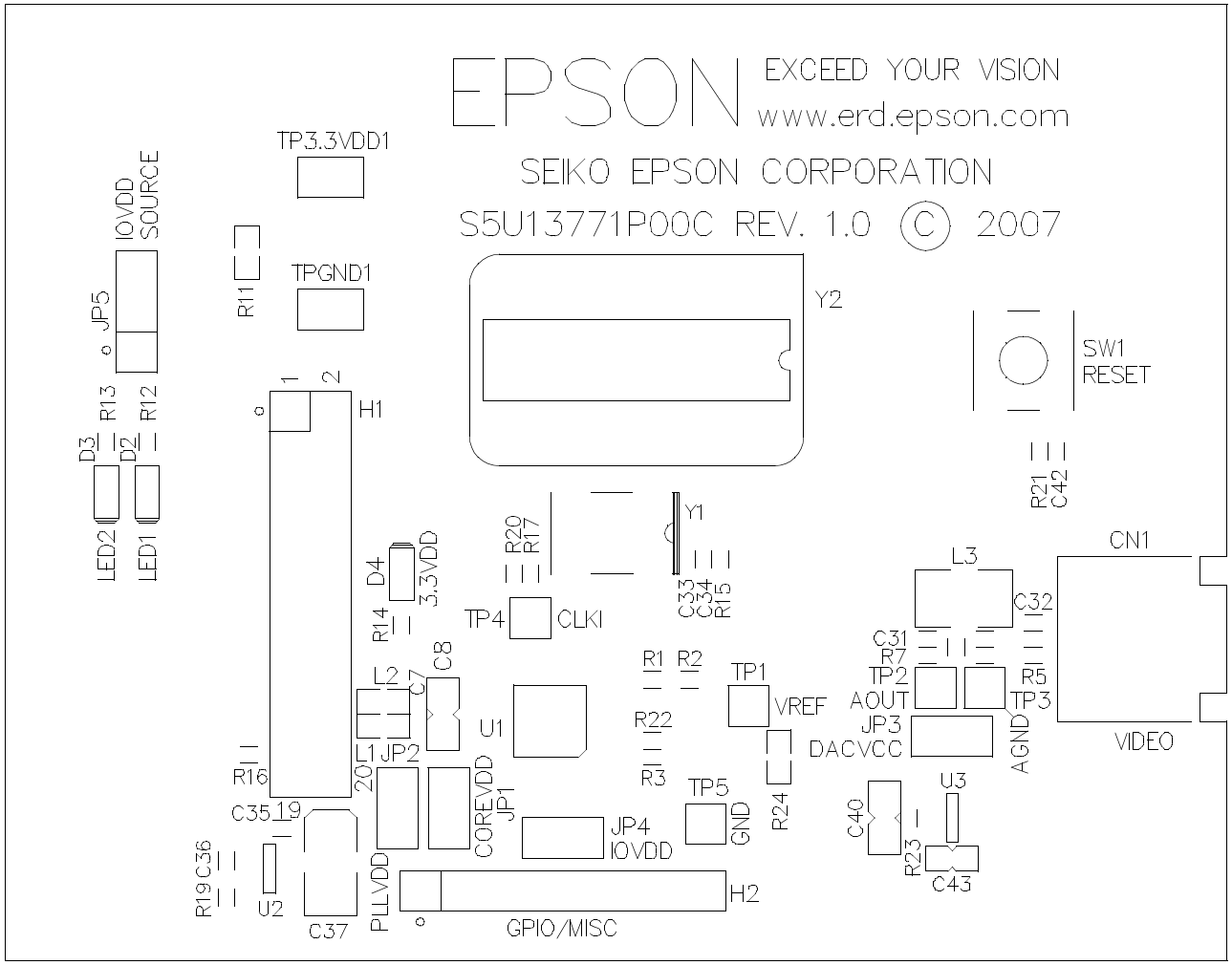

Figure 7-1: S5U13771P00C100 Board Layout - Top View

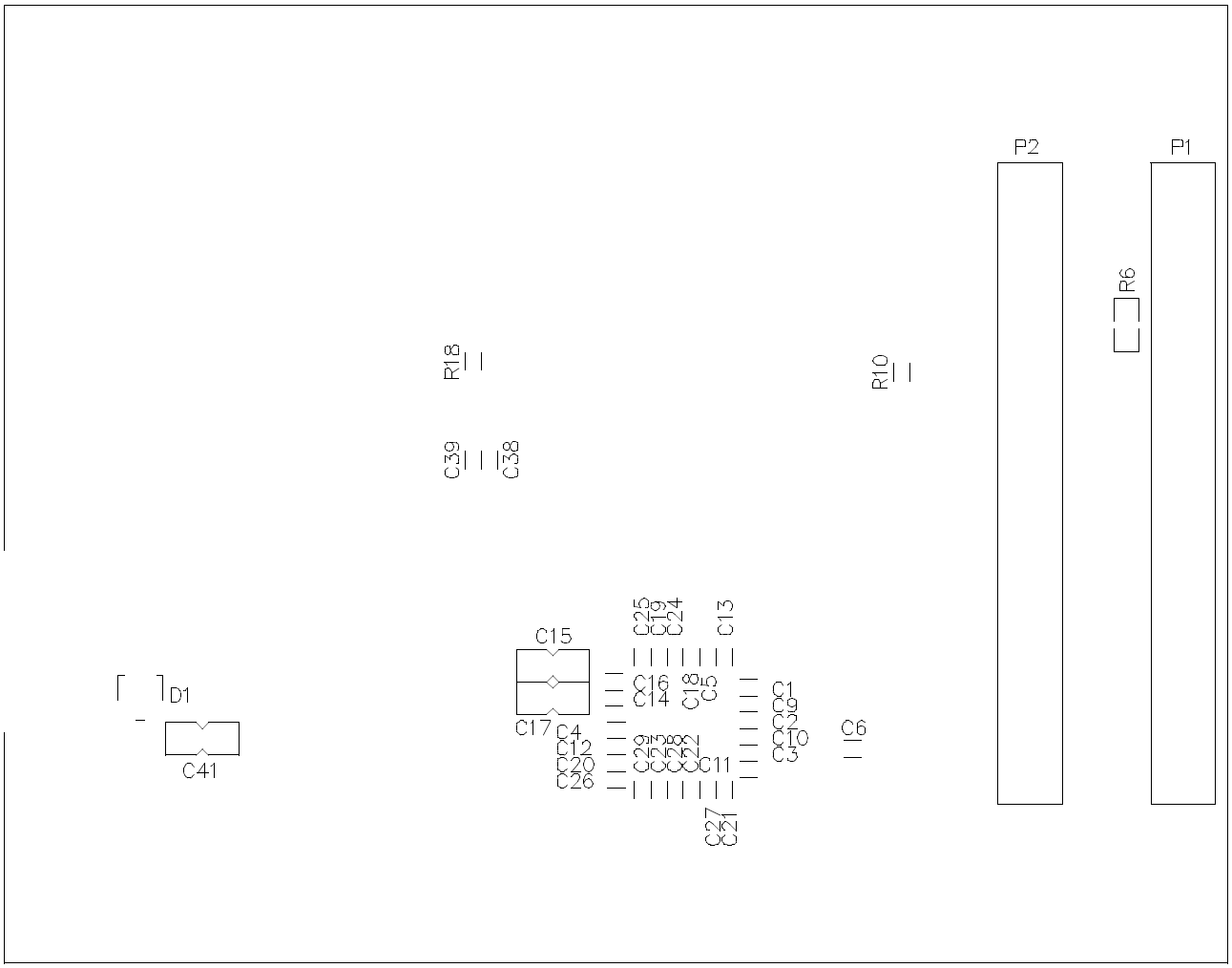

Figure 7-2: S5U13771P00C100 Board Layout - Bottom View

8 References

8.1 Documents

- Epson Research and Development, Inc., *S1D13771 Hardware Functional Specification*, document number X82A-A-001-xx.

8.2 Document Sources

- Epson Research and Development Website: http://www.erd.epson.com.

9 Technical Support

9.1 EPSON Display Controllers (S1D13771)

Japan
Seiko Epson Corporation
IC International Sales Group
421-8, Hino, Hino-shi
Tokyo 191-8501, Japan
Tel: 042-587-5812
Fax: 042-587-5564
http://www.epson.co.jp/

North America
Epson Electronics America, Inc.
2580 Orchard Parkway
San Jose, CA 95131, USA
Tel: (408) 922-0200
Fax: (408) 922-0238
http://www.eea.epson.com/

Taiwan
Epson Taiwan Technology & Trading Ltd.
14F, No. 7
Song Ren Road
Taipei 110, Taiwan, ROC
Tel: 02-8786-6688
Fax: 02-8786-6677
http://www.epson.com.tw/

Hong Kong
Epson Hong Kong Ltd.
20/F., Harbour Centre
25 Harbour Road
Wanchai, Hong Kong
Tel: 2585-4600
Fax: 2827-4346
http://www.epson.com.hk/

Europe
Epson Europe Electronics GmbH
Riesstrasse 15
80992 Munich, Germany
Tel: 089-14005-0
Fax: 089-14005-110
http://www.epson-electronics.de/

Singapore
Epson Singapore Pte Ltd
1 HarbourFront Place #03-02
HarbourFront Tower One
Singapore, 098633
Tel: (65) 6586-5500
Fax: (65) 6271-3182
http://www.epson.com.sg/

9.2 Ordering Information

To order the S5U13771P00C100 Evaluation Board, contact the Epson sales representative in your area and order part number **S5U13771P00C100**.

Change Record

X82A-G-003-01 Revision 1.0 - Issued: July 04, 2007

- released as revision 1.0