v3.1

Radiation-Hardened FPGAs

Features

- Guaranteed Total Dose Radiation Capability
- Low Single Event Upset Susceptibility
- High Dose Rate Survivability
- Latch-Up Immunity Guaranteed
- QML Qualified Devices
- Commercial Devices Available for Prototyping and Pre-Production Requirements
- Gate Capacities of 2,000 and 8,000 Gate Array Gates
- More Design Flexibility than Custom ASICs
- Significantly Greater Densities than Discrete Logic Devices
- Replaces up to 200 TTL Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to Two High-Speed, Low-Skew Clock Networks
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Non-Volatile, User Programmable Devices
- Fabricated in 0.8 μ Epitaxial Bulk CMOS Process
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer

Product Family Profile

Device	**RH1020**	**RH1280**
Capacity		
System Gates	3,000	12,000
Gate Array Equivalent Gates	2,000	8,000
PLD Equivalent Gates	6,000	20,000
TTL Equivalent Packages	50	200
20-Pin PAL Equivalent Packages	20	80
Logic Modules	547	1,232
S-Modules	0	624
C-Modules	547	608
Flip-Flops (Maximum)	273	998
Routing Resources		
Horizontal Tracks/Channel	22	35
Vertical Tracks/Channel	13	15
PLICE Antifuse Elements	186,000	750,000
User I/Os (Maximum)	69	140
Packages (by Pin Count)		
Ceramic Quad Flat Pack (CQFP)	84	172

Ordering Information

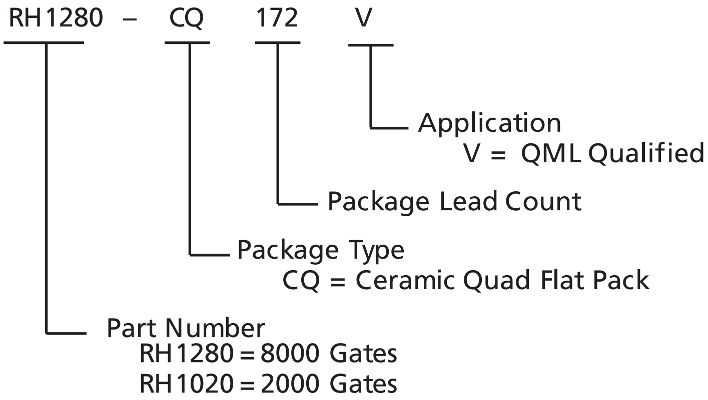


Figure 1-1 • **Ordering Information**

Ceramic Device Resources

	CQFP 84-Pin	CQFP 172-Pin
RH1020	69	–
RH1280	–	140

Table of Contents

Radiation-Hardened FPGAs

General Description

Actel Corporation, the leader in antifuse-based field programmable gate arrays (FPGAs), offers fully guaranteed RadHard versions of the A1280 and A1020 devices with gate densities of 8,000 and 2,000 gate array gates, respectively.

The RH1020 and RH1280 devices are processed in 0.8 μ, two-level metal epitaxial bulk CMOS technology. The devices are based on the Actel patented channeled array architecture, and employ Actel's PLICE antifuse technology. This architecture offers gate array flexibility, high performance, and fast design implementation through user programming.

Actel devices also provide unique on-chip diagnostic probe capabilities, allowing convenient testing and debugging. On-chip clock drivers with hard-wired distribution networks provide efficient clock distribution with minimum skew. A security fuse may be programmed to disable all further programming, and to protect the design from being copied or reverse engineered.

The RH1020 and RH1280 are available as fully qualified QML devices. Unlike traditional ASIC devices, the design does not have to be finalized six months prior to receiving the devices. Customers can make design modifications and program new devices within hours. These devices are fabricated, assembled, and tested at the Lockheed-Martin Space and Electronics facility in Manassas, Virginia on an optimized radiation-hardened CMOS process.

Radiation Survivability

In addition to all electrical limits, all radiation characteristics are tested and guaranteed, reducing overall system-level risks. With total dose hardness of 300 krad (Si), latch-up immunity, and a tested single event upset (SEU) of less than 1x10^{-6} errors/bit-day, these are the only RadHard, high-density field programmable products available today.

QML Qualification

Lockheed Martin Space and Electronics in Manassas, Virginia has achieved full QML certification, assuring that quality management, procedures, processes, and controls are in place from wafer fabrication through final test. QML qualification means that quality is built into the production process rather than verified at the end of the line by expensive and destructive testing. QML also ensures continuous process improvement, a focus on enhanced quality and reliability, and shortened product introduction and cycle time.

Actel Corporation has also achieved QML certification. All RH1020 and RH1280 devices will be shipped with a "QML" marking, signifying that the devices and processes have been reviewed and approved by DESC for QML status.

Development Tool Support

The RadHard family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA development software. Actel Libero IDE is a design management environment, seamlessly integrating design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE flow* diagram for more information (located on the Actel website).

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can select and lock package pins while only minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Applications

The RH1020 and RH1280 devices are targeted for use in military and space applications subject to radiation effects.

1. Accumulated Total Dose Effects

   With the significant increase in Earth-orbiting satellite launches and the ever-decreasing time-to-launch design cycles, the RH1020 and RH1280 devices offer the best combination of total dose radiation hardness and quick design implementation necessary for this increasingly competitive industry. In addition, the high total dose capability allows the use of these devices for deep space probes, which encounter other planetary bodies where the total dose radiation effects are more pronounced.

2. Single Event Effects (SEE)

   Many space applications are more concerned with the number of single event upsets and potential for latch-up in space. The RH1020 and RH1280 devices are latch-up immune, guaranteeing that no latch-up failures will occur. Single event upsets can occur in these devices as with all semiconductor products, but the rate of upset is low, as shown in Table 1-2 on page 1-6.

3. High Dose Rate Survivability

   An additional radiation concern is high dose rate survivability. Solar flares and sudden nuclear events can cause immediate high levels of radiation. The RadHard devices are appropriate for use in these types of applications, including missile systems, ground-based communication systems, and orbiting satellites.

RadHard Architecture

The RH1020 and RH1280 architecture is composed of fine-grained building blocks that produce fast and efficient logic designs. All the devices are composed of logic modules, routing resources, clock networks, and I/O modules, which are the building blocks for fast logic designs.

Logic Modules

RH1280 devices contain two types of logic modules, combinatorial (C-modules) and sequential (S-modules). RH1020 devices contain only C-modules.

The C-module, shown in Figure 1-1, implements the following function:

$$Y = !S1 \times !S0 \times D00 + !S1 \times S0 \times D01 + S1 \times !S0 \times D10 + S1 \times S0 \times D11$$

EQ 1-1

where

$$S0 = A0 \times B0$$

$$S1 = A1 + B1$$

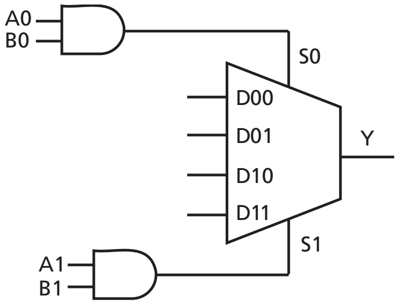


Figure 1-1 • **C-Module Implementation**

The S-module, shown in Figure 1-2 on page 1-3, is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-flip-flop or a transparent latch. To increase flexibility, the S-module register can be bypassed so it implements purely combinatorial logic.

Flip-flops can also be created using two C-modules. The single event upset (SEU) characteristics differ between an S-module flip-flop and a flip-flop created using two C-modules. For details see the Radiation Specifications table on Table 1-2 on page 1-6 and the *Design Techniques for RadHard Field Programmable Gate Arrays* application note.

The RH1020 Logic Module

The RH1020 logic module is an 8-input, one-output logic circuit chosen for the wide range of functions it implements and for its efficient use of interconnect routing resources (Figure 1-3 on page 1-3).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions, with different combinations of active-low inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs, and OR-ANDs. No dedicated hardwired latches or flip-flops are required in the array, since latches and flip-flops may be constructed from logic modules wherever needed in the application.

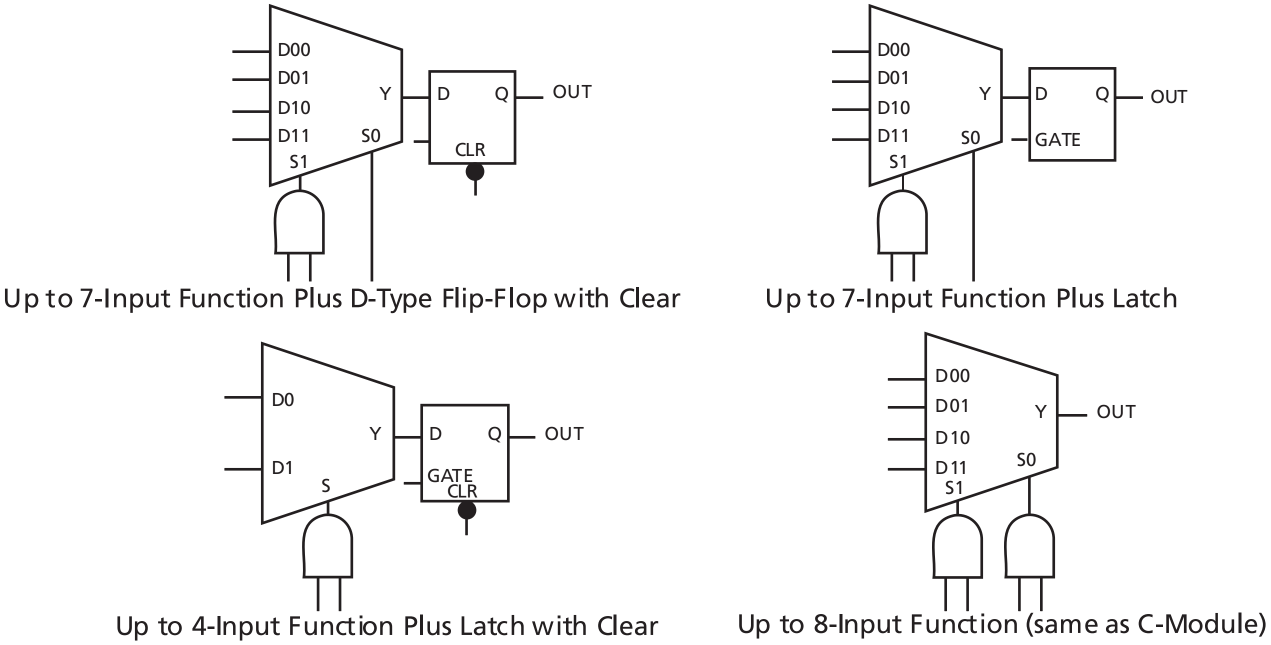


Figure 1-2 • **S-Module Implementation**

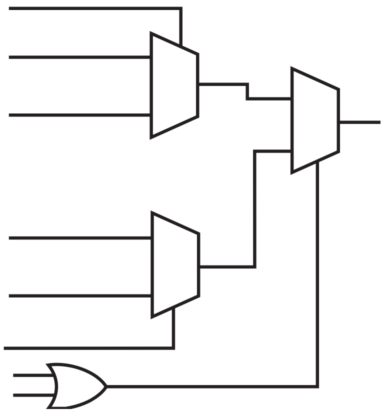
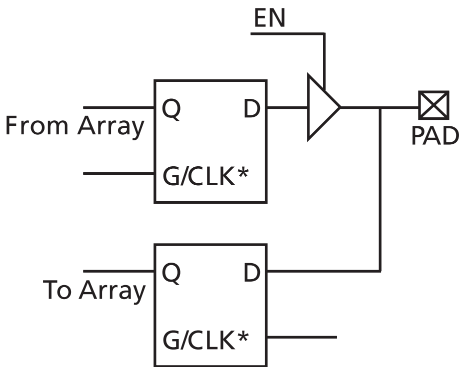


Figure 1-3 • **RH1020 Logic Module**



Note: **Can be configured as a Latch or D Flip-Flop (using C-Module).*

Figure 1-4 • **I/O Module**

I/O Modules

I/O modules provide the interface between the device pins and the logic array. A variety of user functions, determined by a library macro selection, can be implemented in the I/O modules (refer to the *Antifuse Macro Library Guide* for more information). I/O modules contain a tristate buffer, and input and output latches which can be configured for input, output, or bidirectional pins (Figure 1-4).

RadHard devices contain flexible I/O structures in that each output pin has a dedicated output enable control. The I/O module can be used to latch input and/or output data, providing a fast set-up time. In addition, the Actel Designer software tools can build a D-flip-flop, using a C-module, to register input and/or output signals.

Actel Designer development tools provide a design library of I/O macros that can implement all I/O configurations supported by the RadHard FPGAs.

Routing Structure

The RadHard device architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Varying segment lengths allow over 90 percent of the circuit interconnects to be made with only two antifuse connections. Segments can be joined together at the ends, using antifuses to increase their length up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

Horizontal Routing

Horizontal channels are located between the rows of modules, and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 1-5. Non-dedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

Vertical Routing

Another set of routing tracks run vertically through the module. There are three types of vertical tracks, input, output, and long, that can be divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 1-5.

Antifuse Structures

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures, as well as efficient programming algorithms. The structure is highly testable because there are no pre-existing connections, enabling temporary connections to be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed, as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

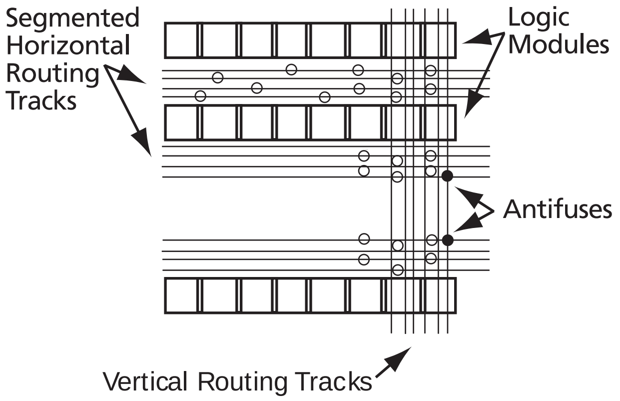


Figure 1-5 • **Routing Structure**

Related Documents

Application Notes

Design Techniques for RadHard Field Programmable Gate Arrays

http://www.actel.com/documents/Des_Tech_RH_AN.pdf

Analysis of SDI/DCLK Issue for RH1020 and RT1020

http://www.actel.com/documents/SDI_DCLK_AN.pdf

Simultaneously Switching Noise and Signal Integrity

http://www.actel.com/documents/SSN_AN.pdf

User's Guides

Antifuse Macro Library Guide

http://www.actel.com/documents/libguide_UG.pdf

QML Flow

Test Inspection	Method
Wafer Lot Acceptance	LMFS Procedure MAN-STC-Q014
Serialization	Required – 100%
Die Adhesion Test	2027 (Stud Pull)
Bond Pull Test	2011 (Wirebond)
Internal Visual	2010, Condition A
Temperature Cycle	1010, Condition C, 50 Cycles
Constant Acceleration	2001, Condition D or E, Y1 Orientation Only
Particle Impact Noise Detection (PIND)	2020, Condition A
X-Ray Radiography	2012
Pre Burn-In Electrical Parameters (T0)	Per Device Specification
Dynamic Burn-In	1015, 240 Hour Minimum, 125°C
Interim Electrical Parameters (T1)	Per Device Specification
Percent Defective Allowable (PDA)	LMFS Procedure MAN-STC-Q016
Static Burn-In	1015, 144 Hour Minimum, 125°C Minimum
Final Electrical Parameters (T2)	Per Device Specification
Percent Defective Allowable (PDA)	LMFS Procedure MAN-STC-Q016
Seal – Fine/Gross Leak	1014
External Visual (as required)	2009

Absolute Maximum Ratings

Table 1-1 • **Free Air Temperature Range**

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2,3,4,5]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source/Sink Current[6]	±20	mA
T_{STG}	Storage Temperature[2]	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.*
2. *Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions.*
3. $V_{PP} = V_{CC}$*, except during device operation.*
4. $V_{SV} = V_{CC}$*, except during device operation.*
5. $V_{KS} = GND$*, except during device operation.*
6. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than* V_{CC} *+ 0.5 V or less than GND – 0.5V, the internal protection diode will be forward-biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	**Military**	**Units**
Temperature Range[1]	–55 to +125	°C
Power Supply Tolerance[2]	±10	$\%V_{CC}$

Notes:

1. *Case temperature (T_C) is used.*
2. *All power supplies must be in the recommended operating range.*

Electrical Specifications

Symbol		**Test Conditions**	**Group A Subgroups**	**Limits Min.**	**Limits Max.**	**Units**
V_{OH}[1]		(I_{OH} = –4 mA)	1, 2, 3	3.7		V
V_{OL}[1]		(I_{OL} = 4 mA)	1, 2, 3		0.4	V
V_{IH}			1, 2, 3	2.2	V_{CC} + 0.3	V
V_{IL}			1, 2, 3	–0.3	0.8	V
Input Transition Time t_R, t_F[2]			—		500	ns
C_{IO}, I/O Capacitance[2]			4		20	pF
I_{IH}, I_{IL}		$V_{IN} = V_{CC}$ or GND V_{CC} = 5.5 V	1, 2, 3	–10	10	µA
I_{OZL}, I_{OZH}		$V_{OUT} = V_{CC}$ or GND V_{CC} = 5.5 V	1, 2, 3	–10	10	µA
I_{CC} Standby[3]			1, 2, 3		25	mA

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Not tested, for information only.*
3. *All outputs unloaded. All inputs = V_{CC} or GND.*

Radiation Specifications

Table 1-2 • **Radiation Specifications[1, 2]**

Symbol	**Characteristics**	**Conditions**	**Min.**	**Max.**	**Units**
RTD	Total Dose			300 k	Rad (Si)
SEL	Single Event Latch-Up	$-55°C \le T_{case} \le 125°C$		0	Fails/Device-Day
SEU1[3]	Single Event Upset for S-modules	$-55°C \le T_{case} \le 125°C$		1E-6	Upsets/Bit-Day
SEU2[3]	Single Event Upset for C-modules	$-55°C \le T_{case} \le 125°C$		1E-7	Upsets/Bit-Day
SEU3[3]	Single Event Fuse Rupture	$-55°C \le T_{case} \le 125°C$		<1	FIT (Fails/Device/1E9 Hrs)
RNF	Neutron Fluence		>1 E+12		N/cm^2

Notes:

1. *Measured at room temperature unless otherwise stated.*
2. *Device electrical characteristics are guaranteed for post-irradiation levels at worst-case conditions.*
3. *10% worst-case particle environment, geosynchronous orbit, 0.025" of aluminum shielding. Specification set using the CREME code upset rate calculation method with a 2 µ epi thickness.*

Package Thermal Characteristics

The device junction to case thermal characteristics is θ_{jc}, and the junction to ambient air characteristics is θ_{ja}. The thermal characteristics for θ_{ja} are listed with two different air flow rates, as shown in Table 1-3. Maximum junction temperature is 150°C.

A sample calculation of the maximum power dissipation for an 84-pin ceramic quad flat pack at commercial temperature is shown in EQ 1-2.

$$\frac{\text{Max. Junction Temperature (°C)} - \text{Max. Commercial Temperature (°C)}}{\theta_{ja}\text{(°C/W)}} = \frac{150°\text{C} - 70°\text{C}}{40°\text{C/W}} = 2.0\ \text{W}$$

EQ 1-2

Table 1-3 • **Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0 m/s 200 ft. / min.	θ_{ja} 2.5 m/s 500 ft. / min.	Units
Ceramic Quad Flat Pack	84	2.0	40.0	33.0	30.0	°C/W
Ceramic Quad Flat Pack	172	2.0	28.0	23.1	21.0	°C/W

Note: *θ_{jc} for CQFP packages refers to the thermal resistance between the junction and the bottom of the package.*

Power Dissipation

General Power Equation

$$P = [I_{CC}\text{standby} + I_{CC}\text{active}] \times V_{CC} + I_{OL} \times V_{OL} \times N + I_{OH} \times (V_{CC} - V_{OH}) \times M$$

EQ 1-3

where

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

Accurate values for N and M are difficult to determine because they depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Components

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for military, worst case conditions.

I_{CC}	V_{CC}	Power
25 mA	5.5 V	138 mW (max)
1 mA	5.5 V	5.5 mW (typ)

Active Power Components

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent and a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totempole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by EQ 1-4:

$$\text{Power (uW)} = C_{EQ} \times V_{CC}^2 \times F$$

EQ 1-4

where

C_{EQ} = Equivalent capacitance in pF

V_{CC} = Power supply in volts (V)

F = Switching frequency in MHz

Equivalent Capacitance

Equivalent capacitance is calculated by measuring I_{CC} active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency-independent so the results may be used over a wide range of operating conditions. Equivalent capacitance values follow.

C_{EQ} Values for Actel FPGAs

	RH1020	RH1280
Modules (C_{EQM})	3.7	5.2
Input Buffers (C_{EQI})	22.1	11.6
Output Buffers (C_{EQO})	31.2	23.8
Routed Array Clock Buffer Loads (C_{EQCR})	4.6	3.5

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 1-5 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 \times [(m \times C_{EQM} \times f_m)_{\text{modules}} + (n \times C_{EQI} \times f_n)_{\text{inputs}} + (p \times (C_{EQO} + C_L) \times f_p)_{\text{outputs}} + 0.5 \times (q_1 \times C_{EQCR} \times f_{q1})_{\text{routed\_Clk1}} + (r_1 \times f_{q1})_{\text{routed\_Clk1}} + 0.5 \times (q_2 \times C_{EQCR} \times f_{q2})_{\text{routed\_Clk2}} + (r_2 \times f_{q2})_{\text{routed\_Clk2}}]$$

EQ 1-5

where

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock (RH1280 only)

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock (RH1280 only)

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz (RH1280 only)

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r1 routed_Clk1	r2 routed_Clk2
RH1020	69	N/A
RH1280	168	168

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios, so they can be generally used to predict the upper limits of power dissipation. These guidelines are as follow:

Logic Modules (m) = 80% of Modules

Inputs Switching (n) = # Inputs/4

Outputs Switching (p) = # Outputs/4

First Routed Array Clock Loads (q_1) = 40% of Sequential Modules

Second Routed Array Clock Loads (q_2) (RH1280 only) = 40% of Sequential Modules

Load Capacitance (C_L) = 35 pF

Average Logic Module Switching Rate (f_m) = F/10

Average Input Switching Rate (f_n) = F/5

Average Output Switching Rate (f_p) = F/10

Average First Routed Array Clock Rate (f_{q1}) = F

Average Second Routed Array Clock Rate (f_{q2}) (RH1280 only) = F/2

Timing Models

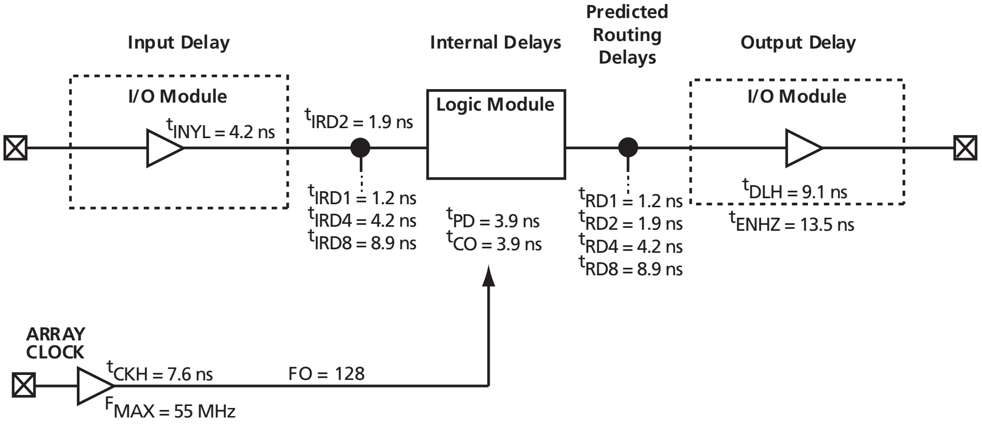
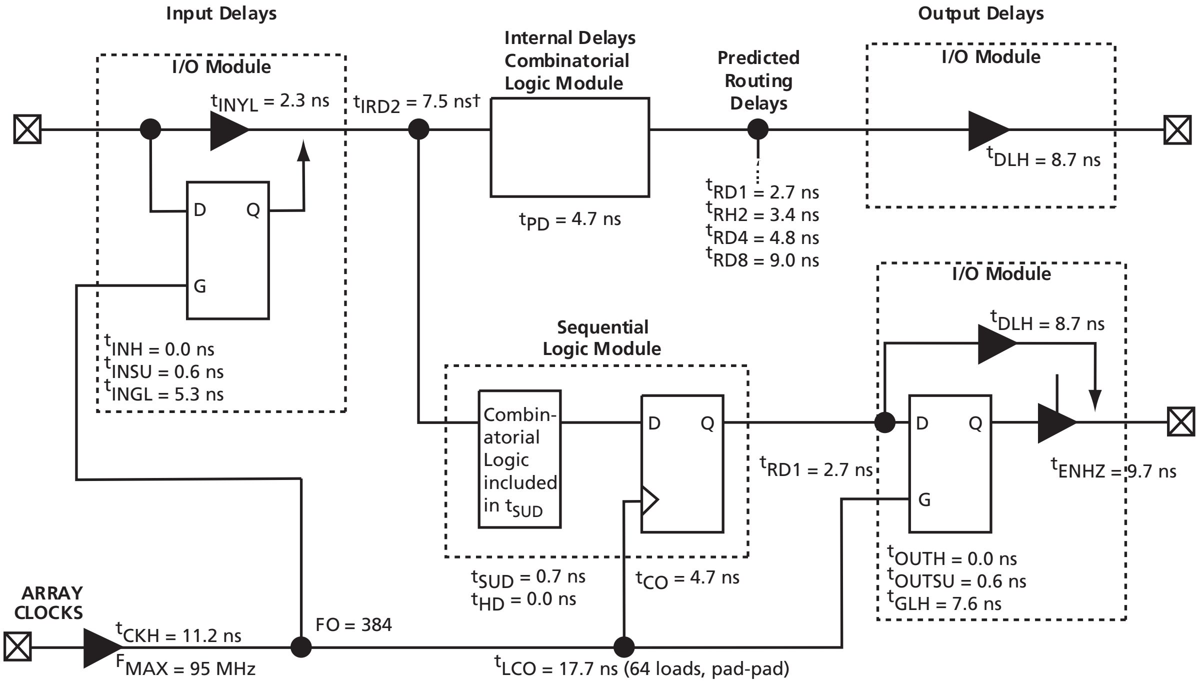


Figure 1-6 • **RH1020 Timing Model**



Note: *† Input module predicted routing delay.*

Figure 1-7 • **RH1280 Timing Model**

Parameter Measurement

Output Buffer Delays

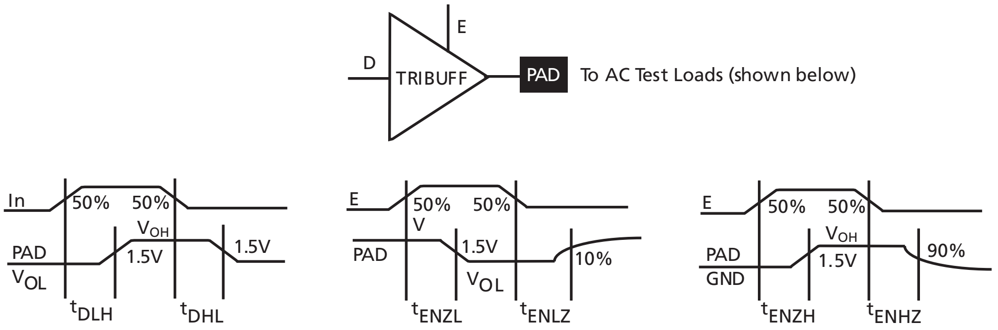


Figure 1-8 • **Output Buffer Delays**

AC Test Loads

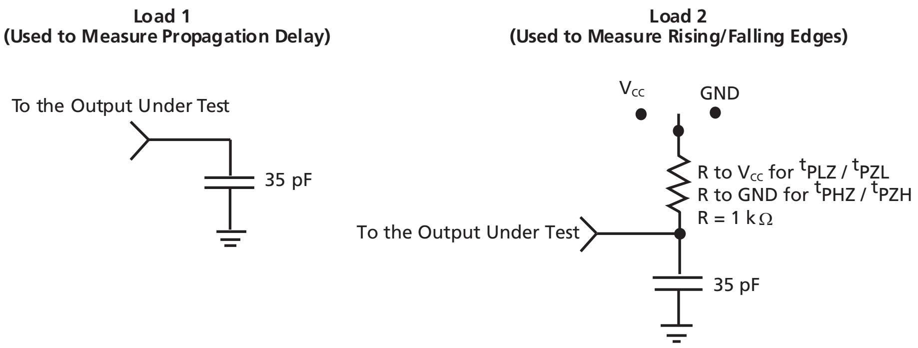


Figure 1-9 • **AC Test Loads**

Input Buffer Delays

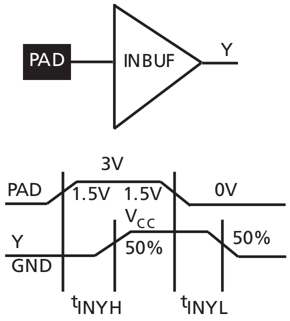


Figure 1-10 • **Input Buffer Delays**

Module Delays

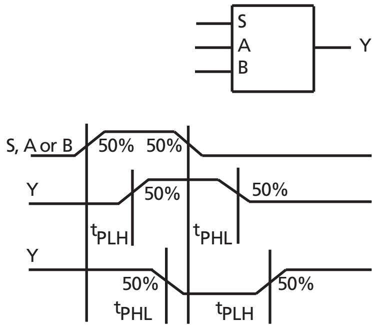
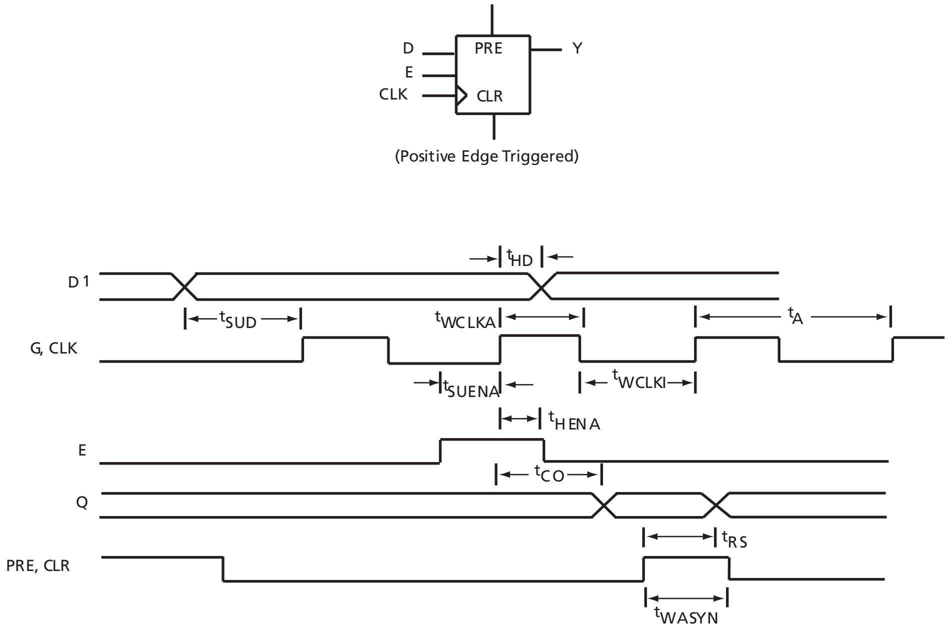


Figure 1-11 • **Module Delays**

Sequential Module Timing Characteristics

Flip-Flops and Latches



Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Figure 1-12 • **Flip-Flops and Latches**

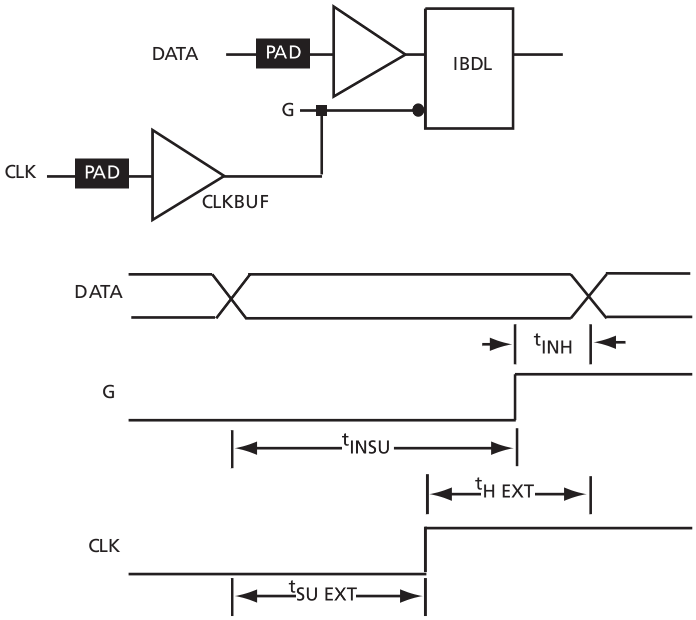


Figure 1-13 • **Input Buffer Latches**

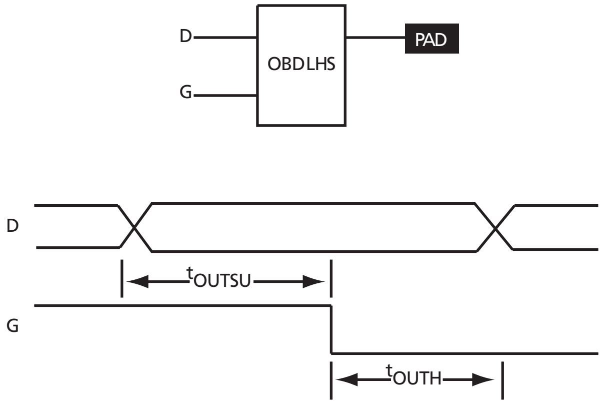


Figure 1-14 • **Output Buffer Latches**

Timing Characteristics

Table 1-4 • **RH1020 Timing Characteristics (Worst-Case Military Conditions, V_{CC} = 4.5 V, T_J = 125°C, RTD = 300 krad (Si))**

Parameter	Description	Min.	Max.	Units
Logic Module Propagation Delays				
t_{PD1}	Single Module		3.9	ns
t_{PD2}	Dual Module Macros		9.2	ns
t_{CO}	Sequential Clk to Q		3.9	ns
t_{GO}	Latch G to Q		3.9	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.9	ns
Logic Module Predicted Routing Delays[1]				
t_{RD1}	FO=1 Routing Delay		1.2	ns
t_{RD2}	FO=2 Routing Delay		1.9	ns
t_{RD3}	FO=3 Routing Delay		2.8	ns
t_{RD4}	FO=4 Routing Delay		4.2	ns
t_{RD8}	FO=8 Routing Delay		8.9	ns
Logic Module Sequential Timing [2]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	7.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	7.5		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	9.2		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	9.2		ns
t_A	Flip-Flop Clock Input Period	19.2		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		50	MHz
Input Module Propagation Delays				
t_{INYH}	Pad to Y High		4.2	ns
t_{INYL}	Pad to Y Low		4.2	ns
Input Module Predicted Routing Delays[1, 3]				
t_{IRD1}	FO=1 Routing Delay		1.2	ns
t_{IRD2}	FO=2 Routing Delay		1.9	ns
t_{IRD3}	FO=3 Routing Delay		2.8	ns
t_{IRD4}	FO=4 Routing Delay		4.2	ns
t_{IRD8}	FO=8 Routing Delay		8.9	ns

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Set-up times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
3. *Optimization techniques may further reduce delays by 0 to 4 ns.*
4. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Designer v3.0 (or later) Timer to check the hold time for this macro.*

Table 1-5 • **RH1020 Timing Characteristics**
(Worst-Case Military Conditions, V_{CC} = 4.5 V, T_J = 125°C, RTD = 300 krad (Si))

Parameter	**Description**		**Min.**	**Max.**	**Units**
Global Clock Network					
t_{CKH}	Input Low to High	FO = 16 FO = 128		6.6 7.6	ns
t_{CKL}	Input High to Low	FO = 16 FO = 128		8.7 9.5	ns
t_{PWH}	Minimum Pulse Width High	FO = 16 FO = 128	8.8 9.2		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16 FO = 128	1.6 2.4		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		1.6 2.5	ns
t_P	Minimum Period	FO = 16 FO = 128	17.9 19.2		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		55 50	MHz
TTL Output Module Timing[1]					
t_{DLH}	Data to Pad High			9.1	ns
t_{DHL}	Data to Pad Low			10.2	ns
t_{ENZH}	Enable Pad Z to High			8.9	ns
t_{ENZL}	Enable Pad Z to Low			10.7	ns
t_{ENHZ}	Enable Pad High to Z			13.5	ns
t_{ENLZ}	Enable Pad Low to Z			12.2	ns
d_{TLH}	Delta Low to High			0.08	ns/pF
d_{THL}	Delta High to Low			0.11	ns/pF
CMOS Output Module Timing[1]					
t_{DLH}	Data to Pad High			10.7	ns
t_{DHL}	Data to Pad Low			8.7	ns
t_{ENZH}	Enable Pad Z to High			8.1	ns
t_{ENZL}	Enable Pad Z to Low			11.2	ns
t_{ENHZ}	Enable Pad High to Z			13.5	ns
t_{ENLZ}	Enable Pad Low to Z			12.2	ns
d_{TLH}	Delta Low to High			0.14	ns/pF
d_{THL}	Delta High to Low			0.08	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Noise and Signal Integrity *application note.*

Table 1-6 • **RH1280 Timing Characteristics (Worst-Case Military Conditions, V_{CC} = 4.5 V, T_J = 125°C, RTD = 300 krad (Si))**

Parameter	Description	Min.	Max.	Units
Logic Module Propagation Delays[1]				
t_{PD1}	Single Module		4.7	ns
t_{CO}	Sequential Clk to Q		4.7	ns
t_{GO}	Latch G to Q		4.7	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		4.7	ns
Logic Module Predicted Routing Delays[2]				
t_{RD1}	FO=1 Routing Delay		2.7	ns
t_{RD2}	FO=2 Routing Delay		3.4	ns
t_{RD3}	FO=3 Routing Delay		4.1	ns
t_{RD4}	FO=4 Routing Delay		4.8	ns
t_{RD8}	FO=8 Routing Delay		9.0	ns
Sequential Timing Characteristics[3, 4]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.7		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.4		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	6.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	6.6		ns
t_A	Flip-Flop Clock Input Period	13.5		ns
t_{INH}	Input Buffer Latch Hold	0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.6		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.6		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		95	MHz

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External set-up/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal set-up (hold) time.*

Table 1-7 • **RH1280 Timing Characteristics (Worst-Case Military Conditions, V_{CC} = 4.5 V, T_J = 125°C, RTD = 300 krad (Si))**

Parameter	Description		Min.	Max.	Units
Input Module Propagation Delays					
t_{INYH}	Pad to Y High			1.9	ns
t_{INYL}	Pad to Y Low			2.3	ns
t_{INGH}	G to Y High			4.1	ns
t_{INGL}	G to Y Low			5.3	ns
Input Module Predicted Routing Delays*					
t_{IRD1}	FO=1 Routing Delay			6.8	ns
t_{IRD2}	FO=2 Routing Delay			7.5	ns
t_{IRD3}	FO=3 Routing Delay			8.2	ns
t_{IRD4}	FO=4 Routing Delay			8.9	ns
t_{IRD8}	FO=8 Routing Delay			11.7	ns
Global Clock Network					
t_{CKH}	Input Low to High	FO = 32 FO = 384		9.6 11.2	ns
t_{CKL}	Input High to Low	FO = 32 FO = 384		9.6 11.2	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 384	5.8 6.2		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 384	5.8 6.2		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		1.1 1.1	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 384	0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	4.6 5.8		ns
t_P	Minimum Period	FO = 32 FO = 384	11.8 13.0		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		105 95	MHz

Note: **Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment. Optimization techniques may further reduce delays by 0 to 4 ns.*

Table 1-8 • **RH1280 Timing Characteristics**
(Worst-Case Military Conditions, V_{CC} = 4.5 V, T_J = 125°C, RTD = 300 krad (Si))

Parameter	Description	Min.	Max.	Units
TTL Output Module Timing[1]				
t_{DLH}	Data to Pad High		6.8	ns
t_{DHL}	Data to Pad Low		7.6	ns
t_{ENZH}	Enable Pad Z to High		6.8	ns
t_{ENZL}	Enable Pad Z to Low		7.6	ns
t_{ENHZ}	Enable Pad High to Z		9.7	ns
t_{ENLZ}	Enable Pad Low to Z		9.7	ns
t_{GLH}	G to Pad High		7.6	ns
t_{GHL}	G to Pad Low		8.9	ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad), 64 Clock Loading		17.7	ns
t_{ACO}	Array Clock-Out (Pad-to-Pad), 64 Clock Loading		25.0	ns
d_{TLH}	Capacitive Loading, Low to High		0.07	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.09	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data to Pad High		8.7	ns
t_{DHL}	Data to Pad Low		6.4	ns
t_{ENZH}	Enable Pad Z to High		6.8	ns
t_{ENZL}	Enable Pad Z to Low		7.6	ns
t_{ENHZ}	Enable Pad High to Z		9.7	ns
t_{ENLZ}	Enable Pad Low to Z		9.7	ns
t_{GLH}	G to Pad High		7.6	ns
t_{GHL}	G to Pad Low		8.9	ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad), 64 Clock Loading		20.1	ns
t_{ACO}	Array Clock-Out (Pad-to-Pad), 64 Clock Loading		29.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.09	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.08	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the* Simultaneously Switching Noise and Signal Integrity *application note.*

Pin Description

CLKA **Clock A (Input)**

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB **Clock B (Input)**

Not applicable for RH1020. TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK[1] **Diagnostic Clock (Input)**

TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. If the Program fuse is not programmed and DCLK is undefined, it is configured as an inactive input. In this case, tie the DCLK pin to ground. If the Program fuse is programmed and DCLK is undefined, it will become an active LOW output.The Program fuse must be programmed if the DCLK pin is used as an output or a bidirectional pin.

GND **Ground**

LOW supply voltage.

I/O **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the Designer software.

MODE **Mode (Input)**

The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide debugging capability, the MODE pin should be terminated to GND through a 10 kΩ resistor so that the MODE pin can be pulled HIGH when required.

NC **No Connection**

This pin is not connected to circuitry within the device.

PRA, I/O **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin’s probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI[1] **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. If the Program fuse is not programmed and SDI is undefined, it is configured as an inactive input. In this case, tie the SDI pin to ground. If the Program fuse is programmed and SDI is undefined, it will become an active LOW output.The Program fuse must be programmed if the SDI pin is used as an output or a bidirectional pin.

V_{CC} **5.0V Supply Voltage**

HIGH supply voltage.

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[1] *Please refer to the Actel Technical Brief* Analysis of SDI/DCLK Issue for RH1020 and RT1020.

Package Pin Assignments

84-Pin CQFP

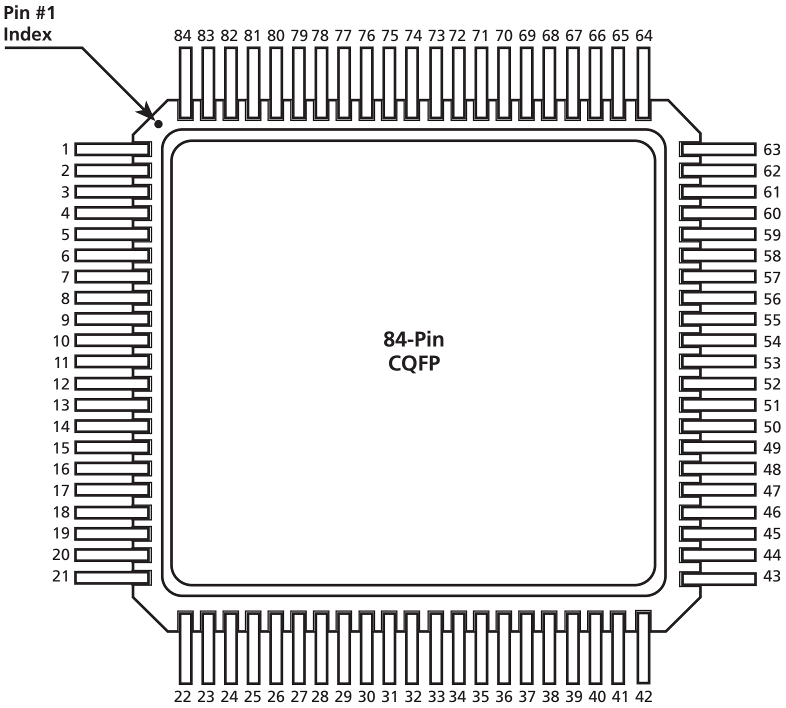

Figure 2-1 • **84-Pin CQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

84-Pin CQFP	
Pin Number	RH1020 Function
1	NC
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	GND
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	V_{CC}
15	V_{CC}
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	V_{CC}
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	GND
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	V_{CC}
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	GND
50	GND
51	I/O
52	I/O
53	CLKA, I/O
54	I/O
55	MODE
56	V_{CC}
57	V_{CC}
58	I/O
59	I/O
60	I/O
61	SDI, I/O
62	DCLK, I/O
63	PRA, I/O
64	PRB, I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	GND
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	V_{CC}
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O

172-Pin CQFP

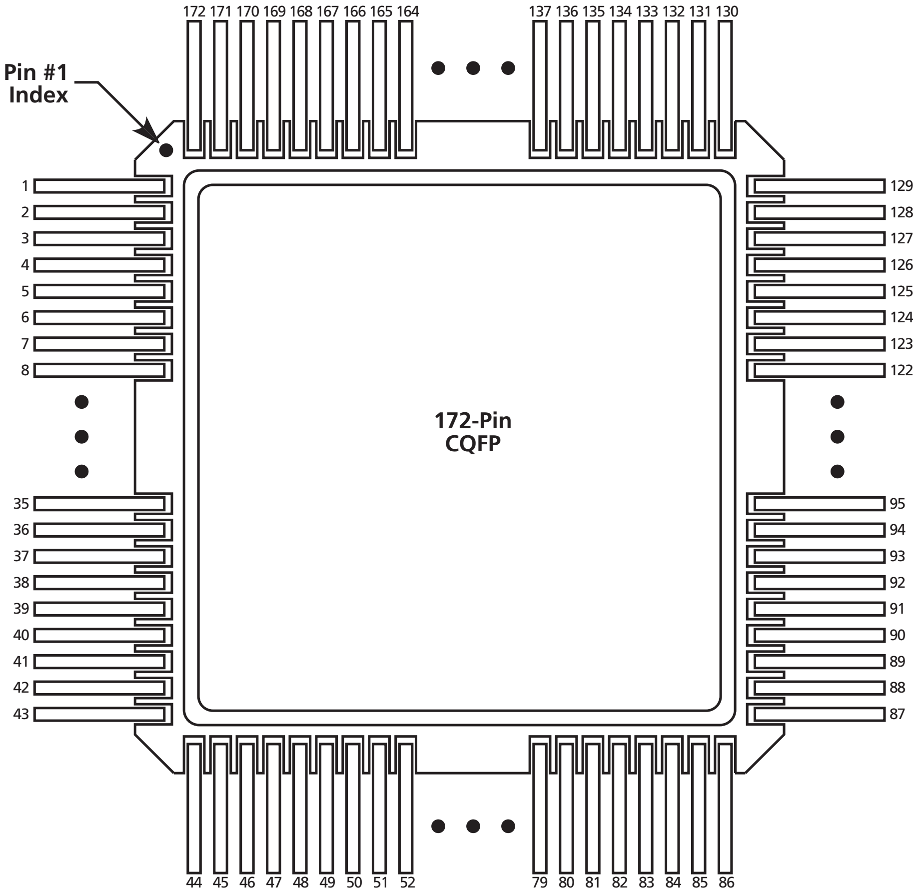

Figure 2-2 • **172-Pin CQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Package Resource center at http://www.actel.com/products/rescenter/package/index.html.

172-Pin CQFP	
Pin Number	**RH1280A Function**
1	MODE
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	GND
8	I/O
9	I/O
10	I/O
11	I/O
12	V_{CC}
13	I/O
14	I/O
15	I/O
16	I/O
17	GND
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	V_{CC}
24	V_{CC}
25	I/O
26	I/O
27	V_{CC}
28	I/O
29	I/O
30	I/O
31	I/O
32	GND
33	I/O
34	I/O
35	I/O

172-Pin CQFP	
Pin Number	**RH1280A Function**
36	I/O
37	GND
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	V_{CC}
51	I/O
52	I/O
53	I/O
54	I/O
55	GND
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	GND
66	V_{CC}
67	I/O
68	I/O
69	I/O
70	I/O

172-Pin CQFP	
Pin Number	**RH1280A Function**
71	I/O
72	I/O
73	I/O
74	I/O
75	GND
76	I/O
77	I/O
78	I/O
79	I/O
80	V_{CC}
81	I/O
82	I/O
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	GND
99	I/O
100	I/O
101	I/O
102	I/O
103	GND
104	I/O
105	I/O

172-Pin CQFP	
Pin Number	**RH1280A Function**
106	GND
107	V_{CC}
108	GND
109	V_{CC}
110	V_{CC}
111	I/O
112	I/O
113	V_{CC}
114	I/O
115	I/O
116	I/O
117	I/O
118	GND
119	I/O
120	I/O
121	I/O
122	I/O
123	GND
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	SDI, I/O
132	I/O
133	I/O
134	I/O
135	I/O
136	V_{CC}
137	I/O
138	I/O
139	I/O
140	I/O

172-Pin CQFP	
Pin Number	**RH1280A Function**
141	GND
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	PRA, I/O
149	I/O
150	CLKA, I/O
151	V_{CC}
152	GND
153	I/O
154	CLKB, I/O
155	I/O
156	PRB, I/O
157	I/O
158	I/O
159	I/O
160	I/O
161	GND
162	I/O
163	I/O
164	I/O
165	I/O
166	V_{CC}
167	I/O
168	I/O
169	I/O
170	I/O
171	DCLK, I/O
172	I/O

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.1)	Page
v3.0	"Development Tool Support" section was updated.	1-1
	Table 1-1 was updated.	1-5
	Table 1-2 was updated.	1-6
	Table 1-3 was updated.	1-7
	The "DCLK Diagnostic Clock (Input)" section was updated.	1-18
	The "SDI1 Serial Data Input (Input)" section was updated.	1-18

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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