Innovasic®
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The Industrial Semiconductor Solutions Company

IA82527
Serial Communications Controller · CAN Protocol

Data Sheet

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1. Introduction

The Innovasic Semiconductor IA82527 Controller Area Network (CAN) Serial Communications Controller is a form, fit, and function replacement for the original Intel® 82527 Serial Communications Controller.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures complete compatibility with the original device, including any "undocumented features." Additionally, MILES™ captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA82527 Serial Communications Controller replaces the obsolete Intel® 82527 device, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

NOTE

This data sheet contains preliminary information for the Innovasic Semiconductor IA82527 Serial Communications Controller. The finalized data sheet that documents all necessary engineering information about the IA82527 will be available when the device nears completion in Q2 2008.

1.1 General Description

Controller Area Network (CAN) protocol uses a multi-master CSMA/CR (Carrier Sense, Multiple Access with Collision Resolution) bus to transfer message objects between network nodes.

The IA82527 supports CAN Specification 2.0 Part A and B, standard and extended message frames, and has the capability to transmit, receive, and perform message filtering on extended message frames.

The IA82527 can store 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for the last message object, which is receive-only. The last message object also provides a special acceptance mask designed to allow select groups of different message identifiers to be received.

The IA82527 also provides a programmable acceptance mask that allows users to globally mask any identifier bits of the incoming message. This global mask can be used for both standard and extended message frames.

1.2 Features

The primary features of the IA82527 are as follows:

- CAN Protocol Support
  - Specification 2.0, Part A and Part B
  - Standard Data and Remote Frames
  - Extended Data and Remote Frames
- CAN Bus Interface
  - Configurable Input Comparator
  - Configurable Output Driver
- Global Mask, Programmable
  - Standard Message Identifier
  - Extended Message Identifier
- Message Objects
  - 14 Transmit/Receive Buffers
  - 1 Receive Buffer with Programmable Mask
- Programmable Bit Rate
- Flexible Status Interface
- CPU Interface Options
  - 16-Bit Multiplexed Intel® Architecture
  - 8-Bit Multiplexed Intel® Architecture
  - 8-Bit Multiplexed Non-Intel® Architecture
  - 8-Bit Non-Multiplexed Non-Intel® Architecture
  - Serial (SPI)
- I/O Ports (2)
  - 8-Bit
  - Bidirectional
- Flexible Interrupt Structure
- Programmable Clock Output

A more detailed description of the IA82527, including the features listed above, is provided in Section 4.

2. Packaging and Pin Descriptions

2.1 Packages and Pinouts

The Innovasic Semiconductor IA82527 CAN Serial Communications Controller is available in the following packages:

- 44-Pin Plastic Leaded Chip Carrier (PLCC)
- 44-Pin Quad Flat Pack (QFP)

The 44-pin PLCC package is shown in Figure 1/Table 1, and the 44-pin QFP package is shown in Figure 2/Table 2.

Detailed descriptions of pin/signal functions are provided in section 2.2 (Table 3).

NOTE
Table 1 (PLCC package) and Table 2 (QFP package) provide numerical indexes of pin names. Table 3 provides an alphabetical index of pin and signal descriptions.

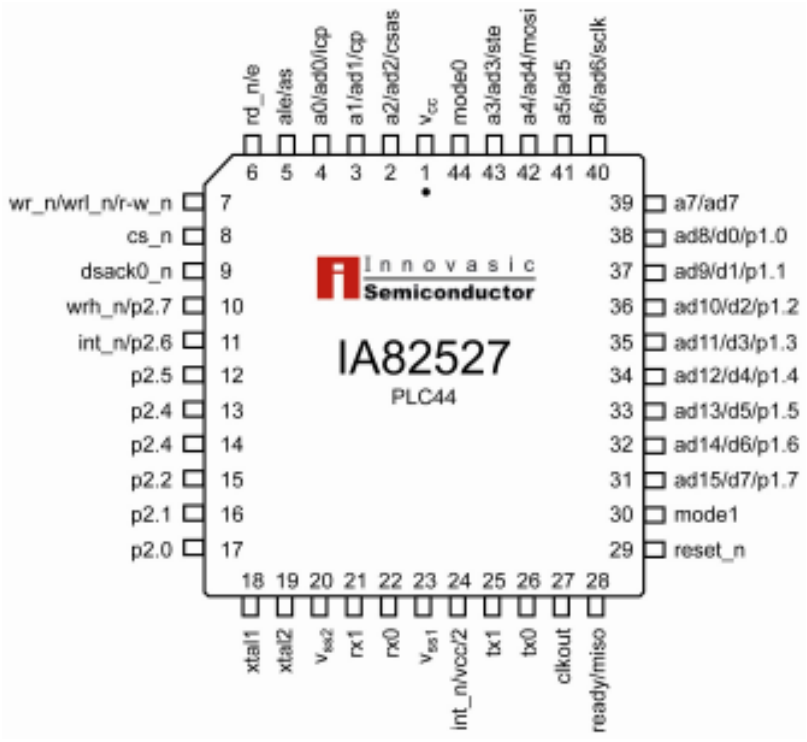

Figure 1. IA82527 44-Pin PLCC Package Diagram

Table 1. IA82527 44-Pin PLCC Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	v_{cc}	12	p2.5	23	v_{ss1}	34	ad12/d4/p1.4
2	a2/ad2/csas	13	p2.4	24	int_n/v_{cc}/2	35	ad11/d3/p1.3
3	a1/ad1/cp	14	p2.3	25	tx1	36	ad10/d2/p1.2
4	a0/ad0/icp	15	p2.2	26	tx0	37	ad9/d1/p1.1
5	ale/as	16	p2.1	27	clkout	38	ad8/d0/p1.0
6	rd_n/e	17	p2.0	28	ready/miso	39	a7/ad7
7	wr_n/wrl_n/r-w_n	18	xtal1	29	reset_n	40	a6/ad6/sclk
8	cs_n	19	xtal2	30	mode1	41	a5/ad5
9	dsack0_n	20	v_{ss2}	31	ad15/d7/p1.7	42	a4/ad4/mosi
10	wrh_n/p2.7	21	rx1	32	ad14/d6/p1.6	43	a3/ad3/ste
11	int_n/p2.6	22	rx0	33	ad13/d5/p1.5	44	mode0

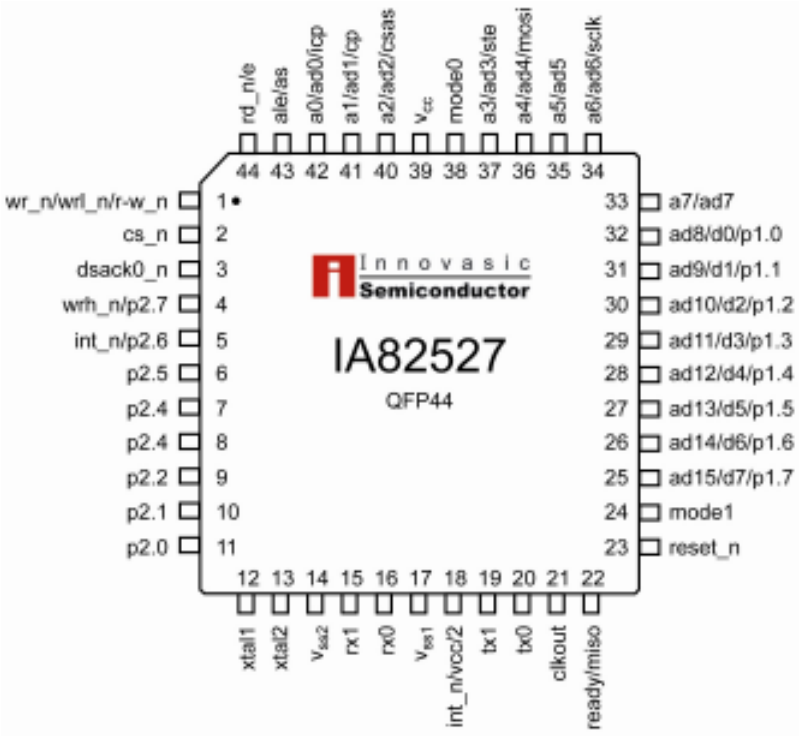

Figure 2. IA82527 44-Pin QFP Package Diagram

Table 2. IA82527 44-Pin QFP Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	wr_n/wrl_n/r-w_n	12	xtal1	23	reset_n	34	a6/ad6/sclk
2	cs_n	13	xtal2	24	mode1	35	a5/ad5
3	dsack0_n	14	V_{ss2}	25	ad15/d7/p1.7	36	a4/ad4/mosi
4	wrh_n/p2.7	15	rx1	26	ad14/d6/p1.6	37	a3/ad3/ste
5	int_n/p2.6	16	rx0	27	ad13/d5/p1.5	38	mode0
6	p2.5	17	V_{ss1}	28	ad12/d4/p1.4	39	V_{cc}
7	p2.4	18	int_n/V_{cc}/2	29	ad11/d3/p1.3	40	a2/ad2/csas
8	p2.3	19	tx1	30	ad10/d2/p1.2	41	a1/ad1/cp
9	p2.2	20	tx0	31	ad9/d1/p1.1	42	a0/ad0/icp
10	p2.1	21	clkout	32	ad8/d0/p1.0	43	ale/as
11	p2.0	22	ready/miso	33	a7/ad7	44	rd_n/e

2.2 Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA82527 Serial Communications Controller are provided in Table 3.

Several of the IA82527 pins have different functions depending on the operating mode of the device. Each of the different *signals* supported by a pin is listed and defined in Table 3, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for both the PLCC and QFP packages are provided in the "Pin" column. If the signal and pin names are the same, no entry is provided in the "Pin-Name" column.

Table 3. IA82527 Pin/Signal Descriptions

Signal	Pin			Description
	Name	PLCC	QFP	
a0	**a0**/ad0/icp	4	42	**a**ddress bits **7**–**0**. Input. Mode 3. When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel® architecture mode (Mode 3), these lines provide the 8-bit address bus input to the device.
a1	**a1**/ad1/cp	3	41	
a2	**a2**/ad2/csas	2	40	
a3	**a3**/ad3/ste	43	37	
a4	**a4**/ad4/mosi	42	36	
a5	**a5**/ad5	41	35	
a6	**a6**/ad6/sclk	40	34	
a7	**a7**/ad7	39	33	
ad0	a0/**ad0**/icp	4	42	**a**ddress/**d**ata bits **15**–**0**. Input/Output. Mode 1. When the IA82527 is configured to operate in the 16-bit multiplexed Intel® architecture mode (Mode 1), these lines provide the 16-bit address bus (input) and the 16-bit data bus (input/output) for the device.
ad1	a1/**ad1**/cp	3	41	
ad2	a2/**ad2**/csas	2	40	
ad3	a3/**ad3**/ste	43	37	
ad4	a4/**ad4**/mosi	42	36	
ad5	a5/**ad5**	41	35	
ad6	a6/**ad6**/sclk	40	34	
ad7	a7/**ad7**	39	33	
ad8	**ad8**/d0/p1.0	38	32	
ad9	**ad9**/d1/p1.1	37	31	
ad10	**ad10**/d2/p1.2	36	30	
ad11	**ad11**/d3/p1.3	35	29	
ad12	**ad12**/d4/p1.4	34	28	
ad13	**ad13**/d5/p1.5	33	27	
ad14	**ad14**/d6/p1.6	32	26	
ad15	**ad15**/d7/p1.7	31	25	
ale	**ale**/as	5	43	**a**ddress **l**atch **e**nable. Input. Active High. Mode 0 and Mode 1. When the IA82527 is configured to operate in either the 8-bit multiplexed Intel® architecture mode (Mode 0) or the 16-bit multiplexed Intel® architecture mode (Mode 1), this signal latches the address into the device during the address phase of the bus cycle.

continued . . .

Table 3. IA82527 Pin/Signal Descriptions, continued

Signal	Pin			Description
	Name	PLCC	QFP	
as	ale/**as**	5	43	**a**ddress **s**trobe. Input. Active High. Mode 2. When the IA82527 is configured to operate in either the 8-bit multiplexed non-Intel® architecture mode (Mode 2), this signal latches the address into the device during the address phase of the bus cycle. **NOTE**: If the IA82527 is configured to operate in Mode 3 (8-bit non-multiplexed non-Intel® architecture), this pin must be tied high.
clkout	—	27	21	**cl**oc**k out**. Output (push-pull). This output provides a programmable clock frequency. The frequency is set via the Clockout Register (1FH) and can range from the frequency of the **xtal** (crystal) input to xtal/*n*, where *n* can be an integer value from 2 through 15. This output allows the IA82527 to clock other devices such as the host CPU.
cp	a1/ad1/**cp**	3	41	**c**lock **p**hase. Input. Serial Interface Mode. When this input is a logic 0, data are sampled on the rising edge of **sclk**. When this input is a logic 1, data are sampled on the falling edge of **sclk**.
cs_n	—	8	2	**c**hip **s**elect. Input. Active Low (Modes 0–3); Selectable Active Level (Serial Interface Mode). When the IA82527 is configured to operate in one of the parallel interface modes (Modes 0–3) or the Serial Interface Mode, this input, during its active state, selects the device allowing CPU access. For Serial Interface Mode operation, the active state is selectable (i.e., either high or low) via the IA8257 **csas** pin.
csas	a2/ad2/**csas**	2	40	**c**hip **s**elect **a**ctive **s**tate. Input. Serial Interface Mode. When this input is a logic 0, the **cs_n** input is configured to function active low. When this input is a logic 1, the **cs_n** input is configured to function active high.
d0	ad8/**d0**/p1.0	38	32	**d**ata bits **7**–**0**. Input/Output. Mode 3. When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel® architecture mode (Mode 3), these lines provide the 8-bit data bus to the device.
d1	ad9/**d1**/p1.1	37	31	
d2	ad10/**d2**/p1.2	36	30	
d3	ad11/**d3**/p1.3	35	29	
d4	ad12/**d4**/p1.4	34	28	
d5	ad13/**d5**/p1.5	33	27	
d6	ad14/**d6**/p1.6	32	26	
d7	ad15/**d7**/p1.7	31	25	

continued . . .

Table 3. IA82527 Pin/Signal Descriptions, continued

Signal	Pin			Description
	Name	PLCC	QFP	
dsack0_n	—	9	3	**d**ata and **s**ize **ack**nowledge **0**. Output. Active Low (open drain with active pull-up). Mode 3 (asynchronous operation). When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel® architecture mode (Mode 3), this signal functions as follows: when the CPU reads from the IA82527, **dsack0_n** active low indicates that the data are valid; when the CPU writes to the IA82527, **dsack0_n** active low indicates that the data have been received.
e	rd_n/**e**	6	44	**e**nable. Input. Active High. Mode 3 (asynchronous). When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel® architecture mode (Mode 3), this signal functions as follows: when the CPU reads from or writes to the IA82527, **e** active high indicates that the address is valid.
icp	a0/ad0/**icp**	4	42	**i**dle **c**lock **p**olarity. Input. Serial Interface Mode. When this input is a logic 0, the polarity for the idle state of **sclk** is low. When this input is a logic 1, the polarity for the idle state of **sclk** is high.
int_n	**int_n**/ V_{CC}/2	24	18	**int**errupt. Output (open collector). Active Low. On the IA82527, two pins can provide the interrupt (**int_n**) output; however, depending on the setting of the MUX bit in the CPU Interface Register (02H), only one of the pins will serve as the source of **int_n** as follows: • PLCC Package: – When the MUX bit of the CPU Interface Register is 0, pin 24 functions as the **int_n** output and pin 11 functions as **p2.6**. – When the MUX bit of the CPU Interface Register is 1, pin 11 functions as the **int_n** output and pin 24 functions as **V_{cc}/2**. • QFP Package: – When the MUX bit of the CPU Interface Register is 0, pin 18 functions as the **int_n** output and pin 5 functions as **p2.6**. – When the MUX bit of the CPU Interface Register is 1, pin 5 functions as the **int_n** output and pin 18 functions as **V_{cc}/2**.
	int_n/p2.6	11	5	

continued . . .

Table 3. IA82527 Pin/Signal Descriptions, continued

Signal	Pin			Description
	Name	PLCC	QFP	
miso	ready/**miso**	28	22	**m**aster **i**n **s**lave **o**ut. Output (open drain). Serial Interface Mode. When the IA82527 is configured to operate with a serial interface, **miso** is the serial data output.
mode0	—	44	38	**modeN** (N = 1 or 0). Input. The logic levels at the mode0 and mode1 inputs determine the operating mode (i.e., interface type) of the IA82527 as follows: **mode1** **mode0** **Interface Type** 0 0 8-bit Multiplexed Intel® 0 1 16-bit Multiplexed Intel® 1 0 8-bit Multiplexed Non-Intel® 1 1 8-bit Non-Multiplexed Non-Intel® The **mode1** and **mode0** inputs are also used to establish the Serial Interface Mode as follows: when the IA82527 is reset, if • **mode1** = 0 • **mode0** = 0 • **rd_n** = 0 • **wr_n** = 0 the Serial Interface Mode will be selected. The **mode1** and **mode0** pins are internally connected to weak pull-downs. These pins will be pulled low during reset if unconnected. Following reset, these pins will float.
mode1	—	30	24	
mosi	a4/ad4/**mosi**	42	36	**m**aster **o**ut **s**lave **i**n. Input. Serial Interface Mode. When the IA82527 is configured to operate with a serial interface, **mosi** is the serial data input.

continued . . .

Table 3. IA82527 Pin/Signal Descriptions, continued

Signal	Pin			Description
	Name	PLCC	QFP	
p1.0	ad8/d0/**p1.0**	38	32	**p**ort **1**, bit **N** (N = 7–0). Input/Output (general-purpose). Mode 0, Mode 2, and Serial Interface Mode. Port 1 bits **p1.7**–**p1.0** can be individually programmed as inputs or outputs. Programming is accomplished by writing to the P1CONF Register (9FH). The 8 bits of the P1CONF Register, P1CONF7–P1CONF0, correspond directly to pins **p1.7**–**p1.0**. Writing a 0 to a bit in the P1CONF Register causes the corresponding pin to be configured as a high-impedance input. Writing a 1 to a bit in the P1CONF Register causes the corresponding pin to be configured as a push-pull output. All Port 1 pins have weak pull-ups until the port is configured by writing to the P1CONF Register. The default value of the P1CONF Register following a reset is 00H. Data are read from Port 1 via the P1IN Register (BFH). A logic 0 for any bit in this register means that a logic 0 was read from the corresponding pin; a logic 1 for any bit means that a logic 1 was read from the corresponding pin. The default value of the P1IN Register following a reset is FFH. Data are written to Port 1 via the P1OUT Register (DFH). Writing a logic 0 to any bit in this register means that a logic 0 is written to the corresponding pin; writing a logic 1 to any bit means that a logic 1 is written to the corresponding pin. The default value of the P1OUT Register following a reset is 00H.
p1.1	ad9/d1/**p1.1**	37	31	
p1.2	ad10/d2/**p1.2**	36	30	
p1.3	ad11/d3/**p1.3**	35	29	
p1.4	ad12/d4/**p1.4**	34	28	
p1.5	ad13/d5/**p1.5**	33	27	
p1.6	ad14/d6/**p1.6**	32	26	
p1.7	ad15/d7/**p1.7**	31	25	
p2.0	—	17	11	**p**ort **2**, bit **N** (N = 7–0). Input/Output. Port 2 bits **p2.7**–**p2.0**, can be individually programmed as inputs or outputs. Programming is accomplished by writing to the P2CONF Register (AFH). The 8 bits of the P2CONF Register, P2CONF7–P2CONF0, correspond directly to pins **p2.7**–**p2.0**. Writing a 0 to a bit in the P2CONF Register causes the corresponding pin to be configured as a high-impedance input. Writing a 1 to a bit in the P2CONF Register causes the corresponding pin to be configured as a push-pull output. All Port 2 pins have weak pull-ups until the port is configured by writing to the P2CONF Register. The default value of the P1CONF Register following a reset is 00H. Data are read from Port 2 via the P2IN Register (CFH). A logic 0 for any bit in this register means that a logic 0 was read from the corresponding pin; a logic 1 for any bit means that a logic 1 was read from the corresponding pin. The default value of the P2IN Register following a reset is FFH. Data are written to Port 2 via the P2OUT Register (EFH). Writing a logic 0 to any bit in this register means that a logic 0 is written to the corresponding pin; writing a logic 1 to any bit means that a logic 1 is written to the corresponding pin. The default value of the P2OUT Register following a reset is 00H.
p2.1	—	16	10	
p2.2	—	15	9	
p2.3	—	14	8	
p2.4	—	13	7	
p2.5	—	12	6	
p2.6	int_n/**p2.6**	11	5	
p2.7	wrh_n/**p2.7**	10	4	

continued . . .

Table 3. IA82527 Pin/Signal Descriptions, continued

Signal	Pin			Description
	Name	PLCC	QFP	
rd_n	**rd_n**/e	6	44	**rea**d. Input. Active Low. Mode 0 and Mode 1. When **rd_n** is asserted (low), it causes the IA82527 to drive the data from the location being read onto the data bus.
ready	**ready**/miso	28	22	**ready**. Output (open drain). Active High. Mode 0 and Mode 1. When ready is asserted (high), it signals the completion of a bus cycle. The ready output is provided to force system CPU wait states as required.
reset_n	—	29	23	**reset**. Input. Active Low. When the **reset_n** signal is asserted (low), the IA82527 is initialized. There are two reset situations: Cold Reset. This is a power-on reset: As V_{CC} is driven to a valid level (power on), the **reset_n** signal must be driven low for a minimum of 1 ms measured from a valid V_{CC} level. No falling edge on the reset_n pin is required during a cold reset. Warm Reset. For this reset, V_{CC} remains at a valid level (i.e., power is already on and remains on) while **reset_n** is driven low for a minimum of 1 ms.
r-w_n	wr_n/wrl_n/**r-w_n**	7	1	**r**ead-**w**rite. Input. Active High (read)-Active Low (write). Mode 3. When **r-w_n** is high, it signals a read cycle. When **r-w_n** is low, it signals a write cycle.
rx0	—	22	16	Receive (**rx**), lines **0** and **1**. Input. Pins **rx0** and **rx1** are the inputs to the IA82527 from the Controller Area Network (CAN) bus lines. These pins connect internally to the receiver input comparator. Serial data from the CAN bus can be received using both **rx0** and **rx1** or by using only **rx0** as follows: • When the CoBy Bit in the Bus Configuration Register (2FH) is a 0, **rx0** and **rx1** are connected to the input comparator. (**rx0** is connected to the non-inverting input and rx1 is connected to the inverting input.) A recessive level is read when **rx0** > **rx1**. A dominant level is read when **rx1** > **rx0**. • When the CoBy Bit in the Bus Configuration Register (2FH) is a 1, input comparison is disabled, and **rx0**, which is still connected to the non-inverting input of the comparator, is the CAN bus line input. For this configuration, the DcR0 bit of the Bus Configuration Register must be a 0. After a cold reset (power on), the default configuration is the use of both **rx0** and **rx1** for the CAN bus input.
rx1	—	21	15	
sclk	a6/ad6/**sclk**	40	34	**s**erial **clo**ck. Input. Serial Interface Mode. The **sclk** pin is the serial clock input to the IA82527 (slave device). The clock signal is provided by the master device.

continued . . .

Table 3. IA82527 Pin/Signal Descriptions, continued

Signal	Pin			Description
	Name	PLCC	QFP	
ste	a3/ad3/**ste**	43	37	**s**ynchronization **t**ransmission **e**nable. Input. Serial interface Mode. The logic level at the **ste** pin enables the transmission of the synchronization bytes through the IA82527 **miso** pin while the master device transmits the Address and Control Byte as follows: • When a logic 0 is placed on the **ste** pin, the synchronization bytes sent through the **miso** pin are 00H and 00H. • When a logic 1 is placed on the **ste** pin, the synchronization bytes sent through the **miso** pin are AAH and 55H. The IA82527 sends the synchronization bytes after the **cs_n** signal has been asserted (low).
tx0	—	26	20	Transmit (**tx**), lines **0** and **1**. Output (push-pull). Pins **tx0** and **tx1** are the outputs from the IA82527 to the Controller Area Network (CAN) bus lines. During a recessive bit, **tx0** is high and **tx1** is low. During a dominant bit, **tx0** is low and **tx1** is high.
tx1	—	25	19	
V_{CC}	—	1	39	Power (**V_{CC}**). This pin provides power for the IA82527 device. It must be connected to a +5V DC power source.
$V_{CC}/2$	int_n/ **$V_{CC}/2$**	24	18	Reference Voltage, ISO Physical Layer (**$V_{CC}/2$**). Output. The **$V_{CC}/2$** pin provides a reference voltage for the ISO low-speed physical layer: • 2.38V DC (minimum) to 2.60V DC (maximum) (V_{CC} = +5.00V; $I_{OUT} \leq 75$ µA) This pin only functions as **$V_{CC}/2$** when the MUX bit of the CPU Interface Register (02H) is 1.
V_{SS1}	—	23	17	Ground, Digital (**V_{SS1}**). This pin provides the digital ground (0V) for the IA82527. It must be connected to a V_{SS} board plane.
V_{SS2}	—	20	14	Ground, Analog (**V_{SS2}**). This pin provides the ground (0V) for the IA82527 analog comparator. It must be connected to a V_{SS} board plane.

continued . . .

Table 3. IA82527 Pin/Signal Descriptions, continued

Signal	Pin			Description
	Name	PLCC	QFP	
wr_n	**wr_n**/wrl_n/r-w_n	7	1	**wr**ite. Input. Active Low. Mode 0. When **wr_n** is asserted (low), it signals a write cycle.
wrh_n	**wrh_n**/p2.7	10	4	**wr**ite **h**igh byte. Input. Active Low. Mode 1. When **wrh_n** is asserted (low), it signals a write cycle for the high byte of data (bits 15–8).
wrl_n	wr_n/**wrl_n**/r-w_n	7	1	**wr**ite **l**ow byte. Input. Active Low. Mode 1. When **wrl_n** is asserted (low), it signals a write cycle for the low byte of data (bits 7–0).
xtal1	—	18	12	Crystal (**xtal**) **1**. Input. The **xtal1** pin is the input connection for an external crystal that drives the IA82527 internal oscillator. (When an external crystal is used, it is connected between this pin and the **xtal2** pin—see next table entry.) **NOTE:** If an external oscillator or clock source is used to drive the IA82527 instead of a crystal, the **xtal1** pin is the input for this clock source.
xtal2	—	19	13	Crystal (**xtal**) **2**. Output (push-pull). The **xtal2** pin is the output connection for an external crystal that drives the IA82527 internal oscillator. (When an external crystal is used, it is connected between this pin and the **xtal1** pin—see previous table entry.) **NOTE:** If an external oscillator or clock source is used to drive the IA82527 instead of a crystal, **xtal2** must be left unconnected (i.e., must be floated). Additionally, the **xtal2** output must not be used as a clock source for other system components.

3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA82527 Serial Communications Controller, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 4–6, respectively.

Additionally, the DC parameters of the ISO Physical Layer are provided in Table 7.

NOTE
The values provided in the following tables are preliminary.

Table 4. IA82527 Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65°C to +150°C
Case Temperature under Bias	−65°C to +120°C
Supply Voltage with Respect to Vss	−0.5V to +6.5V
Voltage on Pins other than Supply with Respect to Vss	−0.5V to +5.5V

Table 5. IA82527 Thermal Characteristics

Symbol	Characteristic	Value	Units
T_A	Ambient Temperature	User Determined	°C
P_{INT}	Device Internal Power Dissipation	$I_{DD} \times V_{DD}$	W
$P_{I/O}$	I/O Pin Power Dissipation	User Determined	W
P_D	Total Power Dissipation	$P_{INT} + P_{I/O}$	W
Θ_{Ja}	44-Pin PLCC Package	To Be Determined	°C/W
	44-Pin QFP Package	To Be Determined	
T_J	Average Junction Temperature	$T_A + (P_D \times \Theta_{Ja})$	°C

Table 6. IA82527 DC Parameters

Symbol	Parameter	Pin(s)	Minimum	Maximum	Units	Notes
V_{CC}	Supply Voltage	—	4.5	5.5	V	—
V_{IL}	Voltage, Input Low	ad7–ad0	−0.5	0.5	V	Mode 3
		p1.7–p1.0, p2.7–p2.0	—	0.3(V_{CC})		Not connected to a host CPU
		rx0	—	0.5		Comparator bypassed
			−0.5	0.8		All other pins
V_{IH}	Voltage, Input High	p1.7–p1.0, p2.7–p2.0	0.7(V_{CC})	—	V	Not connected to a host CPU
		reset_n	3.0	V_{CC} + 0.5		**reset_n** hysteresis = 200mV
		rx0	4.0	—		Comparator bypassed
			3.0	V_{CC} + 0.5		All other pins
V_{OL}	Voltage, Output Low	tx0, tx1			V	See Table 7
			—	0.45		All other pins; I_{OL} = 1.6 mA
V_{OH}	Voltage, Output High	clkout	0.8(V_{CC})	—	V	I_{OH} = −80 µA
		tx0, tx1				See Table 7
			V_{CC} − 0.8	—		All other pins; I_{OH} = −200 µA
I_{LEAK}	Input Leakage Current		—	±10	µA	V_{SS} < V_{IN} < V_{CC}
C_{IN}	Pin Capacitance		—	10	pF	$f_{CRYSTAL}$ = 1 KHz
I_{CC}	Supply Current		—	50	mA	$f_{CRYSTAL}$ = 16 KHz; all pins are driven to V_{SS} or V_{CC}.
$I_{SLEEP-E}$	Sleep Current		—	700	µA	**V_{CC}/2** enabled; no load.
$I_{SLEEP-D}$	Sleep Current		—	100		**V_{CC}/2** disabled.
I_{PD}	Power-Down Current		—	25		**xtal1** clocked; all pins driven to V_{SS} or V_{CC}.
All ratings listed are for the temperature range T_A = −40°C to +125°C (V_{CC} = 5V ± 10%).						

Table 7. IA82527 ISO Physical Layer DC Parameters

Signal	Parameter	Minimum	Maximum	Units	Notes
rx0 & rx1; tx0 & tx1	Input Voltage	−0.5	V_{CC} + 0.5	V	—
	Common Mode Range	V_{ss} + 1.0	V_{CC} − 1.0	V	—
	Differential Input Threshold	±100	—	mV	—
	Delay 1: receive comparator input delay + **tx0**/**tx1** output delay	—	60	ns	Load on **tx0**/**tx1** = 100 pF; **rx0**/**rx1** differential = +100 mV to −100 mV
	Delay 2: **rx0** pin delay (comparator bypassed) + **tx0**/**tx1** output delay	—	50	ns	Load on **tx0**/**tx1** = 100 pF
	Source Current on **tx0**, **tx1**	—	−10	mA	V_{OUT} = V_{CC} − 1.0 V
	Sink Current on **tx0**, **tx1**	—	10	mA	V_{OUT} = 1.0 V
	Input Hysteresis for **rx0**/**rx1**	—	0	V	—
V_{CC}/2	Reference Voltage	2.38	2.62	V	I_{OUT} ≤ 75 µA; V_{CC} = 5.0 V
All ratings listed are for the temperature range T_A = −40°C to +125°C (V_{CC} = 5V ± 10%).					

4. Functional Description

4.1 Hardware Architecture

A block diagram of the IA82527 CAN Serial Communications Controller is shown in Figure 3. The primary architectural features of the device are as follows:

- Controller Area Network (CAN) Controller
- RAM
- CPU Interface
- I/O Ports
- Programmable Clock Output

These features are briefly described in the following subsections.

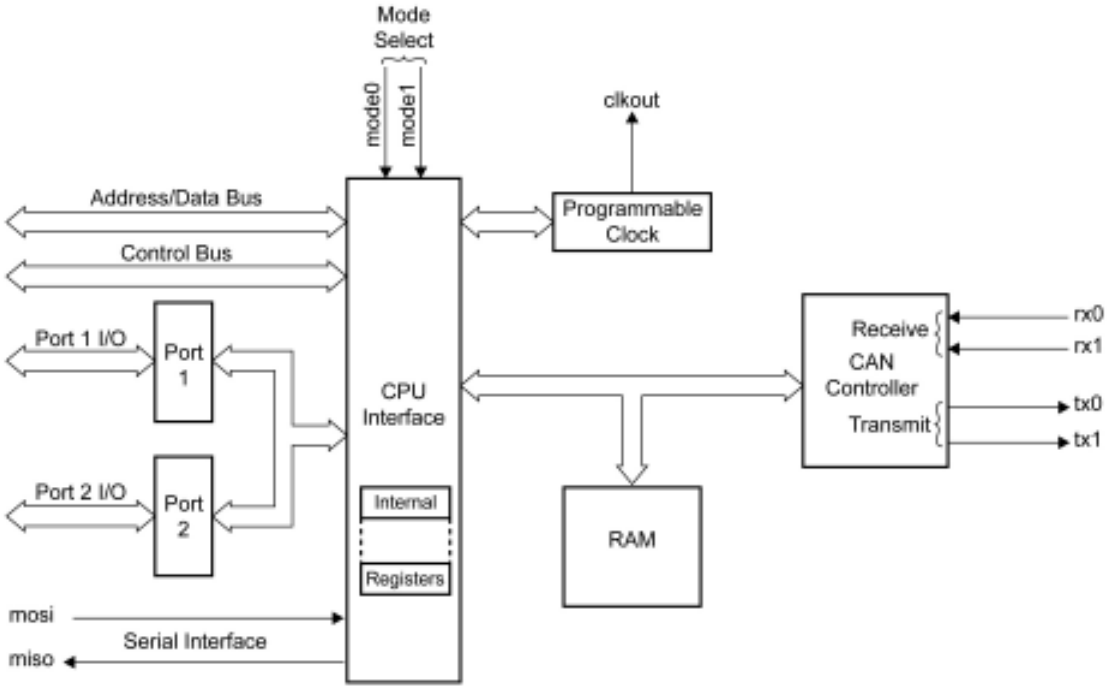

Figure 3. IA82527 Functional Block Diagram

4.1.1 CAN Controller

The CAN Controller block of the IA82527 supports the interface to the CAN Bus via the **rx0, rx1**, **tx0**, and **tx1** lines. The CAN Controller manages the transceiver logic, error management logic, and the message objects, controlling the data stream between the RAM (parallel data) and the CAN Bus (serial data).

4.1.2 RAM

The RAM block of the IA82527 provides the interface buffer between the system CPU and the CAN Bus. The IA82527 RAM provides storage for 15 message objects of 8-byte data length. The RAM is an interleaved-access memory, which means that access to the RAM is timeshared between the CPU Interface Logic and the CAN Bus.

4.1.3 CPU Interface

The IA82527 is capable of interfacing to many commonly used microcontrollers. There are four parallel interface options and a serial interface option.

Different interface options, or modes, are selected using interface mode pins, **mode1** and **mode0**. The parallel interface modes that can be selected are as follows:

- 8-bit Intel® multiplexed address and data buses
- 16-bit Intel® multiplexed address and data buses
- 8-bit non- Intel® multiplexed address and data buses
- 8-bit non-multiplexed address and data buses

The serial interface mode is fully compatible with the Motorola® SPI protocol and will interface to most commonly used serial interfaces. The serial interface is implemented in slave mode only, and responds to the master using the specially designed serial interface protocol. The serial interface mode interconnection scheme is shown in Figure 4.

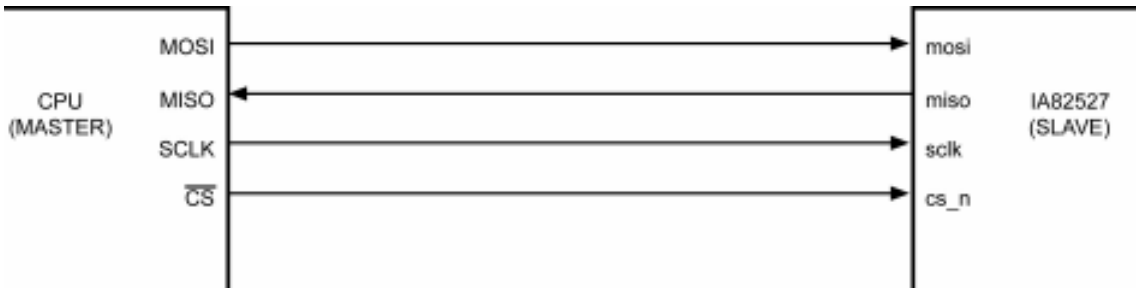

Figure 4. mosi/miso Connection

4.1.4 I/O Ports

The IA82527 provides two 8-bit low-speed input/output (I/O) ports. Depending on the CPU interface mode selected, at least 7 and up to 16 I/O lines are available. Each I/O line is individually programmable to function either as an input or an output.

4.1.5 Programmable Clock Output

Using an oscillator, clock divider register, and a driver circuit, the IA82527 provides a programmable clock output. The output frequency range available is from the external crystal frequency to that frequency divided by 15. The clock output allows the IA82527 to drive other devices such as the host CPU.

4.2 Address Map

The IA82527 includes 256 8-bit locations that provide device configuration registers and message storage. The address map is shown in Figure 5.

4.3 CAN Message Objects

Each CAN message object has a unique identifier and can be configured as either transmit or receive, except for the last message object. The last message object is a receive-only buffer with a special mask design to allow select groups of different message identifiers to be received. Each message object contains control and status bits.

All message objects have separate transmit and receive interrupts and status bits that allow the host CPU to determine when a message frame has been sent or received. The IA82527 implements a global masking feature that allows the user to globally mask any identifier bits of the incoming message. This mask is programmable, which permits application-specific message identification.

The Message Object Structure is shown in Figure 6.

Address	Register/Message
00H	Control Register
01H	Status Register
02H	CPU Interface Register
03H	Reserved
04–05H	High-Speed Read Register
06–07H	Global Mask – Standard
08–0BH	Global Mask – Extended
0V-0FH	Message 15 Mask
10–1EH	**Message 1**
1FH	CLKOUT Register
20–2EH	**Message 2**
2FH	Bus Configuration Register
30–3EH	**Message 3**
3FH	Bit Timing Register 0
40–4EH	**Message 4**
4FH	Bit Timing Register 1
50–5EH	**Message 5**
5FH	Interrupt Register
60–6EH	**Message 6**
6FH	Reserved
70H–7EH	**Message 7**
7FH	Reserved
80–8EH	**Message 8**
8FH	Reserved
90–9EH	**Message 9**
9FH	P1CONF Register
A0–AEH	**Message 10**
AFH	P2CONF Register
B0–BEH	**Message 11**
BFH	P1IN Register
C0–CEH	**Message 12**
CFH	P2IN Register
D0–DEH	**Message 13**
DFH	P1OUT Register
E0–EEH	**Message 14**
EFH	P2OUT Register
F0–FEH	**Message 15**
FFH	Serial Reset Address Register

Figure 5. IA82527 Address Map

Offset (Base Address +n)	Message Component
+0	Control Register 0
+1	Control Register 1
+2	Arbitration Register 0
+3	Arbitration Register 1
+4	Arbitration Register 2
+5	Arbitration Register 3
+6	Message Configuration Register
+7	Data Byte 0
+8	Data Byte 1
+9	Data Byte 2
+10	Data Byte 3
+11	Data Byte 4
+12	Data Byte 5
+13	Data Byte 6
+14	Data Byte 7

Figure 6. IA82527 Message Object Structure

5. AC Characteristics

The AC characteristics of the IA82527 are provided in the figures and tables of this chapter.

The IA82527 can be configured to operate in the following parallel and serial CPU interface modes:

- Mode 0: 8-Bit Multiplexed Intel® Architecture
- Mode 1: 16-Bit Multiplexed Intel® Architecture
- Mode 2: 8-Bit Multiplexed Non-Intel® Architecture
- Mode 3: 8-Bit Non-Multiplexed Non-Intel® Architecture
- Serial Interface Mode

The AC characteristics of these modes in operation of are provided as follows:

- Mode 0 and Mode 1 General Bus Timing (Table 8/Figure 7)
- Mode 0 and Mode 1 **ready** Timing for Read Cycle (Table 8/Figure 8)
- Mode 0 and Mode 1 **ready** Timing for Write Cycle with No Write Pending (Table 8/Figure 9)
- Mode 0 & Mode 1 **ready** Timing for Write Cycle with Write Pending (Table 8/Figure 10)
- Mode 2 General Bus Timing (Table 9/Figure 11)
- Mode 3, Asynchronous Operation, Read Cycle (Table 10/Figure 12)
- Mode 3, Asynchronous Operation, Write Cycle (Table 10/Figure 13)
- Mode 3, Synchronous Operation, Read Cycle (Table 11/Figure 14)
- Mode 3, Synchronous Operation, Write Cycle (Table 11/Figure 15)
- Serial Interface Mode, **icp** = 0 and **cp** = 0 (Table 12/Figure 16)
- Serial Interface Mode, **icp** = 1 and **cp** = 1 (Table 12/Figure 17)

NOTE
The values provided in the following tables and figures are preliminary.

Table 8. Mode 0 and Mode 1 General Bus and ready Timing

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVLL}	Address Valid to **ale** Low	7.5 ns	—
t_{LLAX}	Address Hold after **ale** Low	10 ns	—
t_{LHLL}	**ale** High Time	30 ns	—
t_{LLRL}	**ale** Low to **rd_n** Low	20 ns	—
t_{CLLL}	**cs_n** Low to **ale** Low	10 ns	—
t_{QVWH}	Data Setup to **wr_n** or **wrh_n** High	27 ns	—
t_{WHQX}	Input Data Hold after **wr_n** or **wrh_n** High	10 ns	—
t_{WLWH}	**wr_n** or **wrh_n** Pulse Width	30 ns	—
t_{WHLH}	**wr_n** or **wrh_n** High to Next ale High	8 ns	—
t_{WHCH}	**wr_n** or **wrh_n** High to **cs_n** High	0 ns	—
t_{RLRH}	**rd_n** Pulse Width This time is long enough to initiate a double read cycle by loading the High Speed Registers (04H, 05H), but is too short to read from 04H and 05H (see t_{RLDV}).	40 ns	—
t_{RLDV}	**rd_n** Low to Data Valid (Only for Registers 02H, 04H, 05H)	0 ns	55 ns
t_{RLDV1}	**rd_n** Low Data to Data Valid (for all Registers except 02H, 04H, 05H) for Read Cycle without a Previous Write	—	1.5 t_{MCLK} + 100 ns
t_{RLDV1}	**rd_n** Low Data to Data Valid (for all Registers except 02H, 04H, 05H) for Read Cycle with a Previous Write	—	3.5 t_{MCLK} + 100 ns
t_{RHDZ}	Data Float after **rd_n** High	0 ns	45 ns
t_{CLYV}	**cs_n** Low to **ready** Setup (Load Capacitance on the ready Output = 50 pF, V_{OL} = 1.0 V)	—	32 ns
	cs_n Low to **ready** Setup (Load Capacitance on the ready Output = 50 pF, V_{OL} = 0.45 V)	—	40 ns
t_{WLYZ}	**wr_n** or **wrh_n** Low to **ready** Float for a Write Cycle if No Previous Write is Pending	—	145 ns

continued . . .

Table 8. Mode 0 & Mode 1 General Bus and ready **Timing,** continued

Symbol	Parameter	Minimum	Maximum
t_{WHYZ}	End of Last Write to **ready** Float for a Write Cycle if a Previous Write Cycle is Active	—	2 t_{MCLK} + 100 ns
t_{RLYZ}	**rd_n** Low to **ready** Float (for all registers except 02H, 04H, 05H) for Read Cycle without a Previous Write	—	2 t_{MCLK} + 100 ns
t_{RLYZ}	**rd_n** Low to **ready** Float (for all registers except 02H, 04H, 05H) for Read Cycle with a Previous Write	—	4 t_{MCLK} + 100 ns
t_{WHDV}	**wr_n** High to Output Data Valid on Port 1 or Port 2	t_{MCLK}	2 t_{MCLK} + 500 ns
t_{COPO}	**clkout** Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	$(CD_V + 1) \cdot t_{OSC}$	
t_{CHCL}	**clkout** High Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	$(CD_V + 1) \cdot ½\ t_{OSC} - 10$	$(CD_V + 1) \cdot ½\ t_{OSC} - 15$

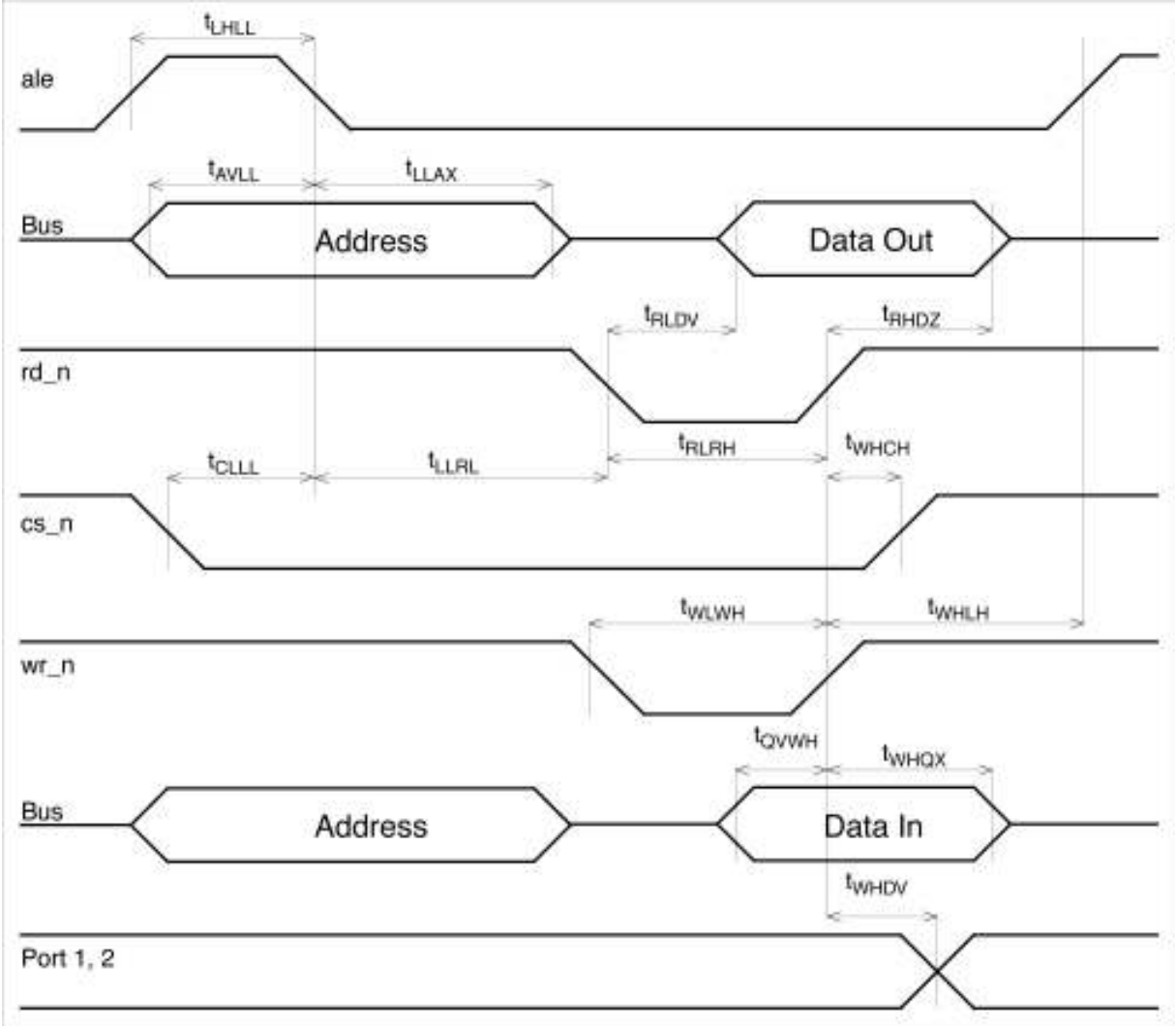

Figure 7. Mode 0 and Mode 1 General Bus Timing

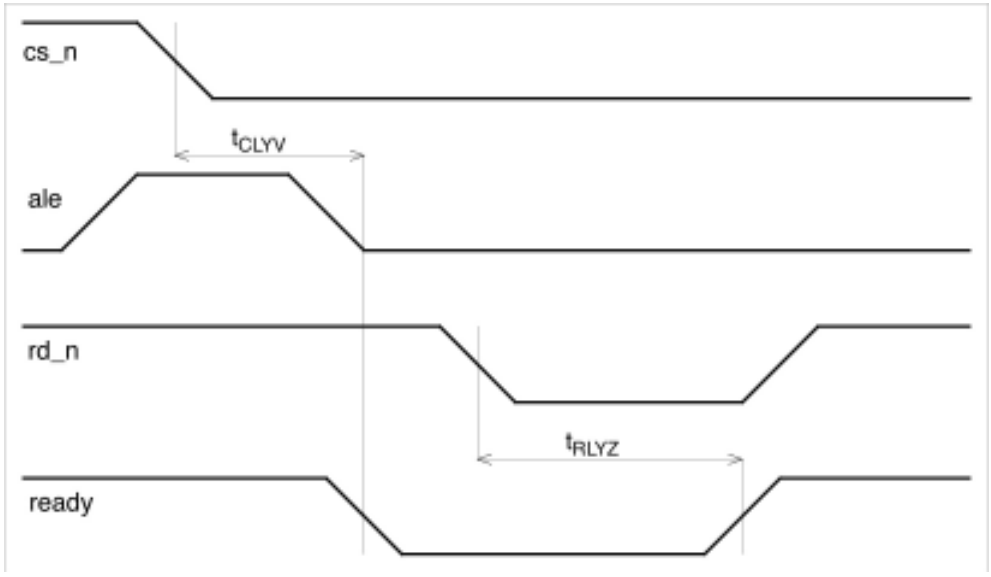

Figure 8. Mode 0 and Mode 1 ready **Timing for Read Cycle**

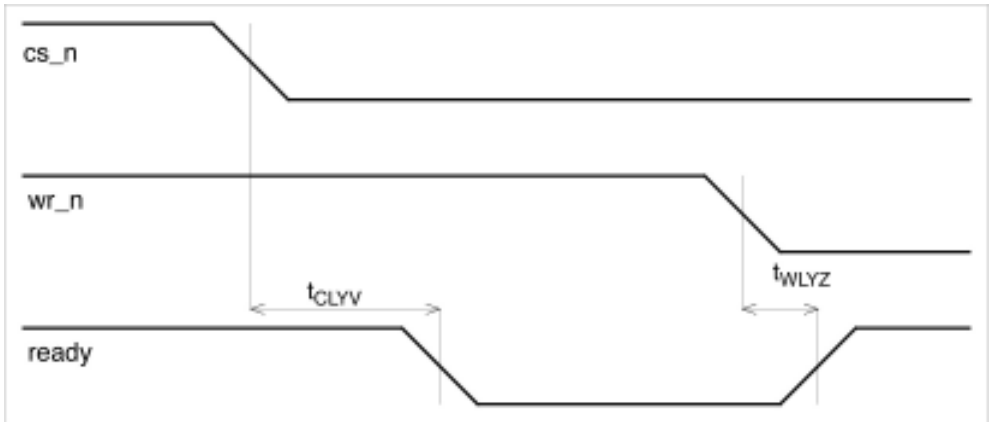

Figure 9. Mode 0 and Mode 1 ready **Timing for Write Cycle with No Write Pending**

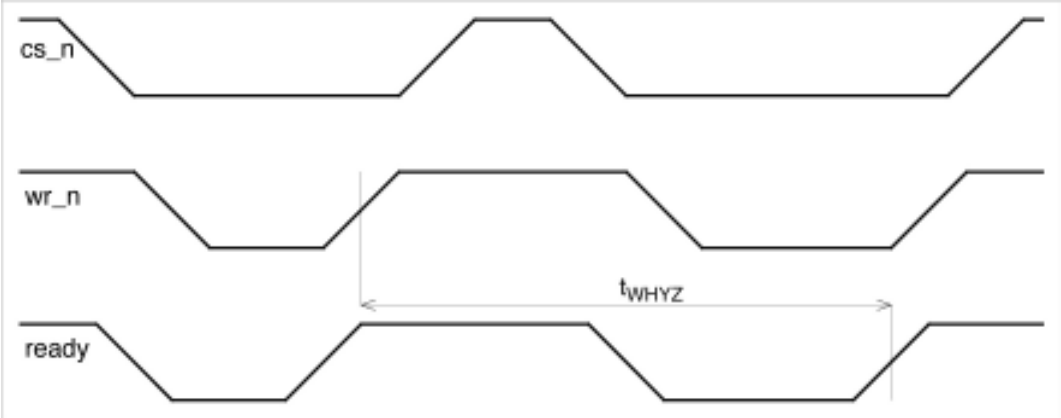

Figure 10. Mode 0 & Mode 1 ready **Timing for Write Cycle with Write Active**

Table 9. Mode 2 General Bus Timing

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVSL}	Address Valid to **as** Low	7.5 ns	
t_{SLAX}	Address Hold after **as** Low	10 ns	
t_{ELDZ}	Data Float after **e** Low	0 ns	45 ns
t_{EHDV}	**e** High to Data Valid for Registers 02H, 04H, 05H	0 ns	45 ns
	e High to Data Valid (all Registers except for 02H, 04H, 05H) for Read Cycle without a Previous Write	—	1.5 t_{mclk} + 100 ns
	e High to Data Valid (all Registers except for 02H, 04H, 05H) for Read Cycle with a Previous Write	—	3.5 t_{mclk} + 100 ns
t_{QVEL}	Data Setup to **e** Low	30 ns	—
t_{ELQX}	Input Data Hold after **e** Low	20 ns	—
t_{ELDV}	**e** Low to Output Data Valid on Port 1/2	t_{mclk}	2 t_{mclk} + 500 ns
t_{EHEL}	**e** High Time	45 ns	
t_{SHSL}	**as** High Time	30 ns	—
t_{RSEH}	Setup Time of **r-w_n** to **e** High	30 ns	—
t_{SLEH}	**as** Low to **e** High	20 ns	—
t_{CLSL}	**cs_n** Low to **as** Low	20 ns	—
t_{ELCH}	**e** Low to **cs_n** High	0 ns	—
t_{COPD}	**clkout** Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	$(CD_V + 1) \cdot t_{osc}$	
t_{CHCL}	**clkout** High Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	$(CD_V + 1) \cdot ½\ t_{osc} - 10$	$(CD_V + 1) \cdot ½\ t_{osc} - 15$

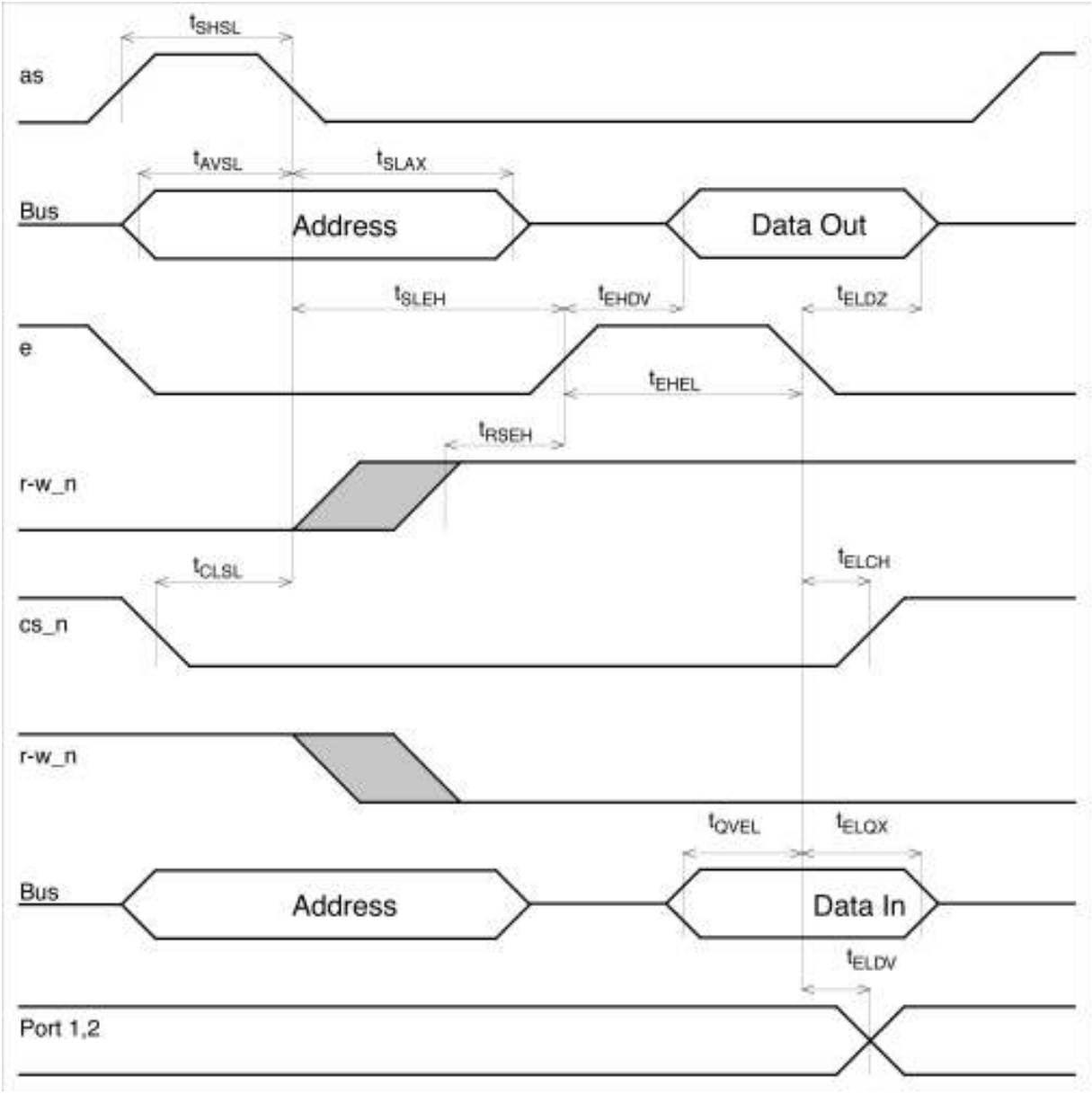

Figure 11. Mode 2 General Bus Timing

Table 10. Mode 3 Asynchronous Operation Timing

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVCL}	Address or **r-w_n** Valid to **cs_n** Low Setup	3 ns	—
t_{CLDV}	**cs_n** Low to Data Valid (for High-Speed Registers 02H, 04H, and 05H)	0 ns	55 ns
	cs_n Low to Data Valid (for Low-Speed Registers) Read Cycle without Previous Write	0 ns	1.5 t_{mclk} + 100 ns
	cs_n Low to Data Valid (for Low-Speed Registers) Read Cycle with Previous Write	0 ns	3.5 t_{mclk} + 100 ns
t_{KLDV}	**dsack0_n** Low to Output Data Valid (for High-Speed Read Registers)	—	23 ns
	dsack0_n Low to Output Data Valid (for Low-Speed Read Registers)	< 0 ns	—
t_{CHDV}	Input Data Hold after **cs_n** High	15 ns	—
t_{CHDH}	Output Data Hold after **cs_n** High	0 ns	—
t_{CHDZ}	**cs_n** High to Output Data Float	—	35 ns
t_{CHKH_1}	**cs_n** High to **dsack0_n** = 2.4V (An on-chip pull-up will drive **dsack0_n** to approximately 2.4V; an external pull-up is required to drive this signal to a higher voltage.)	0 ns	55 ns
t_{CHKH_2}	**cs_n** High to **dsack0_n** = 2.8V	—	150 ns
t_{CHKZ}	**cs_n** High to **dsack0_n** Float	0 ns	100 ns
t_{CHCL}	**cs_n** Width between Successive Cycles	25 ns	—
t_{CHAI}	**cs_n** High to Address Invalid	7 ns	—
t_{CLCH}	**cs_n** Width Low	65 ns	—
t_{DVCH}	CPU Write Data Valid to **cs_n** High	20 ns	—

continued . . .

Table 10. Mode 3 Asynchronous Operation Timing, continued

Symbol	Parameter	Minimum	Maximum
t_{CLKL}	**cs_n** Low to **dsack0_n** Low (for High- and Low-Speed Registers) Write Cycle without Previous Write	0 ns	67 ns
t_{CHKL}	End of Previous Write (**cs_n** High) to **dsack0_n** Low for a Write Cycle with a Previous Write	0 ns	2 t_{mclk} + 145 ns
t_{COPD}	**clkout** Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	(CD_V + 1) * t_{osc}	
t_{CHCL}	**clkout** High Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	(CD_V + 1) * ½ t_{osc} – 10	(CD_V + 1) * ½ t_{osc} – 15

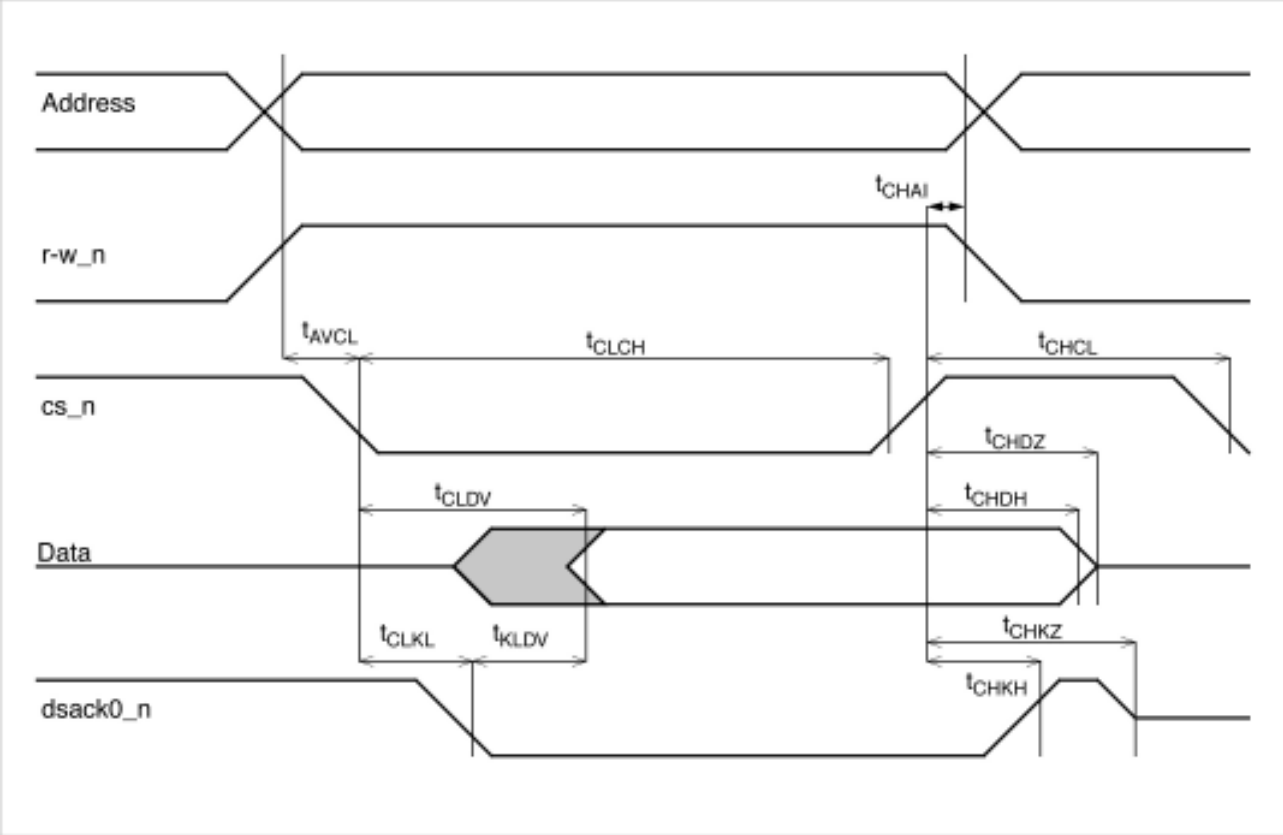

Figure 12. Mode 3, Asynchronous Operation, Read Cycle

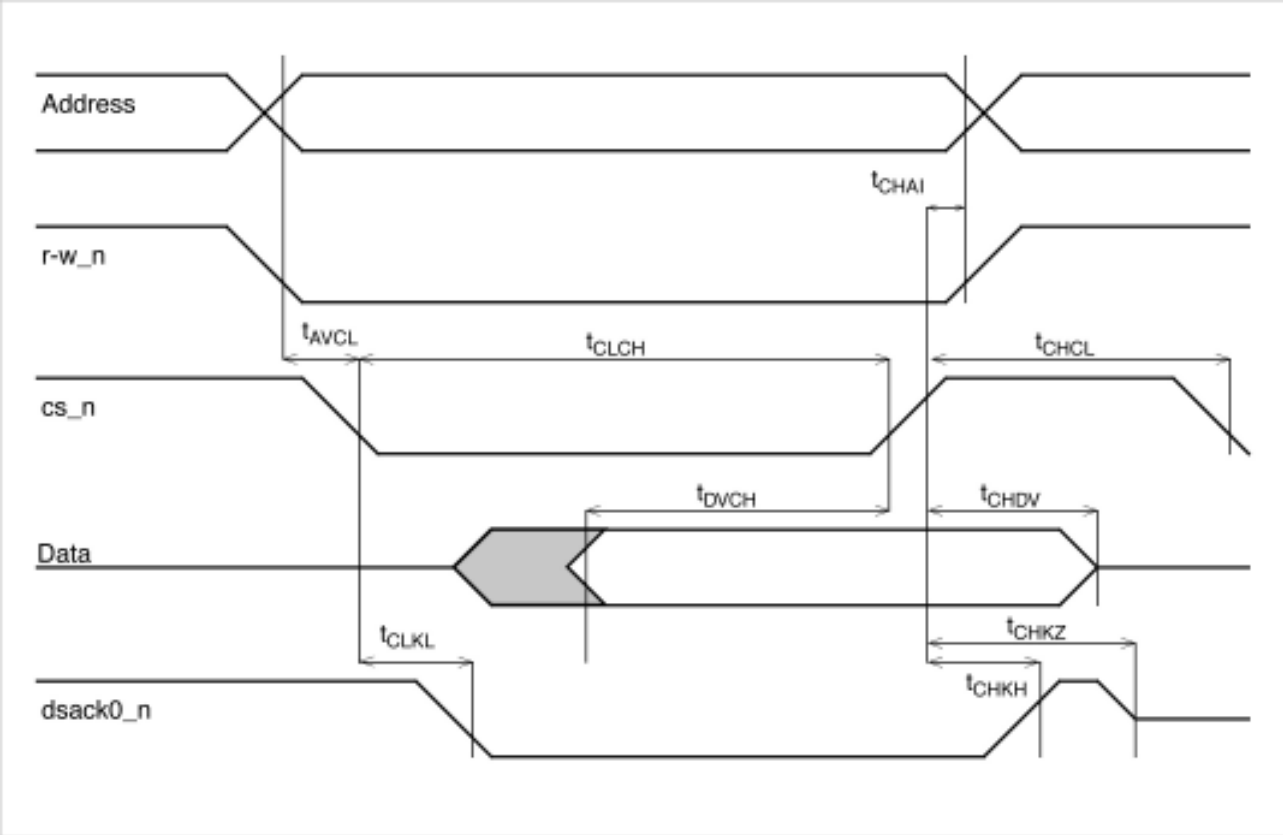

Figure 13. Mode 3, Asynchronous Operation, Write Cycle

Table 11. Mode 3 Synchronous Operation Timing

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{EHDV}	**e** High to Data Valid (for High-Speed Registers 02H, 04H, and 5H)	—	55 ns
	e High to Data Valid (for Low-Speed Registers) Read Cycle without Previous Write	—	1.5 t_{mclk} + 100 ns
	e High to Data Valid (for Low-Speed Registers) Read Cycle with Previous Write	—	3.5 t_{mclk} + 100 ns
t_{ELDH}	Data Hold after **e** Low for a Read Cycle	5 ns	—
t_{ELDZ}	Data Float after **e** Low	—	35 ns
t_{ELDV}	Data Hold after **e** Low for a Write Cycle	15 ns	—
t_{AVEH}	Address and **r-w_n** to e Setup	25 ns	—
t_{ELAV}	Address and **r-w_n** Valid after e Falls	15 ns	—
t_{CVEH}	**cs_n** Valid to **e** High	0 ns	—
t_{ELCV}	**cs_n** Valid after **e** Low	0 ns	—
t_{DVEL}	Data Setup to e Low	55 ns	—
t_{EHEL}	**e** Active Width	100 ns	—
t_{AVAV}	Start of a Write Cycle after a Previous Write Access	2 t_{mclk}	—
t_{AVCL}	Address or **r-w_n** to **cs_n** Low Setup	3 ns	—
t_{CHAI}	**cs_n** High Address Invalid	7 ns	—
t_{COPD}	**clkout** Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	(CD_V + 1) * t_{osc}	
t_{CHCL}	**clkout** High Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	(CD_V + 1) * ½ t_{osc} – 10	(CD_V + 1) * ½ t_{osc} + 15

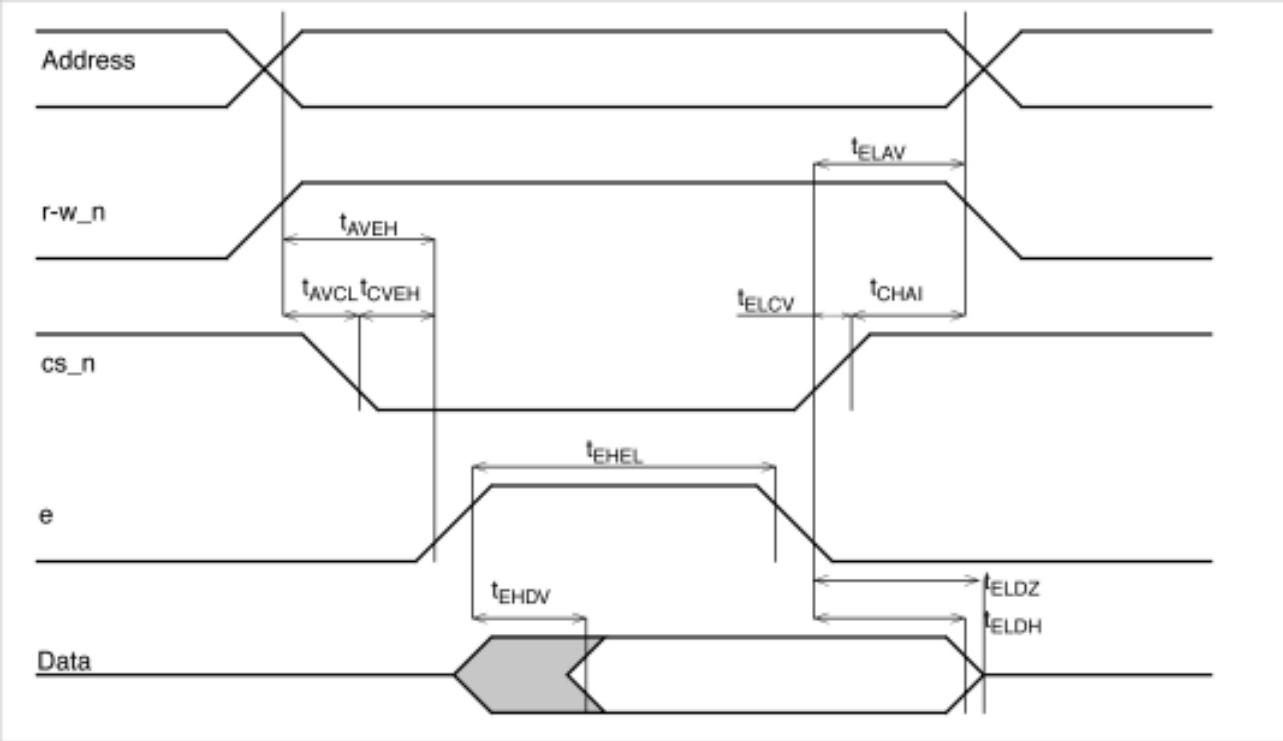

Figure 14. Mode 3, Synchronous Operation, Read Cycle Timing

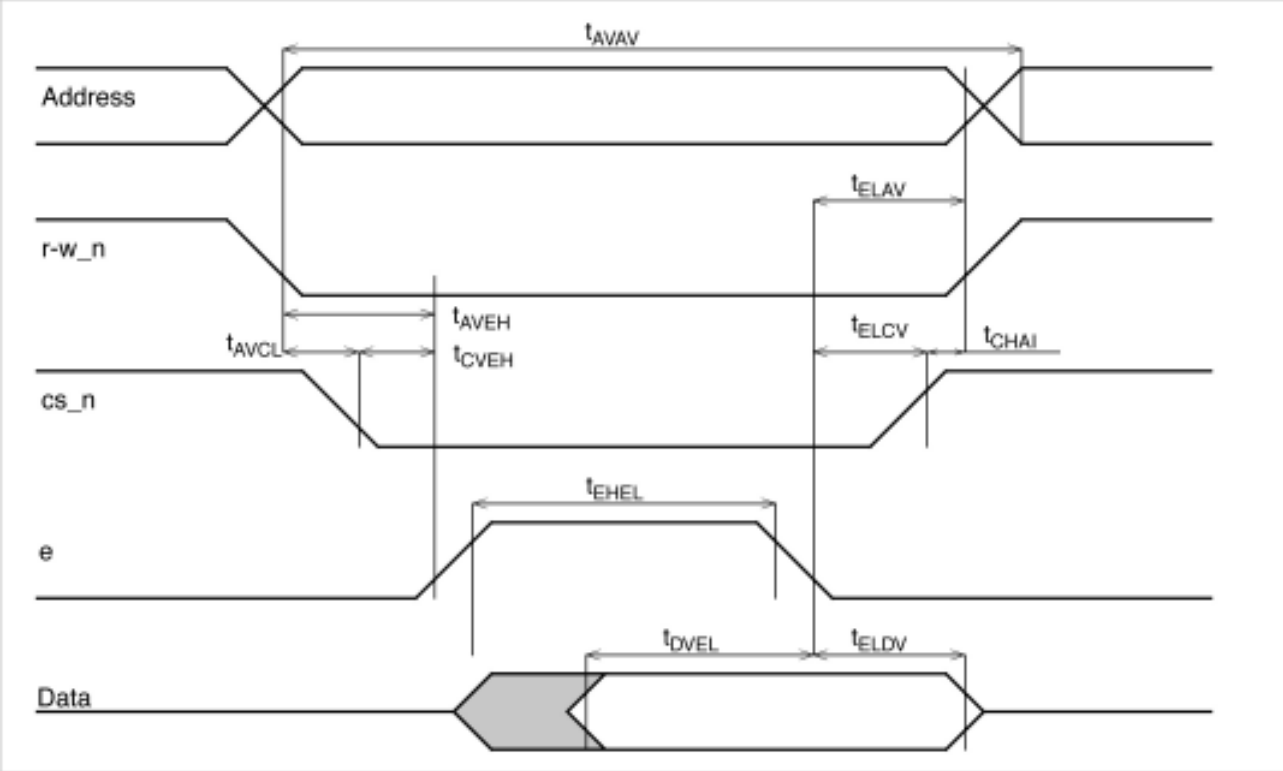

Figure 15. Mode 3, Synchronous Operation, Write Cycle Timing

Table 12. Serial Interface Mode Timing

Symbol	Parameter	Minimum	Maximum
sclk	Serial Port Interface Clock	0.5 MHz	8 MHz
t_{CYC}	1/**sclk**	125 ns	2000 ns
t_{SKHI}	Minimum Clock High Time	84 ns	—
t_{SKLO}	Minimum Clock Low Time	84 ns	—
t_{LEAD}	Enable Lead Time	70 ns	—
t_{LAG}	Enable Lag Time	109 ns	—
t_{ACC}	Access Time	—	50 ns
t_{PDO}	Maximum Data Out Delay Time	—	59 ns
t_{HO}	Minimum Data Out Hold Time	0 ns	—
t_{DIS}	Maximum Data Out Disable Time		665 ns
t_{SETUP}	Minimum Data Setup Time	35 ns	—
t_{HOLD}	Minimum Data Hold Time	84 ns	—
t_{RISE}	Maximum Time for Input to go from V_{OL} to V_{OH}	—	100 ns
t_{FALL}	Maximum Time for input to go from V_{OH} to V_{OL}	—	100 ns
t_{CS}	Minimum Time between Consecutive **cs_n** Assertions	670 ns	—
t_{COPD}	**clkout** Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	$(CD_V + 1) * t_{osc}$	
t_{CHCL}	**clkout** High Period (CD_V is the value loaded in the CLKOUT Register representing the **clkout** divisor.)	$(CD_V + 1) * ½ t_{osc} – 10$	$(CD_V + 1) * ½ t_{osc} + 15$

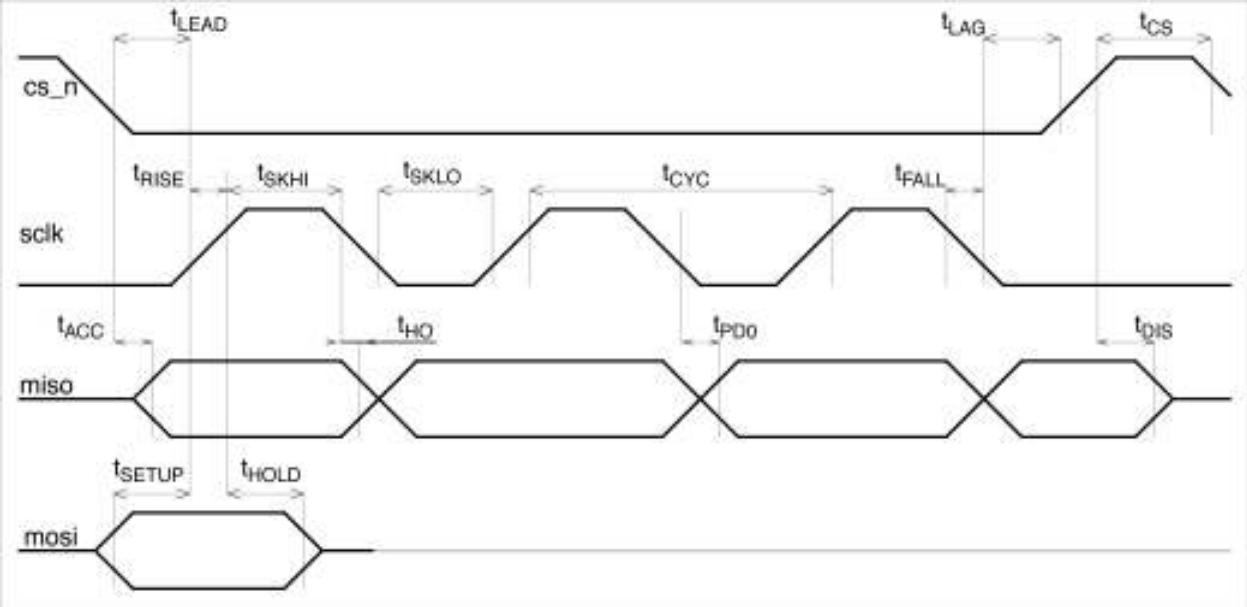

Figure 16. Serial Interface Mode, icp **= 0 and** cp **= 0**

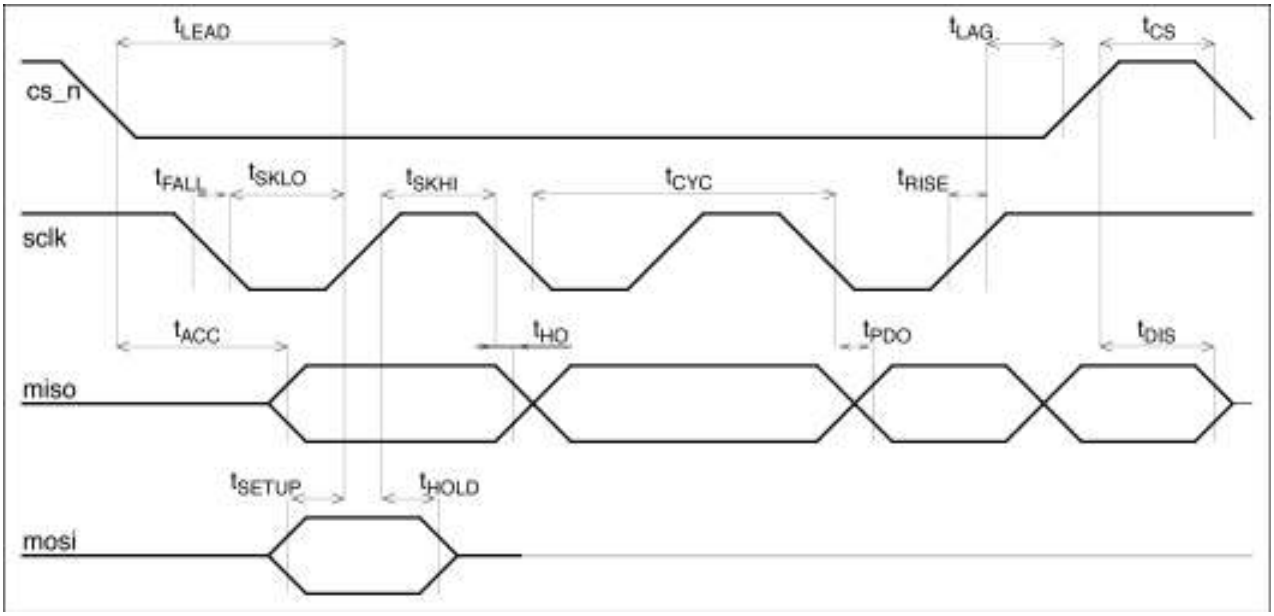

Figure 17. Serial Interface Mode, icp **= 1 and** cp **= 1**

6. Physical Dimensions

For the Innovasic Semiconductor IA82527 Serial Communications Interface, the physical dimensions for the available packages are provided in the following figures:

- 44-Pin PLCC Package: Figure 18
- 44-Pin QFP Package: Figure 19

A table specifying dimensions accompanies each figure (Tables 13 and 14).

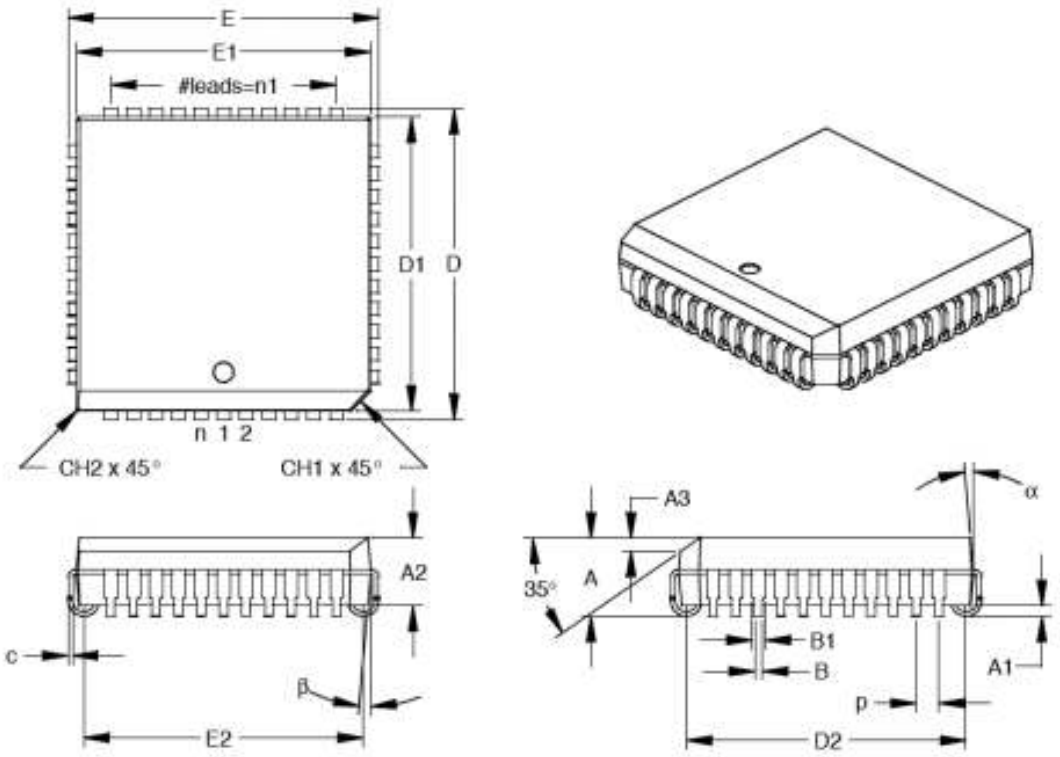

Figure 18. 44-Pin PLCC Physical Dimensions

Table 13. 44-Pin PLCC Physical Dimensions

Dimension		Minimum	Nominal	Maximum	Units
Number of Pins	n	—	44	—	—
Number of Pins per Side	n1	—	11	—	—
Pitch	p	—	0.0500	—	inches
Overall Height	A	0.1650	—	0.1800	
Molded Package Thickness	A2	0.1450	—	0.1600	
Standoff	A1	0.0200	—	—	
Overall Width	E	0.6850	—	0.6950	
Overall Length	D	0.6850	—	0.6950	
Molded Package Width	E1	0.6500	—	0.6560	
Molded Package Length	D1	0.6500	—	0.6560	
Lead Thickness	c	0.0077	—	0.1160	
Lead Width	B	0.0130	0.0170	0.0210	
Pin 1 Corner Chamfer	CH	0.0420	—	0.0560	
Mold Draft Angle Top	α	—	7.00	—	degrees
Mold Draft Angle Bottom	β	—	7.00	—	

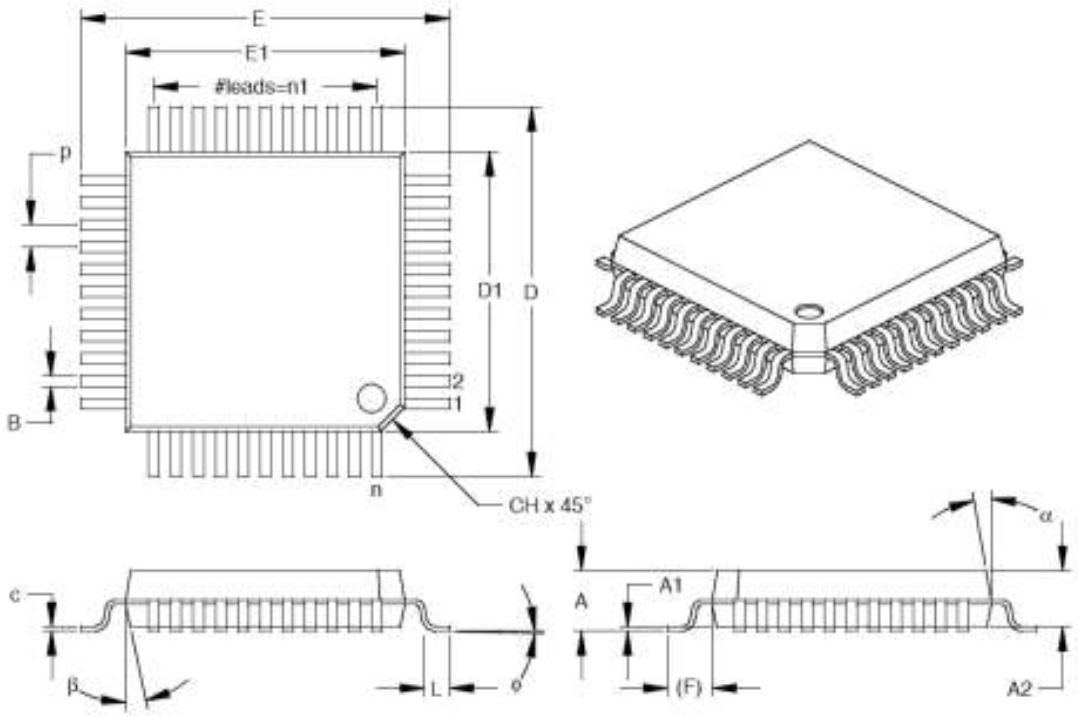

Figure 19. 44-Pin QFP Physical Dimensions

Table 14. 44-Pin QFP Physical Dimensions

Dimensions		Minimum	Nominal	Maximum	Units
Number of Pins	n	—	44	—	—
Number of Pins per Side	n1	—	11	—	—
Pitch	p	—	0.031	—	inches
Overall Height	A	—	—	0.096	
Molded Package Thickness	A2	—	0.079	—	
Standoff	A1	—	0.010	—	
Foot Length	L	0.029	0.035	0.041	
Footprint (Reference)	(F)	—	0.063	—	
Overall Width	E	0.510	0.520	0.530	
Overall Length	D	0.510	0.520	0.530	
Molded Package Width	E1	0.390	0.394	0.398	
Molded Package Length	D1	0.390	0.394	0.398	
Lead Thickness	c	0.005	0.007	0.009	
Lead Width	B	0.012	0.015	0.018	
Pin 1 Corner Chamfer	CH	—	0.030	—	
Mold Draft Angle Top	α	5.00	—	16.00	degrees
Mold Draft Angle Bottom	β	5.00	—	16.00	
Foot Angle	ϕ	0.00	—	10.00	

7. Ordering Information

Ordering information for the Innovasic IA82527 Serial Communications Controller is provided in Table 15.

Table 15. IA82527 Ordering Information

Innovasic Part Number	Intel® Part Number	Package Status	Package Type	Temperature Grades
IA82527-PLC44A	AS/AN82527F8	Standard	44-Pin Plastic Leaded Chip Carrier (PLCC)	Automotive
IA82527-PTQ44A	AS/AN82527F8	Standard	44-Pin Quad Flat Package (QFP)	Automotive
IA82527-PLC44A-R	AS/AN82527F8	RoHS	44-Pin Plastic Leaded Chip Carrier (PLCC)	Automotive
IA82527-PTQ44A-R	AS/AN82527F8	RoHS	44-Pin Quad Flat Package (QFP)	Automotive

Other packages and temperature grades may be available for an additional cost, longer lead time, or both.

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