



GENERAL DESCRIPTION

The AK4702 offers the ideal features for digital set-top-box systems. Using AKM's multi-bit architecture for its modulator, the AK4702 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4702 integrates a combination of SCF and CTF filters, removing the need for high cost external filters and increasing performance for systems with excessive clock jitter. The AK4702 also including the audio switches and volumes designed primarily for digital set-top-box systems. The AK4702 is offered in a space saving 48-pin LQFP package.

FEATURES

DAC

- Sampling Rates Ranging from 8kHz to 50kHz
- 18bit 8x FIR Digital Filter
- 2nd order Analog LPF
- On chip Buffer with Single-ended Output
- Digital de-emphasis for 32k, 44.1k and 48kHz sampling
- I/F format: 18bit MSB justified, 18/16bit LSB justified, I²S
- Master clock: 256fs, 384fs
- High Tolerance to Clock Jitter

Analog switches for SCART

Audio section

- THD+N: -86dB (@2Vrms)
- Dynamic Range: 96dB (@2Vrms)
- Stereo Analog Volume with Zero-cross Detection Circuit (+6dB to -60dB & Mute)
- Five Analog Inputs
 - Two Stereo Input (TV, VCR SCART)
 - One Mono Input for Tone
- Five Analog Outputs
 - Two Stereo Outputs (TV, VCR SCART)
 - One Mono Output
- Loop-through mode for standby
- Pop Noise Free Circuit for Power on/off

Video section

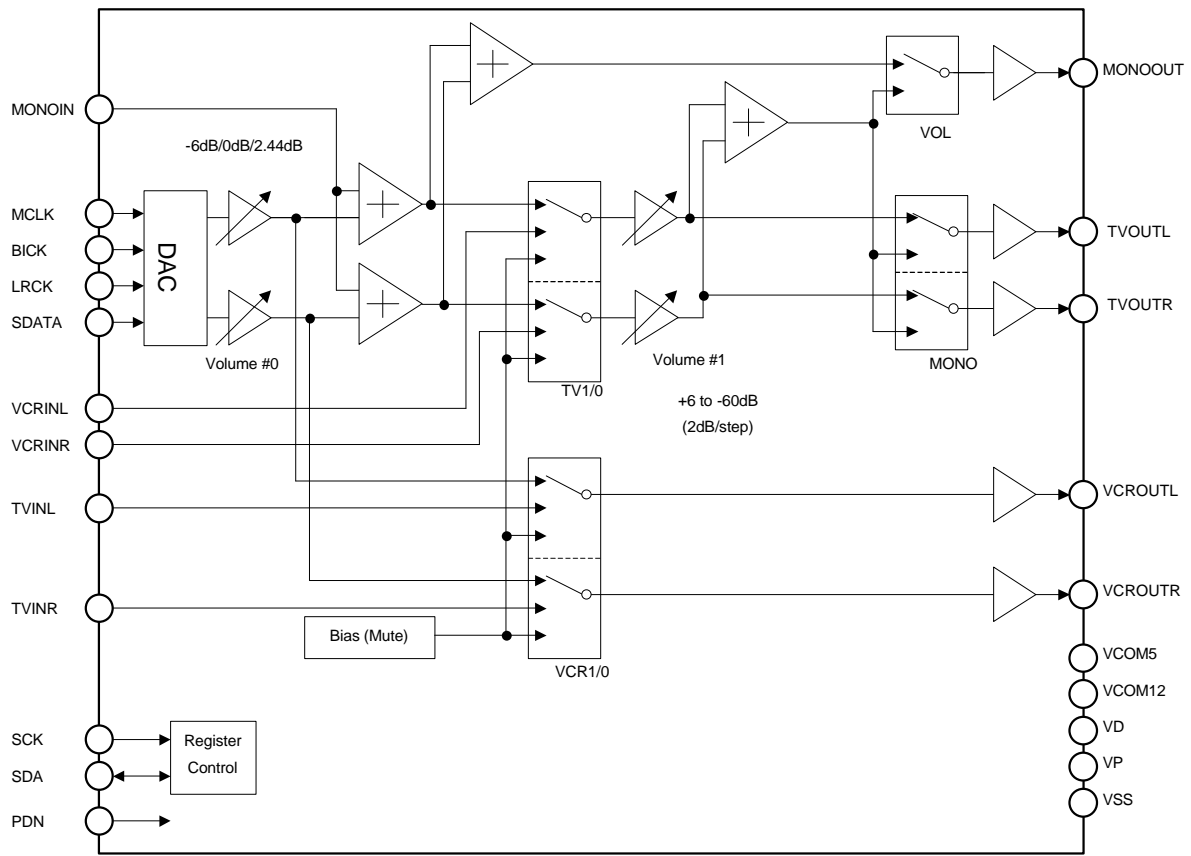
- 75ohm driver
- 6dB Gain for Outputs
- Adjustable gain
- Four CVBS/Y inputs (ENCx2, TV, VCR), Three CVBS/Y output (RF, TV, VCR)
- Three R/C inputs (ENCx2, VCR), Two R/C output (TV, VCR)
- Bi-directional control for VCR-Chroma/Red
- Two G and B inputs (ENC, VCR), One G and B outputs (TV)

Power supply

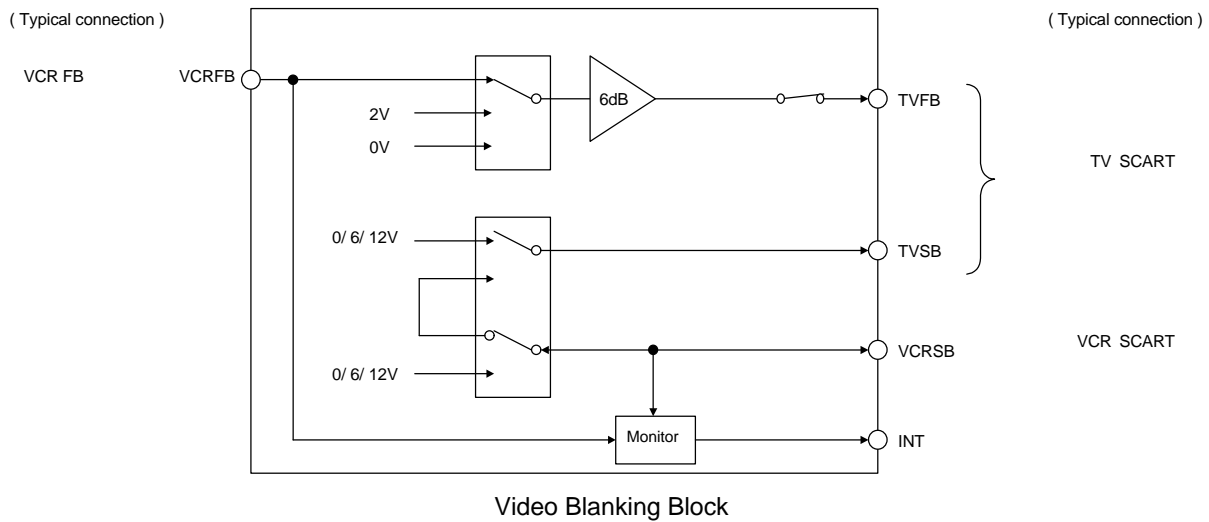
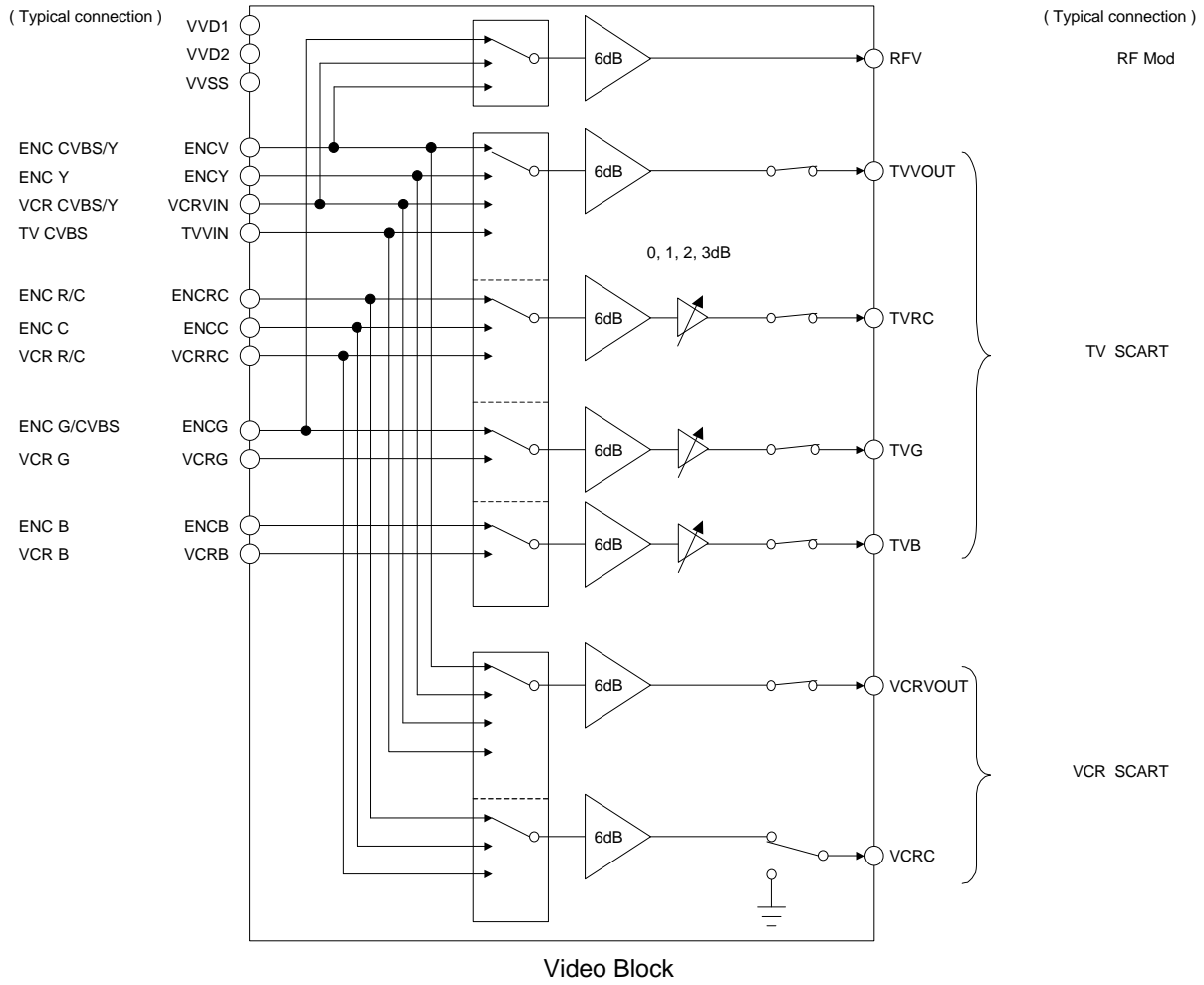
- 5V+/-5% and 12V+/-5%
- Low Power Dissipation

Package

- Small 48pin LQFP



Audio Block



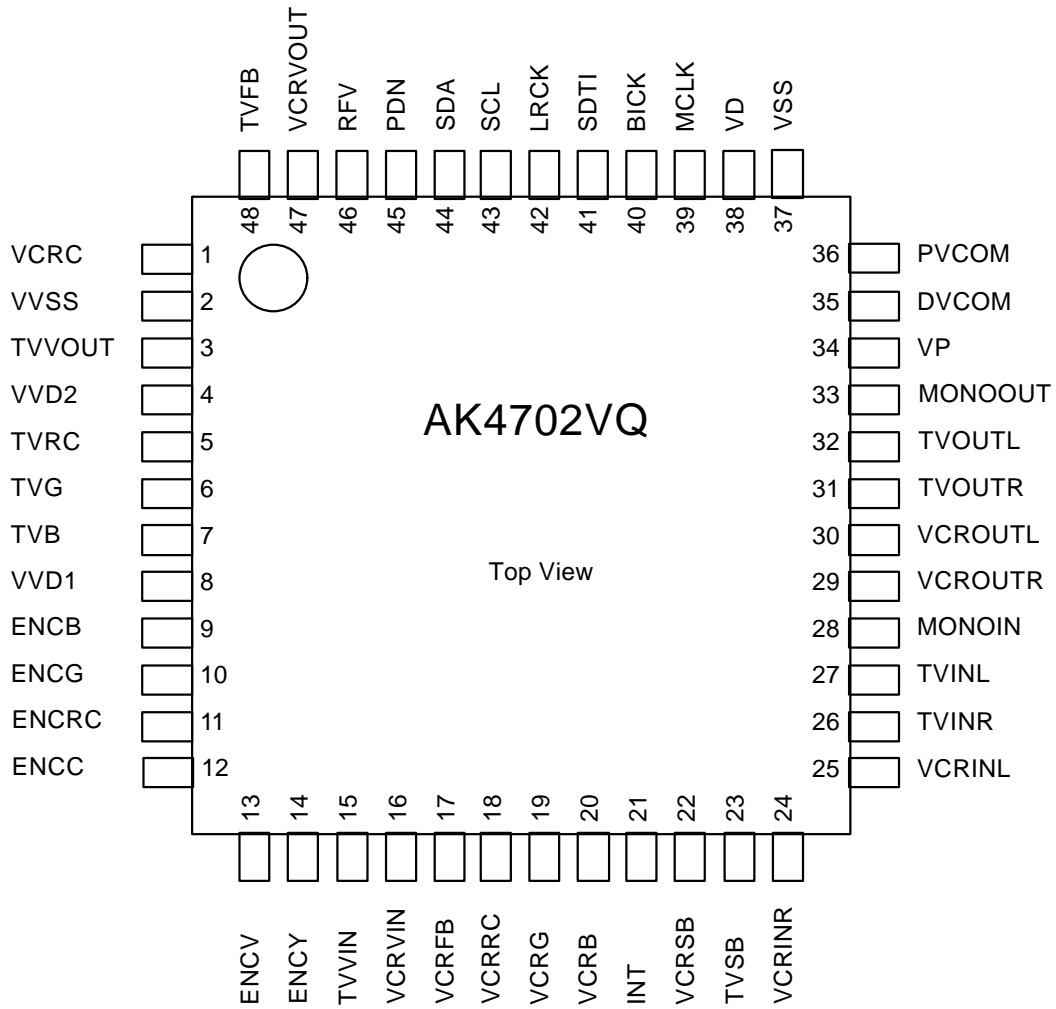
■ Ordering Guide

AK4702

-10 ~ +70°C

48pin LQFP (0.5mm pitch)

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCRC	O	Chrominance Output Pin for VCR
2	VVSS	-	Video Ground Pin. 0V.
3	TVVOUT	O	Composite/Luminance Output Pin for TV
4	VVD2	-	Video Power Supply Pin #2. 5V Normally connected to VVSS with a 0.1 μ F ceramic capacitor in parallel with a 10 μ F electrolytic cap.
5	TVRC	O	Red/Chrominance Output Pin for TV
6	TVG	O	Green Output Pin for TV
7	TVB	O	Blue Output Pin for TV
8	VVD1	-	Video Power Supply Pin #1. 5V Normally connected to VVSS with a 0.1 μ F ceramic capacitor in parallel with a 10 μ F electrolytic cap.
9	ENCB	I	Blue Input Pin for Encoder
10	ENCG	I	Green Input Pin for Encoder
11	ENCRC	I	Red/Chrominance Input Pin1 for Encoder
12	ENCC	I	Chrominance Input Pin2 for Encoder
13	ENCV	I	Composite/Luminance Input Pin1 for Encoder
14	ENCY	I	Composite/Luminance Input Pin2 for Encoder
15	TVVIN	I	Composite/Luminance Input Pin for TV
16	VCRVIN	I	Composite/Luminance Input Pin for VCR
17	VCRFB	I	Fast Blanking Input Pin for VCR
18	VCRRC	I	Red/Chrominance Input Pin for VCR
19	VCRG	I	Green Input Pin for VCR
20	VCRB	I	Blue Input Pin for VCR
21	INT	O	Interrupt Pin for Video Blanking
22	VCRSB	I/O	Slow Blanking Input/Output Pin for VCR
23	TVSB	O	Slow Blanking Output Pin for TV
24	VCRINR	I	Rch VCR Audio Input Pin
25	VCRINL	I	Lch VCR Audio Input Pin
26	TVINR	I	Rch TV Audio Input Pin
27	TVINL	I	Lch TV Audio Input Pin
28	MONOIN	I	MONO Input Pin
29	VCROUTR	O	Rch Analog Output Pin1
30	VCROUTL	O	Lch Analog Output Pin1
31	TVOUTR	O	Rch Analog Output Pin2
32	TVOUTL	O	Lch Analog Output Pin2
33	MONOOUT	O	MONO Analog Output Pin
34	VP	-	Power Supply Pin. 12V Normally connected to VSS with a 0.1 μ F ceramic capacitor in parallel with a 10 μ F electrolytic cap.
35	DVCOM	O	DAC Common Voltage Pin Normally connected to VSS with a 0.1 μ F ceramic capacitor in parallel with a 10 μ F electrolytic cap.
36	PVCOM	O	Audio Common Voltage Pin Normally connected to VSS with a 0.1 μ F ceramic capacitor in parallel with a 10 μ F electrolytic cap. The caps affect the settling time of audio bias level.

PIN/FUNCTION (Continued)

37	VSS	-	Ground Pin. 0V.
38	VD	-	DAC Power Supply Pin. 5V Normally connected to VSS with a 0.1 μ F ceramic capacitor in parallel with a 10 μ F electrolytic cap.
39	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
40	BICK	I	Audio Serial Data Clock Pin
41	SDTI	I	Audio Serial Data Input Pin
42	LRCK	I	L/R Clock Pin
43	SCL	I	Control Data Clock Pin
44	SDA	I/O	Control Data Pin
45	PDN	I	Power-Down Mode Pin When at "L", the AK4702 is in the power-down mode and is held in reset. The AK4702 should always be reset upon power-up.
46	RFV	O	Composite Output Pin for RF modulator
47	VCRVOUT	O	Composite/Luminance Output Pin for VCR
48	TVFB	O	Fast Blanking Output Pin for TV

Note: All input pins except pull-up/down pin should not be left floating.

Internal Equivalent Circuits				
Pin No.	Pin Name	Type	Equivalent Circuit	Description
39 40 41 42 43 45	MCLK BICK SDTI LRCK SCL PDN	Digital IN		
44	SDA	Digital I/O		I2C Bus voltage must not exceed VD.
21	INT	Digital OUT		Normally connected to VD(5V) through 10kohm resistor externally.
46 47 48 1 3 5 6 7	RFV VCROUT TVFB VCRC TVVOUT TVRC TVG TVB	Video OUT		

Pin No.	Pin Name	Type	Equivalent Circuit	Description
9 10 11 12 13 14 15 16 17 18 19 20	ENCB ENCG ENCRC ENCC ENCV ENCY TVVIN VCRVIN VCRFB VCRRC VCRG VCRB	Video IN		
22 23	VCRSB TVSB	Video SB		The 120kohm is not attached for TVSB.
24 25 26 27 28	VCRINR VCRINL TVINR TVINL MONOIN	Audio IN		
29 30 31 32 33	VCROUTR VCROUTL TVOUTR TVOUTL MONOOUT	Audio OUT		
35 36	DVCOM PVCOM	VCOM OUT		

ABSOLUTE MAXIMUM RATINGS

(VSS=VVSS=0V; Note: 1)

Parameter	Symbol	min	max	Units
Power Supply	VD	-0.3	6.0	V
	VVD1	-0.3	6.0	V
	VVD2	-0.3	6.0	V
	VP	-0.3	14	V
	VSS-VVSS (Note: 2)	-	0.3	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VD+0.3	V
Video Input Voltage	VINV	-0.3	VVD1+0.3	V
Audio Input Voltage	VINA	-0.3	VP+0.3	V
Ambient Operating Temperature	Ta	-10	70	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.

Note: 2. VSS and VVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=VVSS=0V; Note: 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VD	4.75	5.0	5.25	V
	VVD1	4.75	5.0	VVD2	V
	VVD2	VVD1	5.0	5.25	V
	VP	11.4	12	12.6	V

Note: 3. Analog output voltage scales with the voltage of VD.

$$AOUT (typ@0dB) = 2V_{rms} \times VD/5.$$

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C; VP=12V, VD = 5V; VVD1=VVD2 = 5V; fs = 48kHz; BICK = 64fs)

Power Supplies				
Power Supply Current				
Normal Operation (PDN = "H"; Note: 4)				
VD		14	30	mA
VVD1+VVD2		20	40	mA
VP		5	10	mA
Power-Down Mode (PDN = "L"; Note: 5)				
VD		10	100	μA
VVD1+VVD2		10	100	μA
VP		10	100	μA

Note: 4. STBY bit = "L", All video outputs active.

No signal, no load for A/V switches. fs=48kHz "0" data input for DAC.

Note: 5. All digital inputs including clock pins (MCLK, BICK and LRCK) are held at VD or VSS.

FILTER CHARACTERISTICS (AUDIO)						
(Ta = 25°C; VP=11.4-12.6V, VD = 4.75-5.25V, VVD1=VVD2 = 4.75-5.25V; fs = 48kHz; DEM0 = "1", DEM1 = "0")						
Parameter	Symbol	min	typ	max	Units	
Digital filter						
Passband	±0.05dB (Note: 13) -6.0dB	PB	0	24.0	21.77	kHz
			-		-	kHz
Stopband	(Note: 13)	SB	26.23			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	54			dB
Group Delay	(Note: 14)	GD	-	19.1	-	1/fs
Digital Filter + LPF						
Frequency Response	0 ~ 20.0kHz	FR	-	±0.5	-	dB

Note: 13. The passband and stopband frequencies scale with fs (system sampling rate).
ex.) PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

Note: 14. The calculating delay time which occurred by digital filtering. This time is from setting the 16/18bit data of both channels to input register to the output of analog signal.

ANALOG CHARACTERISTICS (VIDEO)						
(Ta = 25°C; VP=12V, VD = 5V; VVD1=VVD2 = 5V; VVOL1/0= "00" unless specified.)						
Parameter	Conditions	min	typ	max	Units	
Sync tip clamp voltage at output			0.7			V
Chrominance bias voltage at output			2.2			V
Gain	Input=0.3Vp-p, 100kHz	5.5	6	6.5		dB
RGB Gain	Input=0.3Vp-p, 100kHz	VVOL1/0= "00"	5.5	6	6.5	dB
		VVOL1/0= "01"	6.7	7.2	7.7	dB
		VVOL1/0= "10"	7.7	8.2	8.7	dB
		VVOL1/0= "11"	8.6	9.1	9.6	dB
Interchannel Gain Mismatch	Input=0.3Vp-p, 100kHz (Note: 15)	-0.3	-	0.3		dB
Frequency response	Input=0.3Vp-p, Response at 6MHz	-1	-0.5			dB
Input impedance	Chrominance input (internally biased)	40	60	-		kohm
Input Signal	f=100kHz, maximum with distortion < 1.0%, gain=6dB.	-	-	1.5		Vpp
Load Resistance	Except RFV pin (Note: 16)	150	-	-		ohm
	RFV pin (Note: 17)	20k	-	-		ohm
Load Capacitance	C1 (Note: 16)			400		pF
	C2 (Note: 16, Note: 17)			15		pF
Dynamic Output Signal	f=100kHz, maximum with distortion < 1.0%	-	-	3		Vpp
Y/C Cross talk	f=4.43MHz, 1Vp-p input. Among TVVOUT, TVRC, VCRVOUT and VCRC outputs.	-	-50	-		dB
S/N	Reference Level = 0.7Vp-p, CCIR 567 weighting. BW= 15kHz to 5MHz.	-	74	-		dB
Differential Gain	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-3	-	3		%
Differential Phase	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-3	-	3		Degree

Note: 15. TVRC, TVG, TVB.

Note: 16. Refer the Figure 1.

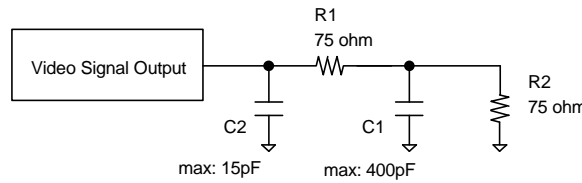


Figure 1. Load Resistance R1+R2, and Load Capacitance C1 and C2.

Note: 17. AC load. Refer the Figure 2.

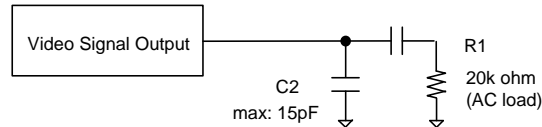


Figure 2. Load Resistance R1 and Load Capacitance C1

SWITCHING CHARACTERISTICS					
(Ta = 25°C; VP=11.4 ~ 12.6V, VD = 4.75 ~ 5.25V, VVD1=VVD2 = 4.75 ~ 5.25V; CL = 20pF)					
Parameter	Symbol	Min	typ	max	Units
Master Clock Frequency	256fs:	fCLK	2.048	12.8	MHz
Duty Cycle		dCLK	40	60	%
384fs:		fCLK	3.072	19.2	MHz
Duty Cycle		dCLK	40	60	%
LRCK Frequency		fs	8	50	kHz
Duty Cycle		Duty	45	55	%
Audio Interface Timing					
BICK Period		tBCK	312.5		ns
BICK Pulse Width Low		tBCKL	100		ns
Pulse Width High		tBCKH	100		ns
BICK “↑” to LRCK Edge	(Note: 18)	tBLR	50		ns
LRCK Edge to BICK “↑”	(Note: 18)	tLRB	50		ns
SDTI Hold Time		tSDH	50		ns
SDTI Setup Time		tSDS	50		ns
Control Interface Timing (I²C Bus):					
SCL Clock Frequency		fSCL	-	100	kHz
Bus Free Time Between Transmissions		tBUF	4.7	-	μs
Start Condition Hold Time		tHD:STA	4.0	-	μs
(prior to first clock pulse)					
Clock Low Time		tLOW	4.7	-	μs
Clock High Time		tHIGH	4.0	-	μs
Setup Time for Repeated Start Condition		tSU:STA	4.7	-	μs
SDA Hold Time from SCL Falling (Note: 19)		tHD:DAT	0	-	μs
SDA Setup Time from SCL Rising		tSU:DAT	0.25	-	μs
Rise Time of Both SDA and SCL Lines		tR	-	1.0	μs
Fall Time of Both SDA and SCL Lines		tF	-	0.3	μs
Setup Time for Stop Condition		tSU:STO	4.0	-	μs
Pulse Width of Spike Noise		tSP	0	50	ns
Suppressed by Input Filter					
Reset Timing					
PDN Pulse Width	(Note: 20)	tPD	150		ns

Note: 18. BICK rising edge must not occur at the same time as LRCK edge.

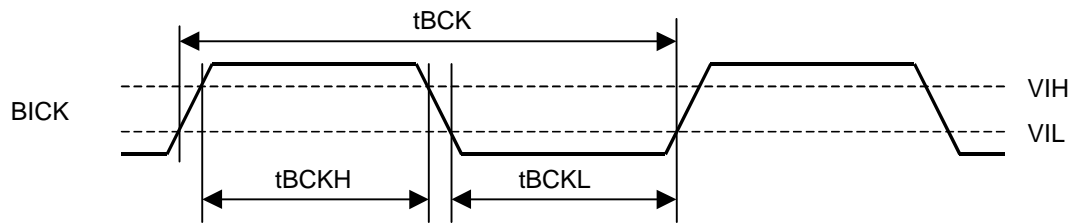
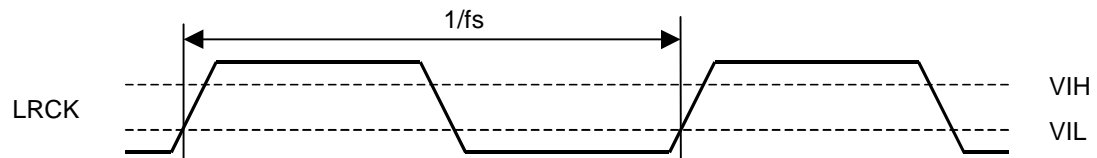
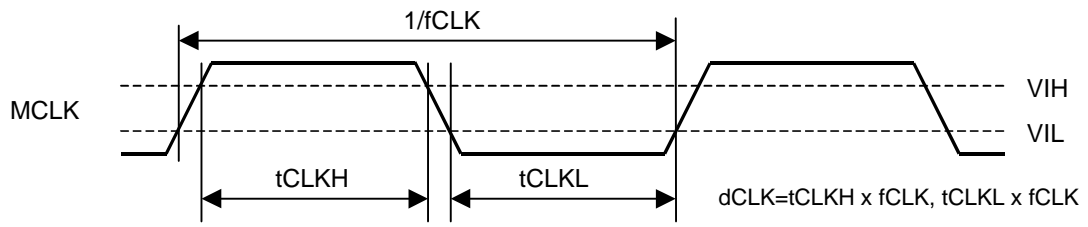
Note: 19. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note: 20. The AK4702 should be reset by PDN= "L" upon power up.

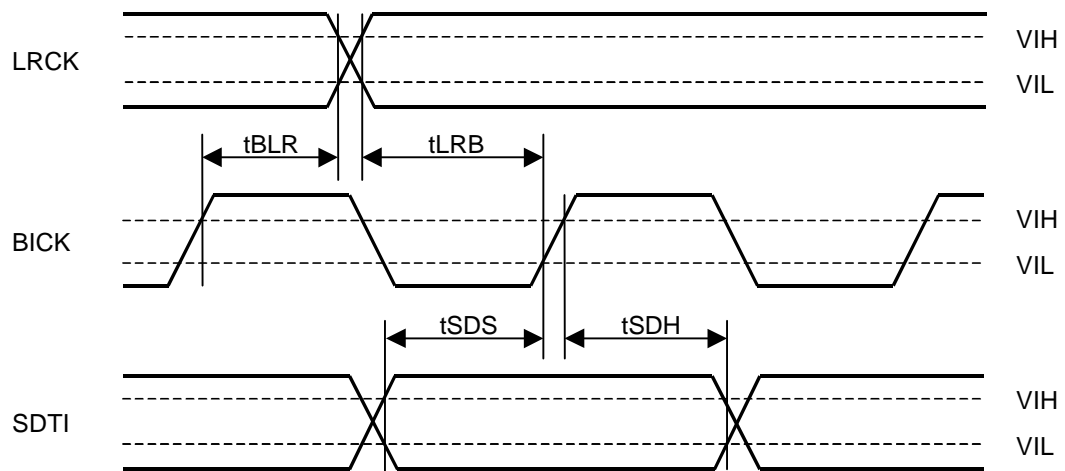
Note: 21. I²C is a registered trademark of Philips Semiconductors.

Purchase of Asahi Kasei Microsystems Co., Ltd I²C components conveys a license under the Philips I²C patent to use the components in the I²C system, provided the system conform to the I²C specifications defined by Philips.

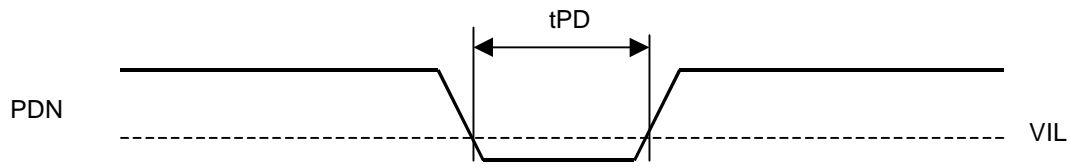
■ Timing Diagram



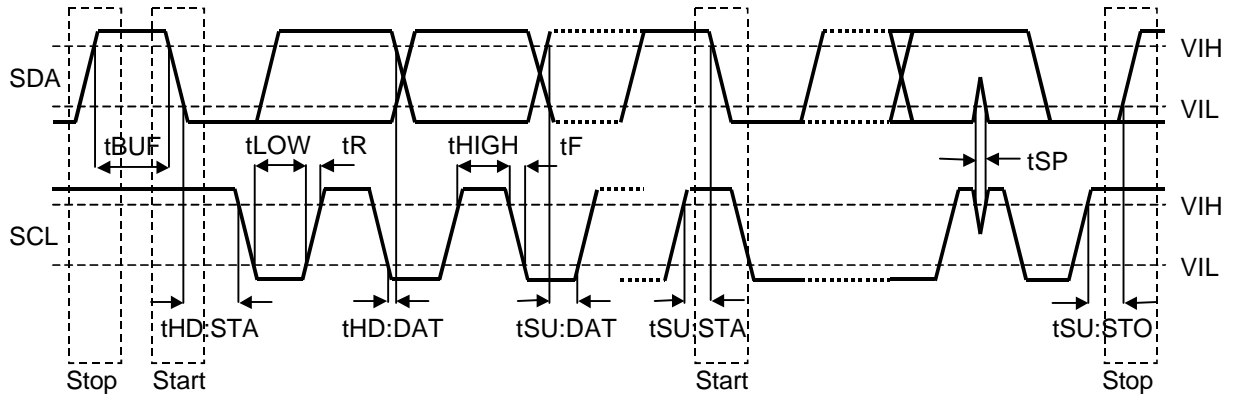
Clock Timing



Serial Interface Timing



Power-down Timing



I²C Bus mode Timing

OPERATION OVERVIEW

■ **System Clock**

The external clocks required to operate the DAC section of AK4702 are MCLK, LRCK and BICK. The master clock (MCLK) corresponds to 256fs or 384fs. MCLK frequency is automatically detected, and the internal master clock becomes 256fs. The MCLK should be synchronized with LRCK but the phase is not critical. Table 1 illustrates corresponding clock frequencies. All external clocks (MCLK, BICK and LRCK) should always be present whenever the DAC section of AK4702 is in the normal operating mode (STBY bit = “0”). If these clocks are not provided, the AK4702 may draw excess current because the device utilizes dynamically refreshed logic internally. The DAC section of the AK4702 should be reset by STBY = “0” after these clocks are provided. If the external clocks are not present, place the AK4702 in power-down mode (STBY bit = “1”). After exiting reset at power-up etc., the AK4702 remains in power-down mode until MCLK and LRCK are input.

LRCK	MCLK		BICK
fs	256fs	384fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	3.0720MHz

Table 1. System clock example

■ **Audio Serial Interface Format**

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF0 and DIF1 bits can select four formats in serial mode as shown in Table 2. In all modes, the serial data is MSB-first, 2’s compliment format and is latched on the rising edge of BICK. Mode 2 can also be used for 16 MSB justified formats by zeroing the unused two LSBs.

Mode	DIF1	DIF0	SDTI Format	BICK	Figure
0	0	0	16bit LSB Justified	≥32fs	Figure 3
1	0	1	18bit LSB Justified	≥36fs	Figure 3
2	1	0	18bit MSB Justified	≥36fs	Figure 4
3	1	1	18bit I ² S Compatible	≥36fs or 32fs	Figure 5

Default

Table 2. Audio Data Formats

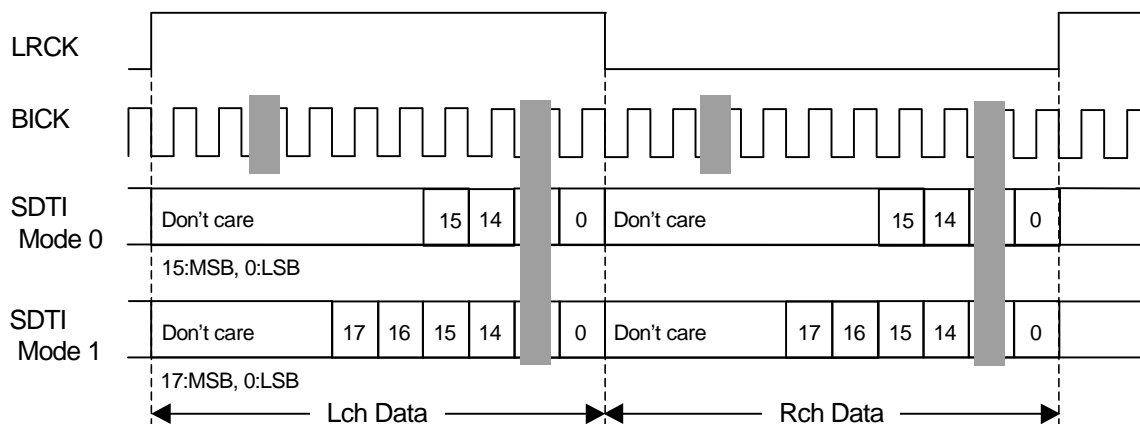


Figure 3. Mode 0,1 Timing

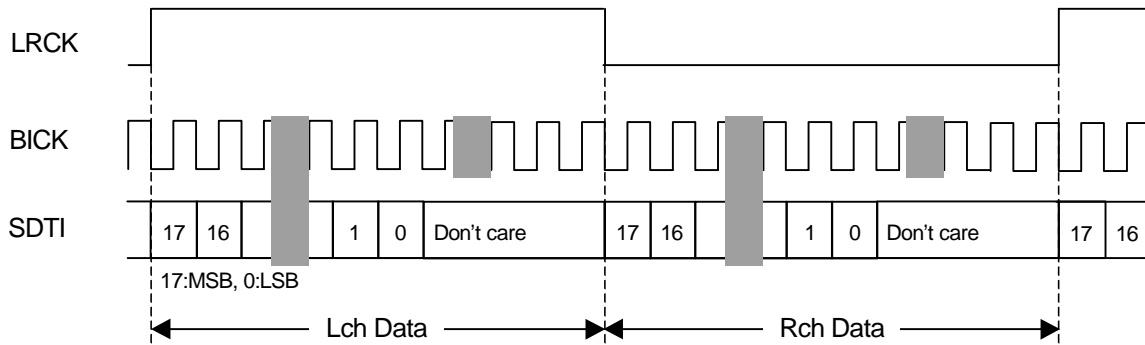


Figure 4. Mode 2 Timing

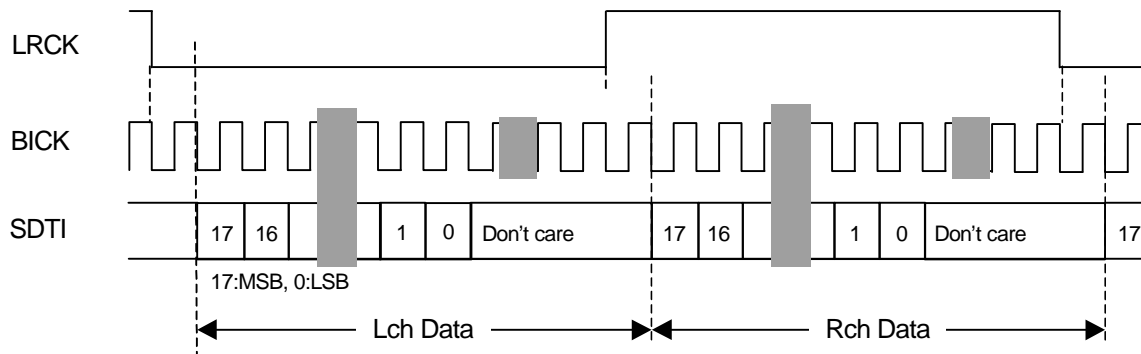


Figure 5. Mode 3 Timing

■ De-emphasis filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates ($t_c = 50/15\mu s$) and is controlled by the DEM0 and DEM1 bits.

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Default

Table 3. De-emphasis filter control

■ Volume/Switch Control

The AK4702 has analog volume controls and switch matrixes designed primarily for SCART routing. Those are controlled via the control register as shown in, Table 4, Table 5, Table 7 and Table 8. (Please refer to the block diagram in figure 1.)

DVOL1	DVOL0	Gain	Output Level (at volume#1=0dB)
0	0	0dB	2Vrms
0	1	-6dB	1Vrms
1	0	2.44dB	2.65Vrms
1	1	(Reserved)	(Reserved)

Table 4. Volume #0 (Digital Volume for DAC)

L5	L4	L3	L2	L1	L0	Gain
1	0	0	0	1	0	+6dB
1	0	0	0	0	1	+4dB
1	0	0	0	0	0	+2dB
0	1	1	1	1	1	0dB (default)
...
0	0	0	0	0	1	-60dB
0	0	0	0	0	0	Mute

Note: Do not exceed 3Vrms as analog output.

Table 5. Volume #1 (Analog Volume)

TV1	TV0	Source of TVOUTL/R
0	0	DAC
0	1	VCRIN (default)
1	0	Mute
1	1	(Reserved)

Table 6. TVOUT Switch Configuration

VOL	TV1	TV0	Source of MONOOUT	
0	0	0	DAC (L+R)/2	Bypass the volume #1
0	0	1	DAC (L+R)/2	
0	1	0	DAC (L+R)/2	
0	1	1	(Reserved)	
1	0	0	DAC (L+R)/2	Through the volume #1
1	0	1	VCRIN (L+R)/2	
1	1	0	Mute	
1	1	1	(Reserved)	

Table 7. MONOOUT Switch Configuration

VCR1	VCR0	Source of VCROUTL/R
0	0	DAC
0	1	TVIN (default)
1	0	Mute
1	1	(Reserved)

Table 8. VCROUT Switch Configuration

■ Zero-cross Detection and Offset Calibration

To minimize the click noise when changing the gain of volume#1, the AK4702 has a zero-cross detection and an offset calibration function.

1. Zero-cross detection function

When the ZERO bit = "1", the zero-cross detection function is enabled. The gain of volume#1 changes at the first zero-cross point from the acknowledgement of a volume changing command or when the zero-cross is not detected within the time set by ZTM1-0 bits (256/fs to 2048/fs). The zero-cross counter is initialized whenever a gain is issued. The zero-cross is detected on L/R channels independently. To disable this function, set the ZERO bit to "0".

ZERO: Zero-cross detection enable for volume#1

- 0 : Disable. The volume value changes immediately without zero-cross.
- 1 : Enable (default). The volume value changes at a zero-crossing point or when timeout (ZTM1-0 bit setting) occurs.

The internal comparator for zero-cross detection has a small offset. Therefore, the gain of volume #1 may change due to a zero-cross timeout before the comparator-based zero-cross detection occurs.

When the new gain value 1EH(-2dB) is written while the gain of both Lch and Rch are 1FH(0dB), if the Lch detects the zero-cross prior to Rch, only the gain of Lch changes to 1EH(-2dB) while Rch waits for a zero-cross. After that, if the gain is set to 1DH(-4dB) before either a zero-cross or zero-cross timeout, the Rch keeps the same value and changes from 1FH to 1DH at next zero-cross or timeout.

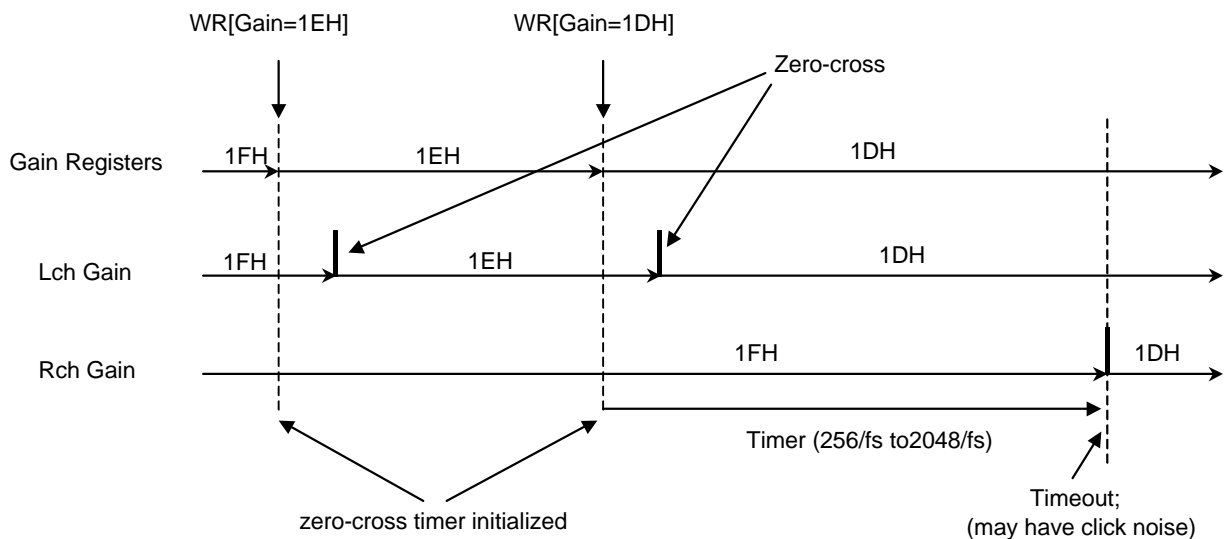


Figure 6. Zero-cross Operation (ZERO= "1")

2. Offset calibration function

Offset calibration is enabled when the CAL bit = "1". This function begins when the TVOUT source is switched to DAC after the STBY bit is changed to "0". It takes 1664/fs to execute the offset calibration cycle. During the offset calibration cycle, the analog outputs are muted. Once the offset calibration is executed, the calibration memory is held until PDN="L" or the new calibration is executed. When the switch is changed from DAC to VCR during calibration, the calibration is discontinued, and resumed when TVOUT is switched back to DAC. If volume#1 gain is changed during calibration, the change takes place after calibration is complete.

■ Standby Mode

When the MUTE bit = "0" and the STBY bit = "1", the AK4702 is forced into TV-VCR loop through mode. In this mode, the sources of TVOUTL/R and MONOOUT are fixed to VCRINL/R, the sources of VCROUTL/R are fixed to TVINL/R respectively. The gain of volume#1 is fixed to 0dB. Since all registers are NOT initialized by STBY="1", a register switch configuration requires standby mode (STBY="0").

■ System Reset and Power-down control

The AK4702 should be reset once by bringing PDN = “L” upon power-up. The AK4702 has several power-down modes. The PDN pin, MUTE bit and STBY bit control them as shown in Table 9 and Table 10.

PDN pin: Power down pin.

“H”: Normal operation

“L”: Device power down.

MUTE bit: Analog Mute bit.

“1”: Mute all analog outputs

“0”: Normal operation

STBY bit : Standby bit.

“1”: Standby mode, DAC is powered down, volume is fixed to 0dB, the analog audio/video paths are fixed to TV-VCR loop-through.

“0”: Normal operation.

After when the PDN pin is set to “H”, the AK4702 is in standby mode and muted. To exit the mute and enter standby mode, set the MUTE bit to “0” and the STBY bit to “1”. To use the DAC or change analog switches, set the STBY bit to “0”. The DAC will power up and the internal timing starts clocking LRCK “↑” after exiting reset and power down states by MCLK. The AK4702 is in power-down mode until MCLK and LRCK are input.

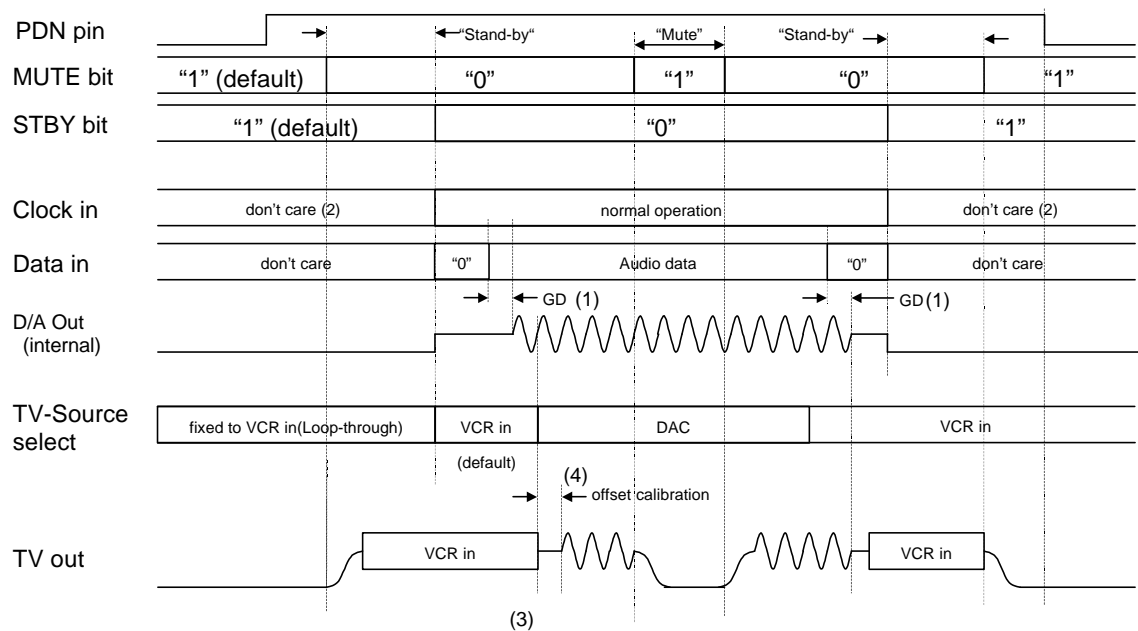
Mode		PDN pin	MUTE bit	STBY bit	MCLK, BICK, LRCK	DAC	Analog outputs	Register control
0	Device power-down	“L”	*	*	Not Needed	Powered Down	GND	Not Available
1	Standby and mute (default)	“H”	1	1	Not Needed	Powered Down	GND	Available
2	Standby	“H”	0	1	Not Needed	Powered Down	fixed to TV-VCR loop-through	Available
3	Mute	“H”	1	0	Needed	Active	GND	Available
4	Normal operation	“H”	0	0	Needed	Active	Active	Available

Table 9. Power-down modes (audio)

Mode		PDN pin	STBY bit	Video outputs	TVFB, TVSB	VCRSB
0	Power-down	“L”	*	Hi-z	Hi-z	Internally pulled down by 120kohm(typ) resister
1	Standby	“H”	1	Active (Path is fixed)	Active	Active
2	Normal operation	“H”	0	Active	Active	Active

Table 10. Power-down modes (video)

The Figure 7 shows an example of the system timing at the power-down and power-up by PDN pin.



Notes:

- (1) The analog output corresponding to the digital input has a group delay, GD.
- (2) The external clocks (MCLK, BICK and LRCK) can be stopped in standby mode.
- (3) Please mute the analog outputs externally if click noise(3) adversely affects the system.
- (4) In case of the CAL bit = "1", the offset calibration is always executed when the source of TVOUT is switched to DAC after the STBY bit is changed to "0". To disable this function, set the CAL bit = "0".

Figure 7. Power-down/up sequence example

■ Mode Control Interface

I²C-bus Control Mode

The AK4702 supports the standard-mode I²C-bus (max: 100kHz). Then AK4702 doesn't support the fast-mode I²C-bus system (max: 400kHz).

1. WRITE Operations

Figure 8 shows the data transfer sequence in I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 14). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010001". If the slave address match that of the AK4702, the AK4702 generates the acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 15). A "1" for R/W bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed. The second byte consists of the address for control registers of the AK4702. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 10). The data after the second byte contain control data. The format is MSB first, 8bits (Figure 11). The AK4702 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 14).

The AK4702 can execute multiple one byte write operations in a sequence. After receipt of the third byte, the AK4702 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 08H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 16) except for the START and the STOP condition.

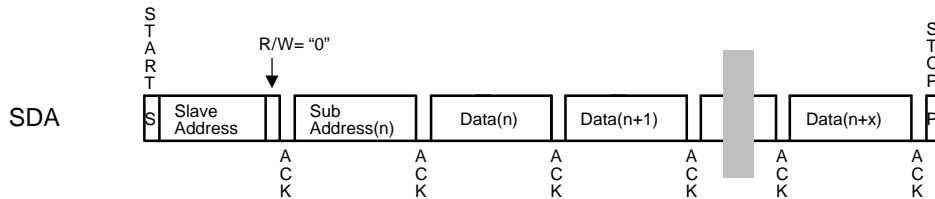


Figure 8. Data transfer sequence at the I²C-bus mode

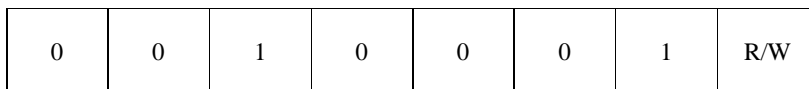


Figure 9. The first byte

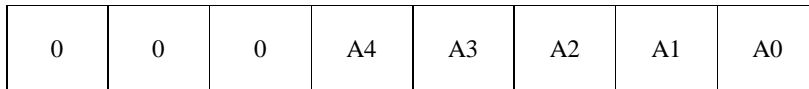


Figure 10. The second byte

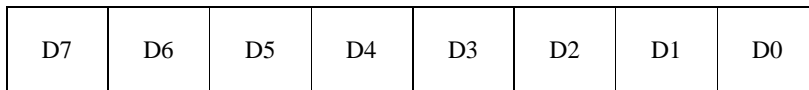


Figure 11. Byte structure after the second byte

2. READ Operations

Set R/W bit = "1" for READ operations. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 08H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4702 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-1. CURRENT ADDRESS READ

The AK4702 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4702 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4702 discontinues transmission

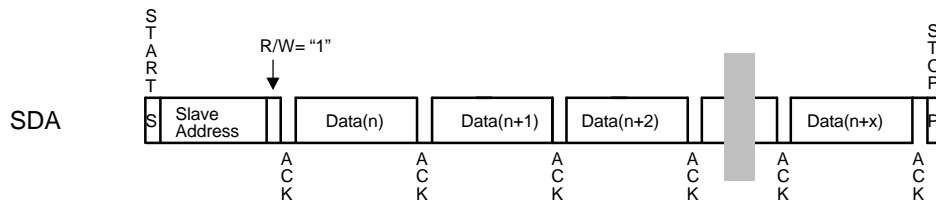


Figure 12. CURRENT ADDRESS READ

2-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address(R/W="0") and then the register address to read. After the register's address is acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4702 generates an acknowledge, 1-byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4702 discontinues transmission.

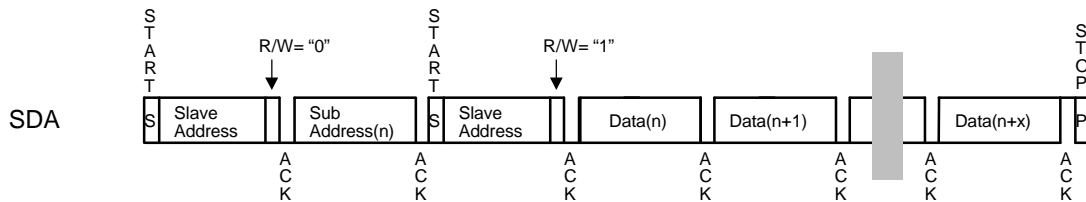


Figure 13. RANDOM ADDRESS READ

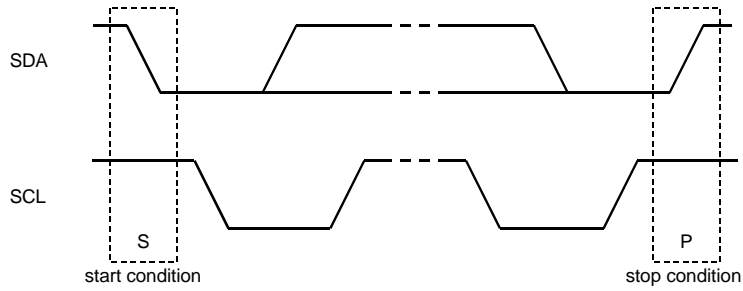


Figure 14. START and STOP conditions

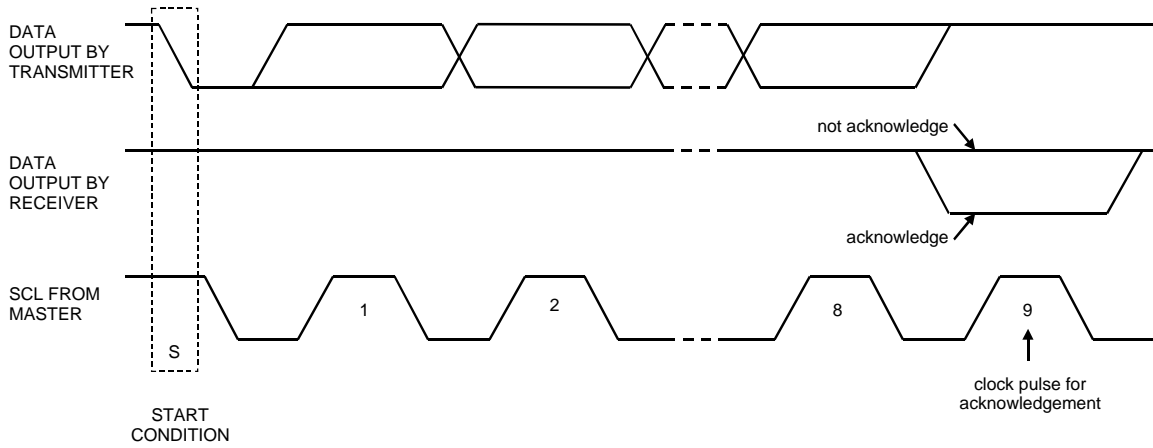


Figure 15. Acknowledge on the I²C-bus

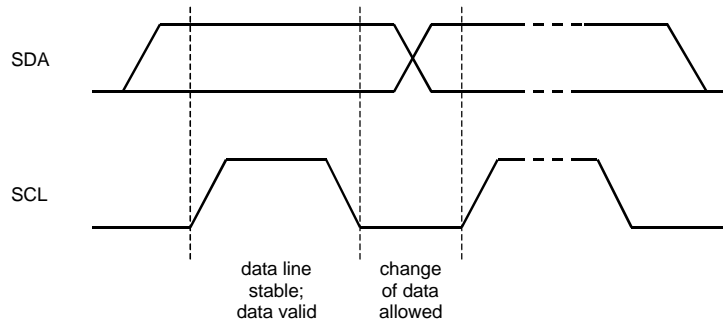


Figure 16. Bit transfer on the I²C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	DEM1	DEM0	DIF1	DIF0	0	0	MUTE	STBY
01H	Switch	VMUTE	MMON	VCR1	VCR0	MONO	VOL	TV1	TV0
02H	Main Volume	0	0	L5	L4	L3	L2	L1	L0
03H	Zerocross	0	0	CAL	DVOL1	DVOL0	ZERO	ZTM1	ZTM0
04H	Video Switch	VRF1	VRF0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
05H	Video output enable	CIO	TVFB	VCRC	VCRV	TVB	TVG	TVR	TVV
06H	Video Volume/Clamp	0	VCLP1	VCLP0	0	CLAMP1	CLAMP0	VVOL1	VVOL0
07H	S/F Blanking control	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
08H	S/F Blanking monitor	0	0	0	0	0	FVCR	SVCR1	SVCR0

When the PDN pin goes “L”, the registers are initialized to their default values.

While the PDN=“H”, all registers can be accessed.

Do not write any data to the register over 08H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	DEM1	DEM0	DIF1	DIF0	0	0	MUTE	STBY
	R/W	R/W							
	default	0	1	1	1	0	0	1	1

STBY: Standby control

0 : Normal Operation

1 : Standby Mode(default). All registers are not initialized.

DAC : powered down and timings are reset.
Gain of Volume#1 : fixed to 0dB,
Source of TVOUT : fixed to VCRIN,
Source of VCROUT : fixed to TVIN,
Source of MONOOUT : fixed to VCRIN,
Source of TVVOUT : fixed to VCRVIN(or Hi-Z),
Source of TVRC : fixed to VCRRC(or Hi-Z),
Source of TVG : fixed to VCRG(or Hi-Z),
Source of TVB : fixed to VCRB(or Hi-Z),
Source of VCRVOUT : fixed to TVVIN(or Hi-Z),
Source of VCRC : fixed to Hi-Z or VSS(controlled by CIO bit).

MUTE: Audio output control

0 : Normal Operation

1 : ALL Audio outputs to GND (default)

DIF1-0: Audio data interface format control

00 : 16bit LSB Justified

01 : 18bit LSB Justified

10 : 18bit MSB Justified

11 : 18bit I²S Compatible (Default)

DEM1-0: De-emphasis Response Control

00 : 44.1kHz

01 : off (Default)

10 : 48kHz

11 : 32kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Switch	VMUTE	MMON	VCR1	VCR0	MONO	VOL	TV1	TV0
	R/W	R/W							
	default	1	1	0	1	0	1	0	1

TV1-0: TVOUT source switch

- 00 : DAC
- 01 : VCRIN (Default)
- 10 : MUTE
- 11 : (Reserved)

VOL: Source select for MONOOUT

- 0 : Bypass the volume (fixed to DAC out)
- 1 : Through the volume (Default)

MONO: Mono select for TVOUT

- 0 : Stereo. (Default)
- 1 : Mono. (L+R)/2

VCR1-0: VCROUT source switch

- 00 : DAC
- 01 : TVIN (Default)
- 10 : MUTE
- 11 : (Reserved)

MMON: Mute of MONOIN input

- 0 : Add the MONOIN
- 1 : Mute the MONOIN (default)

VMUTE: Mute switch for volume#1

- 0 : Normal operation
- 1 : Mute the volume#1 (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Main Volume	0	0	L5	L4	L3	L2	L1	L0
	R/W	R/W							
	default	0	0	0	1	1	1	1	1

L5-0: Volume#1 control

Those registers control both Lch and Rch of Volume#1.

- 111111 to
- 100011 : (Reserved)
- 100010 : Volume gain = +6dB
- 100001 : Volume gain = +4dB
- 100000 : Volume gain = +2dB
- 011111 : Volume gain = +0dB (default)
- 011110 : Volume gain = -2dB
- ...
- 000011 : Volume gain = -56dB
- 000010 : Volume gain = -58dB
- 000001 : Volume gain = -60dB
- 000000 : Volume gain = Mute

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Zerocross	0	0	CAL	DVOL1	DVOL0	ZERO	ZTM1	ZTM0
	R/W	R/W							
	default	0	0	1	0	0	1	1	1

ZTM1-0: The time length control of zero-cross timeout

- 00 : typ. 256/fs
- 01 : 512/fs
- 10 : 1024/fs
- 11 : 2048/fs (default)

ZERO: Zero-cross detection enable for volume control#1

- 0 : Disable
The volume value changes immediately without zero-cross.
- 1 : Enable (default)
The volume value changes when timeout or zero-cross before timeout.
This function is disabled when STBY= "1".

DVOL1-0: Digital volume control for DAC (Volume#0)

- 00 : 0dB
- 01 : -6dB
- 10 : +2.44dB
- 11 : (Reserved)

CAL: Offset calibration Enable

- 0 : Offset calibration disable.
- 1 : Offset calibration enable(default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Video Switch	VRF1	VRF0	VVCR2	VVCR1	VVCR0	VTV2	VTV1	VTV0
R/W		R/W							
default		1	0	0	1	1	1	0	0

VTV0-2: selector for TV video output

Mode	VTV2-0	TVVOUT	TVRC	TVG	TVB
Shutdown	000	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Encoder CVBS or RGB	001	Encoder CVBS ENCV	Encoder R ENCRC	Encoder G ENCG	Encoder B ENCB
Encoder Y/C 1	010	Encoder Luminance ENCV	Encoder Chrominance ENCRC	Hi-Z	Hi-Z
Encoder Y/C 2	011	Encoder Luminance ENCY	Encoder Chrominance ENCC	Hi-Z	Hi-Z
VCR (default)	100	VCR CVBS/Y VCRVIN	VCR R/C VCRRC	VCR G VCRG	VCR B VCRB
TV CVBS	101	TV CVBS/Y TVVIN	Hi-Z	Hi-Z	Hi-Z
(reserved)	110	-	-	-	-
(reserved)	111	-	-	-	-

Table 11. TV video output (see note)

VVCR0-2: selector for VCR video output

Mode	VVCR2-0	VCRVOUT	VCRC
Shutdown	000	Hi-Z	Hi-Z
Encoder CVBS or Y/C 1	001	Encoder CVBS/Y ENCV	Encoder Chrominance ENCRC
Encoder CVBS or Y/C 2	010	Encoder CVBS/Y ENCY	Encoder Chrominance ENCC
TV CVBS (default)	011	TV CVBS TVVIN	Hi-Z
VCR	100	VCR CVBS/Y VCRVIN	VCR R/C VCRRC
(reserved)	101	-	-
(reserved)	110	-	-
(reserved)	111	-	-

Table 12. VCR video output (see note)

VRF0-1: selector for RF video output

Mode	VRF1-0	RF CVBS
Encoder CVBS1	00	Encoder CVBS1 ENCV
Encoder CVBS2	01	Encoder CVBS2 ENCG (Note: 23)
VCR (default)	10	VCR VCRVIN
Shutdown	11	Hi-Z

Table 13. RF video output (see note)

Note: 22: When input the video signal via ENCRC or VCRRC pin, set CLAMP1-0 bits respectively.

Note: 23 When VTV2-0="001", TVG="1" and VRF1-0="01", RFV output is same as TVG (Encoder G).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	output enable	CIO	TVFB	VCRC	VCRV	TVB	TVG	TVR	TVV
R/W		R/W							
default		0	0	0	0	0	0	0	0

Each video outputs can be set to Hi-Z individually.

- TVV : TVVOUT output control
- TVR : TVRCOUT output control
- TVG : TVGOUT output control
- TVB : TVBOUT output control
- VCRV : VCRVOUT output control
- VCRC : VCRC output control
- TVFB : TVFB output control
- 0 : Hi-Z (default)
- 1 : Active.

When CIO= "1", the VCRC pin is connected to GND even if VCRC= "0".

When CIO= "0", the VCRC pin follows the setting of VCRC bit.

CIO: VCR Chrominance I/O control

- 0 : Active (output).
- 1 : Connected to GND

CIO	VCRC	State of VCRC pin
0	0	Hi-z (default)
0	1	Active
1	0	Connected to GND
1	1	Connected to GND

Table 14 VCRC output control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Video Volume	0	VCLP1	VCLP0	0	CLAMP1	CLAMP0	VVOL1	VVOL0
	R/W	R/W							
	default	0	0	0	0	0	1	0	0

VVOL1-0: RGB video gain control

VVOL1	VVOL0	Gain	Output level (Typ. @Input=0.7Vpp)
0	0	+6dB	1.4Vpp (default)
0	1	+7.2dB	1.6Vpp
1	0	+8.2dB	1.8Vpp
1	1	+9.1dB	2.0Vpp

Table 15. RGB gain

CLAMP1 : Encoder R/Chroma (ENCRC pin)input clamp control

- 0 : DC restore clamp active (for RED signal. default)
- 1 : Biased (for Chroma signal.)

CLAMP0 : VCR R/C (VCRC pin)input clamp control

- 0 : DC restore clamp active (for RED signal)
- 1 : Biased (for Chroma signal. default.)

VCLP1-0 : DC restore source control

VCLP1	VCLP0	Sync Source of DC Restore
0	0	ENCV (default)
0	1	ENCY
1	0	VCRVIN
1	1	(Reserved)

Table 16. DC restore source control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	S/F Blanking	SBIO1	SBIO0	SBV1	SBV0	SBT1	SBT0	FB1	FB0
R/W		R/W							
default		0	0	0	0	0	0	0	0

FB1-0: TV Fast Blanking output control (for TVFB)

FB1	FB0	TV FB Output Level
0	0	0V (default)
0	1	4V
1	0	Same as VCR FB input (4V/0V)
1	1	(Reserved)

(note: minimum load is 150ohm)

Table 17. TV Fast Blanking output

SBT1-0: TV Slow Blanking output control (for TVSB)

SBT1	SBT0	Slow Blanking Output Level
0	0	<2V (default)
0	1	5V<, <7V
1	0	(Reserved)
1	1	10V<

(note: minimum load is 10kohm)

Table 18. TV Slow Blanking output

SBV1-0: VCR Slow Blanking output control (for VCRSB)

SBV1	SBV0	Slow Blanking Output Level
0	0	<2V (default)
0	1	5V<, <7V
1	0	(Reserved)
1	1	10V<

(note: minimum load is 10kohm)

Table 19. VCR Slow Blanking output

SBIO1-0: TV/VCR Slow Blanking I/O control

SBIO1	SBIO0	VCR Slow Blanking Direction	TV Slow Blanking Direction
0	0	Output (Controlled by SBV1,0)	Output (Controlled by SBT1,0)
0	1	(Reserved)	(Reserved)
1	0	Input (Stored in SVCR1,0)	Output (Controlled by SBT1,0)
1	1	Input (Stored in SVCR1,0)	Output (Same output as VCR SB)

(default)

Table 20. TV/VCR Slow Blanking output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	SB/FB Monitor	0	0	0	0	0	FVCR	SVCR1	SVCR0
R/W		READ							
default		0	0	0	0	0	0	0	0

SVCR1-0: VCR Slow blanking status monitor

Those bits reflect the voltage at VCRSB pin for both Input/Output modes

SVCR1	SVCR0	VCRSB Level
0	0	< 2V
0	1	4.5 to 7V
1	0	(Reserved)
1	1	9.5<

Table 21. VCR Slow Blanking monitor

FVCR: VCR Fast blanking input level monitor

This bit is enabled when TVFB bit = "1".

FVCR	VCRFB Input Level
0	<0.4V
1	1 V<

Table 22. VCR Fast Blanking monitor (Typical threshold is 0.7V)

Changes to the 08H status can be monitored via the INT pin. The INT pin is the open drain output and goes "L" for 2usec(typ.) when the status of 08H is changed. This pin should be connected to VD (typ. 5V) through 10kohm resistor.

SYSTEM DESIGN

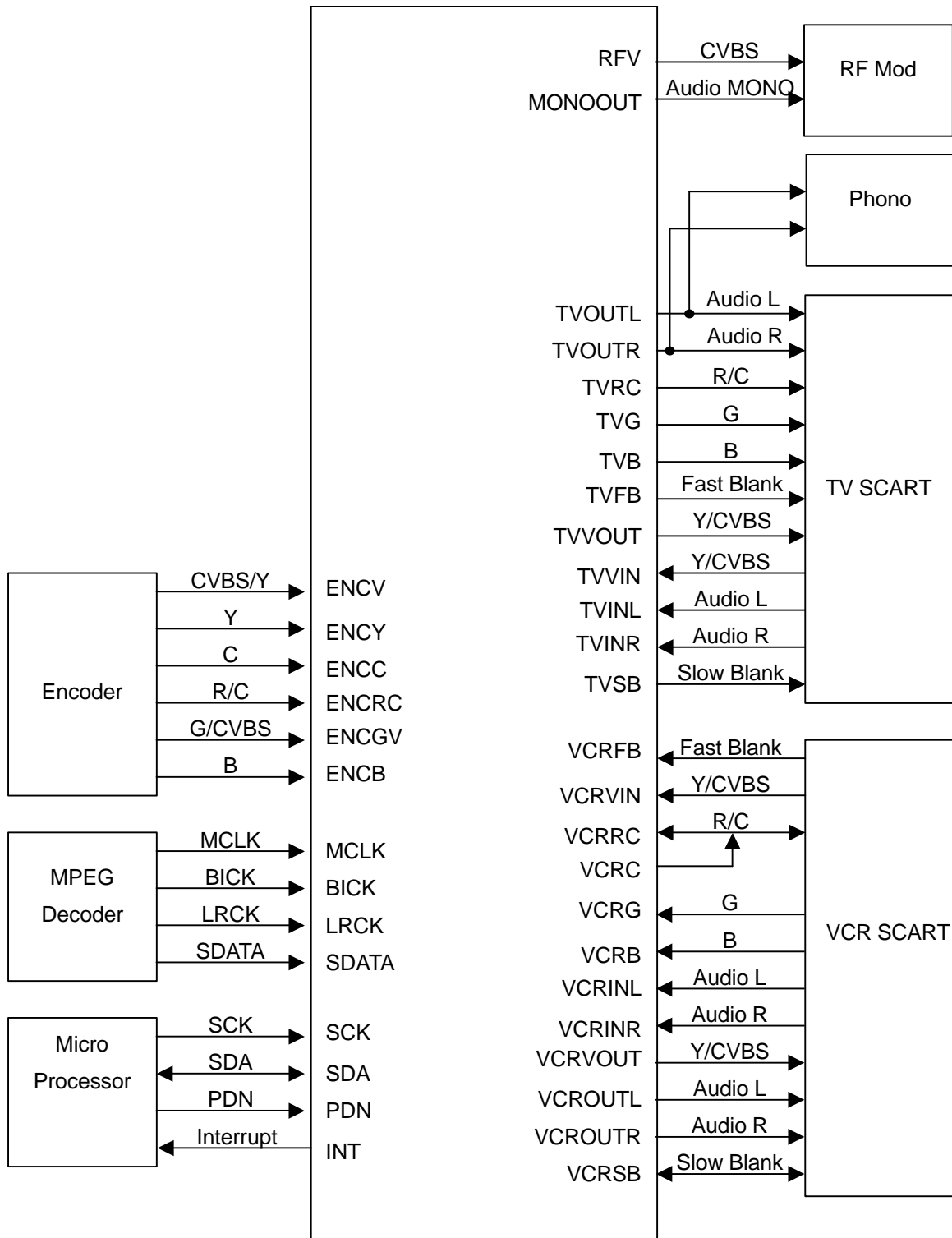


Figure 17. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

VD, VP, VVD1, VVD2, VSS and VVSS should be supplied from analog supply unit and be separated from system digital supply. Decoupling capacitor, especially the 0.1 μ F ceramic capacitor for high frequency noise should be placed as near to VD (VP, VVD1, VVD2) as possible.

2. Voltage Reference

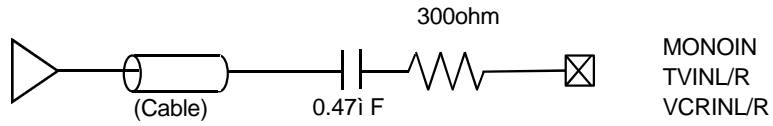
Each VCOM is a signal ground of this chip. An electrolytic capacitor 10 μ F parallel with a 0.1 μ F ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from VCOM pins in order to avoid unwanted coupling into the AK4702.

3. Analog Audio Outputs

The analog outputs are also single-ended and centered on 5.6V(Typ.). The output signal range is typically 2Vrms (typ@VD=5V). The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio pass band. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFFFFH (@18bit) and a negative full scale for 800000H (@18bit). The ideal output is 5.6V(Typ.) for 000000H (@18bit). The DC voltage on analog outputs are eliminated by AC coupling.

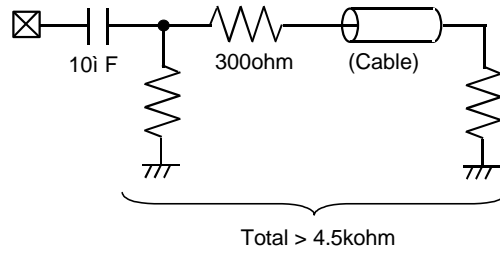
4. External Circuit Example

Analog Audio Input pin

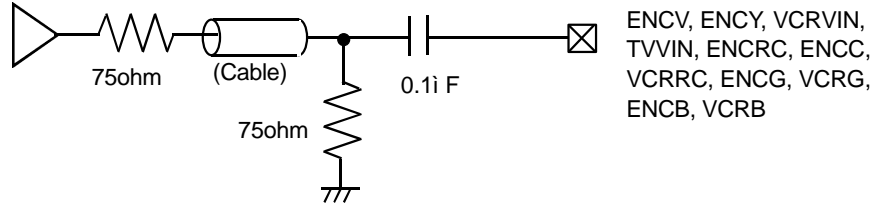


Analog Audio Output pin

MONOOUT
TVOUTL/R
VCROUTL/R

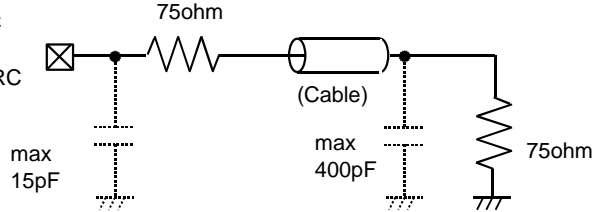


Analog Video Input pin



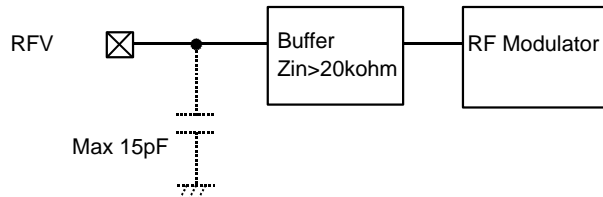
Analog Video Output pin (Except RFV pin)

TVVOUT, TVRC
TVG, TVR
VCRVOUT, VCRC

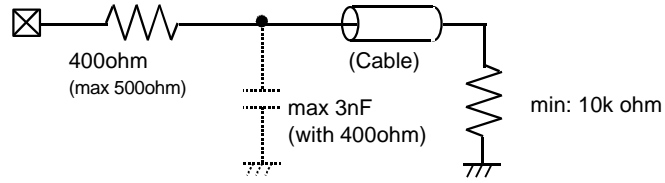


Analog Video Output pin (RFV pin)

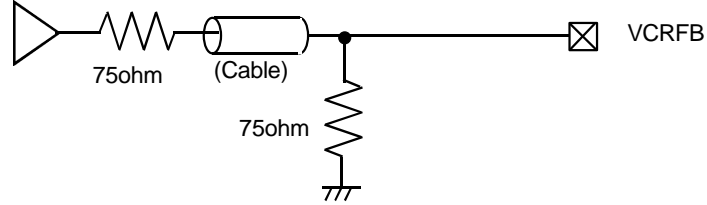
The AK4702 does not have 75ohm driver. Please use an external buffer if the input impedance of the RF modulator is less than 20kohm.



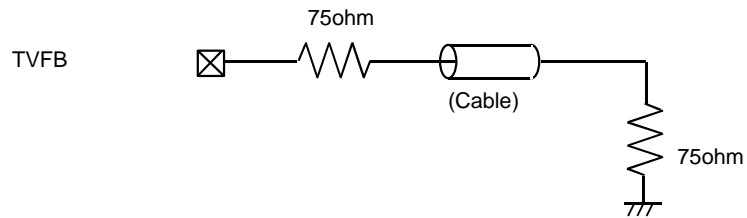
Slow Blanking pin
TVSB
VCRSB



Fast Blanking Input pin

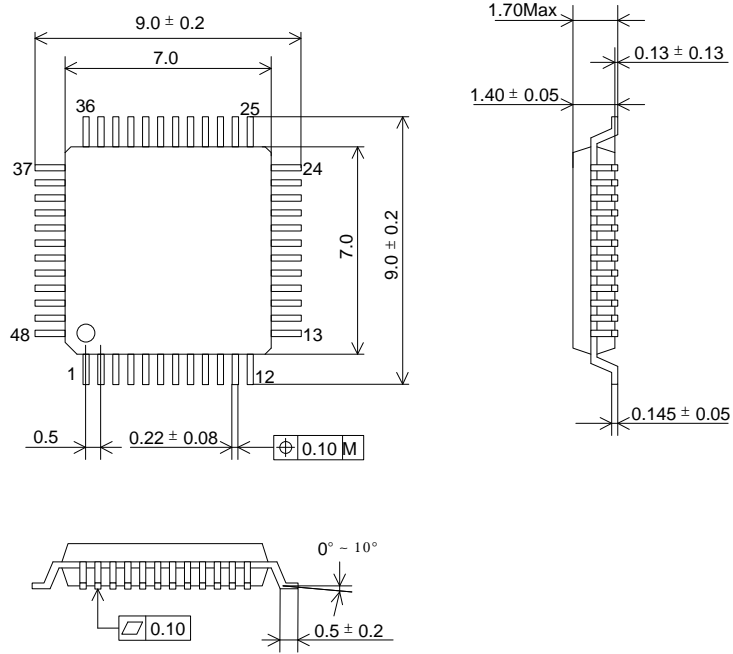


Fast Blanking Output pin



PACKAGE

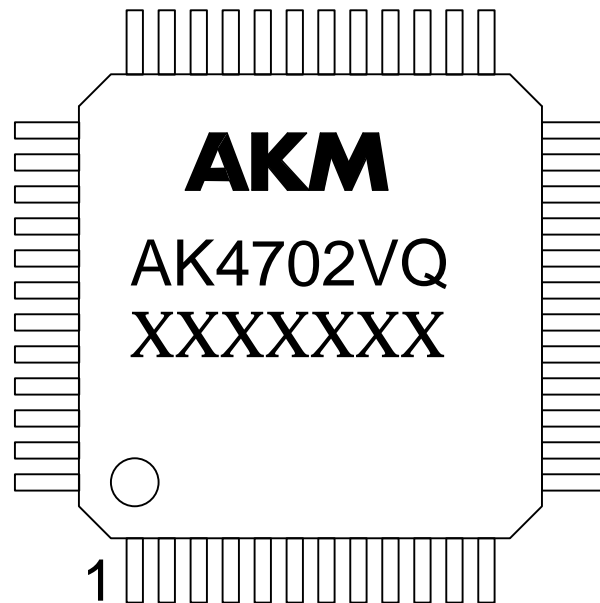
48pin LQFP(Unit:mm)



■ **Package & Lead frame material**

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXXXXXX: Date code identifier

IMPORTANT NOTICE

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