- Preliminary - AK4561
16bit CODEC with built-in ALC and MIC/HP-Amp

GENERAL DESCRIPTION

AK4561 is a 16bit stereo CODEC with a built-in Microphone-Amp, Headphone-Amp. Input circuits include Microphone/LINE inputs selector, power supply for microphone, Pre-Amp, HPF-Amp, EQ-Amp and ALC (Automatic Level Control) circuit, and output circuits include LINEOUT buffer, Analog Volume and Headphone-Amp. As Multi-Power-Supply-System can be set a suitable power supply voltage in each block, the AK4561 is compatible with high performance and low power dissipation. The package is a 64pin TQFP, therefore, a new system can be a smaller board area than a current system is composed of 2 or 3 chips.

FEATURE

1. **Resolution: 16bits**
2. **Recording Function**
   - **3-Input Selector (Internal MIC, External MIC and LINE)**
   - **MIC-Amp**
     - **Pre-Amp, EQ-Amp, HPF-Amp for wind-noise**
   - **Digital ALC (Automatic Level Control) circuit**
   - **FADEIN/FADEOUT**
   - **Digital Delay circuit**
   - **Digital HPF for offset cancellation (fc=3.7Hz@fs=48kHz)**
3. **Playback Function**
   - **Digital De-emphasis Filter (tc=50/15μs, fs = 32kHz, 44.1kHz and 48kHz)**
   - **LINEOUT Buffer: +2dBV**
   - **Analog Volume**
     - **0dB ~ -50dB, Mute**
   - **Headphone-Amp**
     - **Output Level: -5.5dBV@VA=2.8V, R_L=55Ω**
   - **Monaural Output Buffer**
   - **BEEP Signal Input**
4. **Analog Through Mode**
5. **Power Management**
6. **ADC Characteristics (LINEIN → ALC → ADC)**
   - **S/(N+D): 78dB, DR=S/N: 86dB**
7. **DAC Characteristics (DAC → LINEOUT)**
   - **S/(N+D): 76dB, DR=S/N: 88dB**
8. **Master Clock: 256fs/384fs**
9. **Sampling Rate: 8kHz ~50kHz**
10. **Audio Data Interface Format: MSB-First, 2's compliment (AK4550 Compatible)**
    - **ADC: 16bit MSB justified, DAC: 16bit LSB justified**
11. **Ta = -20 ~ 85°C**
12. **Power Supply**
    - **CODEC, Analog Volume, Headphone-Amp: 2.6 ~ 3.3V (typ. 2.8V)**
    - **LINEOUT: 3.8 ~ 5.5V (typ. 4.5V)**
    - **MIC-Amp: 2.6 ~ 5.0V (typ. 2.8V)**
    - **Digital I/F: 1.8 ~ 3.3V (typ. 2.8V)**
13. **Power Supply Current**
    - **All Circuit Power On: 37mA**
14. **Package: 64pin TQFP, 0.4mm Pitch**

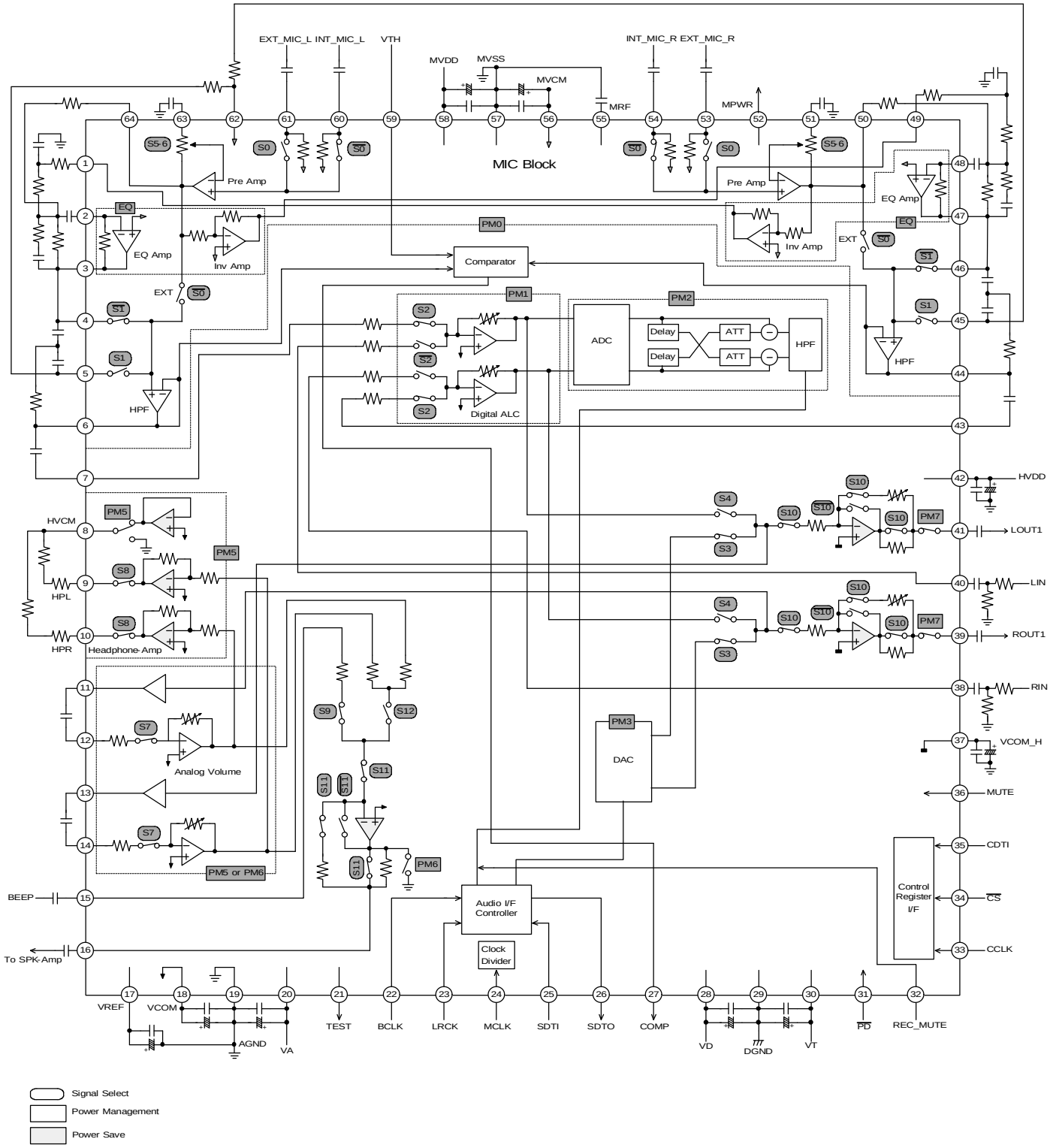
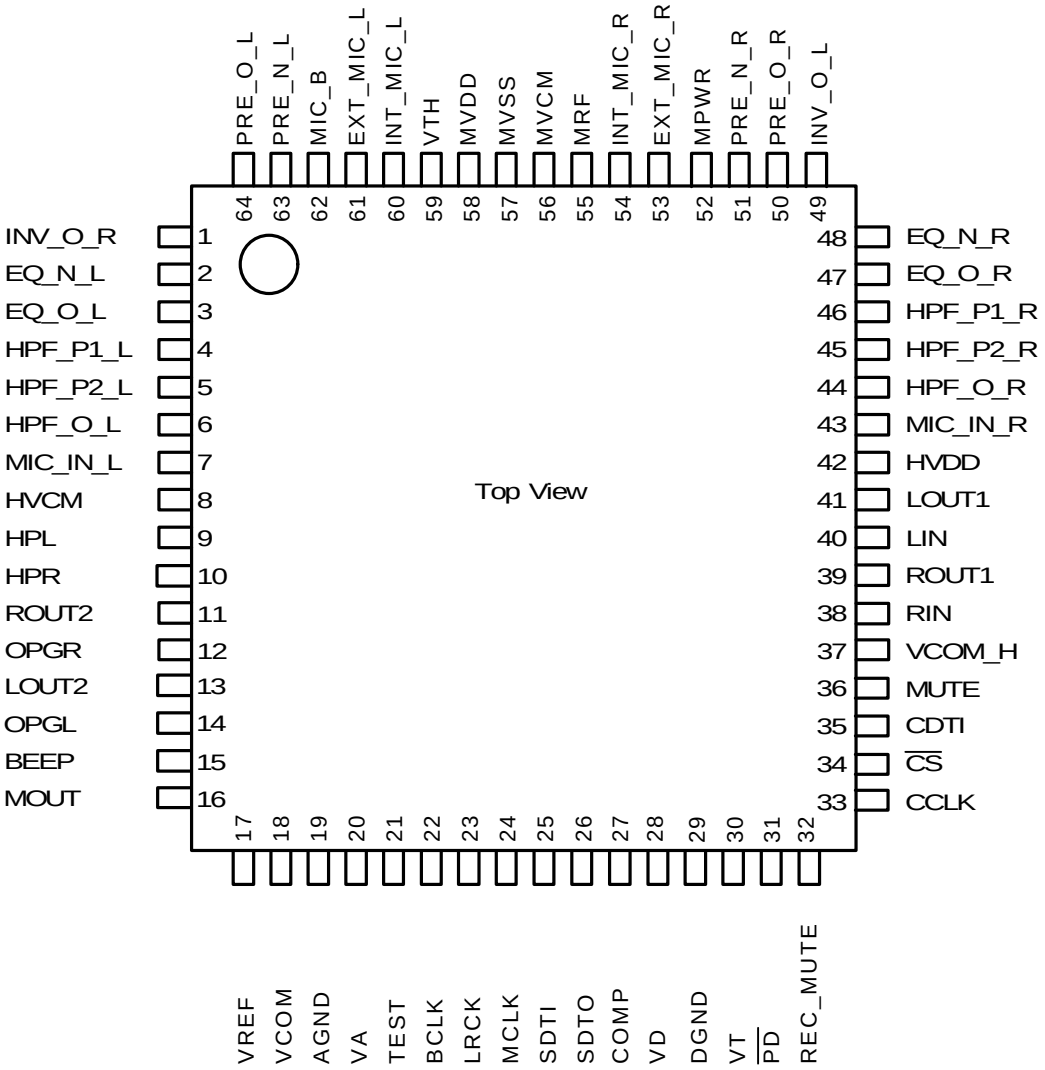


Figure 1. AK4561 Block Diagram

■ Ordering Guide

AK4561VQ	-20 ~ +85 °C	64pin TQFP (0.4mm pitch)
AKD4561	Evaluation Board	

■ Pin layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
Power Supply			
17	VREF	O	ADC, DAC Reference Level, 0.5 x VA
18	VCOM	O	Common Voltage Output Pin, 0.5 x VA
19	AGND	-	Analog Ground Pin
20	VA	-	Analog Power Supply Pin, +2.8V
28	VD	-	Digital Power Supply Pin, +2.8V
29	DGND	-	Digital Ground Pin
30	VT	-	Digital I/F Power Supply Pin, +2.8V
37	VCOM_H	O	LINEOUT Common Voltage Output Pin, 0.5 x HVDD
42	HVDD	-	LINEOUT Power Supply Pin, +4.5V
52	MPWR	O	MIC Power Supply Pin, +2.0V, Idd=3mA(max)
55	MRF	O	MIC Power Supply Ripple Filter Pin
56	MVCM	O	MIC Block Common Voltage Output Pin, 0.5 X MVDD
57	MVSS	-	MIC Block Ground Pin
58	MVDD	-	MIC Block Power Supply Pin
Operation Clock			
22	BCLK	I	Audio Serial Data Clock Pin
23	LRCK	I	Input/Output Channel Clock Pin
24	MCLK	I	Master Clock Input Pin
25	SDTI	I	Audio Serial Data Input Pin
26	SDTO	O	Audio Serial Data Output Pin
MIC Block			
1	INV_O_R	O	Rch Inverter-Amp Output Pin
2	EQ_N_L	I	Lch EQ-Amp Negative Input Pin
3	EQ_O_L	O	Lch EQ-Amp Output Pin
4	HPF_P1_L	I	Lch HPF-Amp Positive #1 Input Pin
5	HPF_P2_L	I	Lch HPF-Amp Positive #2 Input Pin
6	HPF_O_L	O	Lch HPF Output Pin
44	HPF_O_R	O	Rch HPF Output Pin
45	HPF_P2_L	I	Lch HPF-Amp Positive #2 Input Pin
46	HPF_P1_L	I	Lch HPF-Amp Positive #1 Input Pin
47	EQ_O_R	O	Rch EQ-Amp Output Pin
48	EQ_N_R	I	Rch EQ-Amp Negative Input Pin
49	INV_O_L	O	Lch Inverter-Amp Output Pin
50	PRE_O_R	O	Rch Pre-Amp Output Pin
51	PRE_N_R	I	Rch Pre-Amp Negative Input Pin
53	EXT_MIC_R	I	Exteranl MIC Rch Input Pin
54	INT_MIC_R	I	Internal MIC Rch Input Pin
60	INT_MIC_L	I	Internal MIC Lch Input Pin
61	EXT_MIC_L	I	External MIC Lch Input Pin
62	MIC_B	I	MIC-Amp Bias Pin
63	PRE_N_L	I	Lch Pre-Amp Negative Input Pin
64	PRE_O_L	O	Lch Pre-Amp Output Pin

Note: All input pins should not be left floating.

Control Data Interface			
33	CCLK	I	Control Clock Input Pin
34	$\overline{\text{CS}}$	I	Chip Select Pin
35	CDTI	I	Control Data Input Pin
ALC Block			
7	MIC_IN_L	I	Lch MIC Input Pin
38	RIN	I	Rch Line Input Pin
40	LIN	I	Lch Line Input Pin
43	MIC_IN_R	I	Rch MIC Input Pin
DAC			
11	ROUT2	O	Rch #2 Line Output Pin, -5.5dBV@VA=2.8V
13	LOUT2	O	Lch #2 Line Output Pin, -5.5dBV@VA=2.8V
39	ROUT1	O	Rch #1 Line Output Pin, +2dBV@VA=2.8V, VOL=+7.5dB
41	LOUT1	O	Lch #1 Line Output Pin, +2dBV@VA=2.8V, VOL=+7.5dB
Analog Volume			
12	OPGR	I	Rch Analog Volume Input Pin
14	OPGL	I	Lch Analog Volume Input Pin
Headphone Amp			
8	HVCM	O	Headphone-Amp Common Voltage Output Pin
9	HPL	O	Lch Headphone-Amp Output Pin
10	HPR	O	Rch Headphone-Amp Output Pin
Mixer Amp			
16	MOUT	O	Mixing Analog Output Pin
Other Functions			
15	BEEP	I	Beep Signal Input Pin
21	TEST	O	Test pin
27	COMP	O	Comparator Output Pin
31	$\overline{\text{PD}}$	I	Power Down & Reset Pin, “L”: Power-down & Reset, “H”: Normal operation
32	REC_MUTE	I	Rec Mute Pin, “L”: Normal Operation, “H”: ADC Output Data Mute
36	MUTE	I	Mute Pin, “L”: Normal Operation, “H”: Mute
59	VTH	I	Comparator Threshold Voltage Input Pin

Note: All input pins should not be left floating.

ABSOLUTE MAXIMUM RATING

(AGND, DGND, MVSS=0V;Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog 1 (VA pin)	VA	-0.3	6.0	V
	Analog 2 (HVDD pin)	HVDD	-0.3	6.0	V
	MIC (MVDD pin)	MIC	-0.3	6.0	V
	Digital 1 (VD pin)	VD	-0.3	6.0	V
	Digital 2 (VT pin)	VT	-0.3	6.0	V
	| DGND – AGND | (Note 2)	ΔGND1	-	0.3	V
	| MVDD – AGND | (Note 2)	ΔGND2	-	0.3	V
Input Current (Any pines except supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA1	-0.3	VA+0.3	V
(Note 4)		VINA2	-0.3	MIC+0.3	V
Digital Input Voltage (Note 5)		VIND1	-0.3	VD+0.3	V
(Note 6)		VIND2	-0.3	VT+0.3	V
Ambient Temperature		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

Note 2. "DGND and AGND" and "MVSS and AGND" are the same voltage.

Note 3. Analog input pins except EXT_MIC_L, EXT_MIC_R, INT_MIC_L, INT_MIC_R, EQ_N1_L, EQ_N1_R, EQ_N2_L, EQ_N2_R, HPF_P_L, HPF_P_R and MIC_B.

Note 4. EXT_MIC_L, EXT_MIC_R, INT_MIC_L, INT_MIC_R, EQ_N1_L, EQ_N1_R, EQ_N2_L, EQ_N2_R, HPF_P_L, HPF_P_R and MIC_B pins

Note 5. MCLK, LRCK, BCLK and SDTI pins

Note 6. $\overline{\text{CS}}$, CCLK, CDTI, $\overline{\text{PD}}$, REC_MUTE and MUTE pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AGND, DGND, MVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog 1 (VA pin)	VA	2.6	2.8	3.3	V
	Analog 2 (HVDD pin)	HVDD	3.8	4.5	5.5	V
	MIC (MIC pin)	MIC	2.6	2.8	5.0	V
	Digital 1 (VD pin)	VD	2.6	2.8	3.3	V
	Digital 2 (VT pin)	VT	1.8	2.8	3.3	V

Note 1. All voltages with respect to ground.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA=VD=MVDD=VT=2.8V, HVDD=4.5V; AGND=DGND=MVSS=0V; fs=48kHz;
Input Frequency =1kHz; Measurement width=20Hz ~ 20kHz; unless otherwise specified)

Parameter	min	typ	max	Units
Pre-Amp Characteristics:				
Input Resistance: Positive Input Pin (Note 7)		100		kΩ
Negative Input Pin (Note 8)		1.5		kΩ
Maximum Output Voltage (Note 9)			-3.2	dBV
Output Voltage (Input Voltage = -26dBV, Gain = +16dB) (Note 10)		-10		dBV
Step (+12, +16, +20, +24dB)		+4		dB
Load Resistance	2			kΩ
Load Capacitance (Note 11)			20	pF
Inverter-Amp Characteristics: (Gain:0dB)				
Maximum Output Voltage (Note 9)			-3.2	dBV
Load Resistance	3			kΩ
Load Capacitance (Note 11)			20	pF
EQ-Amp Characteristics: (Gain:0dB)				
Maximum Output Voltage (Note 9)			-3.2	dBV
Load Resistance	3			kΩ
Load Capacitance (Note 11)			20	pF
HPF-Amp Characteristics: (Gain: 0dB)				
Maximum Output Voltage (Note 9)			-3.2	dBV
Load Resistance	3			kΩ
Load Capacitance (Note 11)			20	pF
MIC Block Characteristics: Measured via HPF_O_L/HPF_O_R (Note 10)				
S/(N+D) (-10dBV Output) (Note 12)		60		dB
(Note 10)		60		dB
Output Noise Voltage (No signal input, Rg = 1kΩ) (Note 12)		-94		dBV
(Note 10)		-99		dBV
Interchannel Gain Mismatch (Note 12)		0.5		dB
(Note 10)		0.5		dB
Interchannel Isolation (Note 12)		70		dB
(Note 10)		70		dB
MIC Power Supply Characteristics:				
Output Voltage (5kΩ Load)		2.0		V
Output Current			3	mA

Note 7. INT_MIC_L, INT_MIC_R, EXT_MIC_L and EXT_MIC_R pins

Note 8. Gain of Pre-Amp is +16dB. Input resistance of Pre-Amp is changed by gain.
Gain=12dB: 2.4k ± 30%Ω, Gain=20dB: 950 ± 30%Ω, Gain=24dB: 600 ± 30%Ω

Note 9. Maximum output voltage is typically (MVDD x 0.7) V.

Note 10. Pre-Amp(Gain:+16dB) → HPF-Amp (Gain:0dB, HPF OFF)

Note 11. When output pin drives some capacitive load, some resistor should be added in series between output pin and capacitive load.

Note 12. Pre-Amp (Gain: +16dB) → Inverter-Amp (Gain: +0dB) → EQ-Amp (Input/Feedback resistance: 5kΩ) → HPF-Amp (Gain: 0dB, HPF OFF)

Parameter			min	typ	max	Units
ALC Characteristics (IPGA):						
Maximum Input Voltage (Note 13)					-0.5	dBV
Input Resistance:						
MIC(MIC_IN_L,MIC_IN_R pins) (Note 14)			5.6	9	13	kΩ
LINE(LIN, RIN pins) (Note 15)			117	184	260	kΩ
Step Size	MIC	LINE				
	+26dB ~ -10dB	+0dB ~ -36dB	0.1	0.5		dB
	-10dB ~ -18dB	-36dB ~ -44dB	0.1	1		dB
	-18dB ~ -30dB	-44dB ~ -56dB	0.1	2		dB
	-30dB ~ -42dB	-56dB ~ -68dB	-	2	-	dB
	-42dB ~ -54dB	-68dB ~ -80dB	-	4	-	dB
ADC Analog Input Characteristics: Input from LIN/RIN, ALC = OFF, IPGA = 0dB						
Resolution					16	Bits
Input Voltage (Note 16)				-5.5		dBV
S/(N+D)(-0.5dBFS Output)				78		dB
DR (-60dBFS Output, A-Weighted)				86		dB
S/N (A-Weighted)				86		dB
Interchannel Isolation				80		dB
Interchannel Gain Mismatch				0.5		dB
DAC Analog Characteristics: Measured via LOUT1/ROUT1, VOL=+7.5dB						
Resolution					16	Bits
S/(N+D) (0dBFS Input)				76		dB
DR (-60dBFS Input, A-Weighted)				88		dB
S/N (A-Weighted)				88		dB
Output Voltage (Note 16)				+2		dBV
Interchannel Isolation				80		dB
Interchannel Gain Mismatch				0.5		dB
Load Resistance			10			kΩ
Load Capacitance (Note 17)					20	pF
Analog Volume Characteristics (OPGA):						
Input Resistance (OPGL,OPGR pins) (Note 18)			44	110	205	kΩ
Step Size: +0dB ~ -16dB			0.1	1		dB
-16dB ~ -38dB			0.1	2		dB
-38dB ~ -50dB			-	4	-	dB
BEEP Input: (BEEP pin)						
Maximum Input Voltage (Note 16)					-5.5	dBV
Input Resistance				50		kΩ

Note 13. When the ALC operation is enabled, maximum input voltage becomes typically (VA – 0.1V) Vpp.
2.7Vpp = -0.5dBV @VA=2.8V

Note 14. Input resistance of MIC changes from 8kΩ to 10kΩ by setting GAIN value, typically.

Note 15. Input resistance of LINE changes from 168kΩ to 200kΩ by setting GAIN value, typically.

Note 16. Input/Output voltage is proportional to VA voltage. 0.54 x VA.

Note 17. When output pin drives some capacitive load, some resistor should be added in series between output pin and capacitive load.

Note 18. Input resistance of OPGA changes from 63kΩ to 158kΩ by setting GAIN value, typically.

Parameter	min	typ	max	Units
Headphone-Amp Characteristics: R_L= 47 + 8Ω (Note 19)				
Output Voltage (-5.5dBV Input) (Note 16)		-5.5		dBV
S/(N+D) (-5.5dBV Output)		40		dB
Output Noise Voltage (OPGA=MUTE, A-Weighted)		-86		dBV
Interchannel Isolation		40		dB
Interchannel Gain Mismatch		0.5		dB
Load Resistance	55			Ω
Load Capacitance (Note 17)			20	pF
Monaural Output: (MOUT pin) (Note 20)				
Output Voltage (-5.5dBV Input) (Note 21)		-11.5		dBV
S/(N+D) (-5.5dBV Output)		80		dB
S/N (A-weighted)		90		dB
Load Resistance	5			kΩ
Load Capacitance (Note 17)			20	pF
Power Supply Current				
Power Up ($\overline{PD}$ = "H")				
All Circuit Power-Up: (PM7-0 bit all "1")				
VA: Headphone-Amp No input (S8 = "1")		21		mA
VD+VT: (DLYE bit = "1")		5		mA
MVDD: (Note 22)		9		mA
HVDD: (S10 = "1") (Note 23)		3		mA
ALC + ADC: (PM4=PM2=PM1= "1") (Note 23)				
VA:		9		mA
VD+VT: (DLYE bit = "1")		4		mA
HVDD	-	0.5	-	mA
DAC + OPGA + MOUT + LINEOUT: (PM7=PM6=PM4=PM3= "1") (Note 23)				
VA:		10		mA
VD+VT:		2		mA
HVDD: LINEOUT Normal Operation (S10 = "1")		2		mA
LINEOUT Power-Save-Mode (S10 = "0")	-	0.2	-	mA
DAC + OPGA+ MOUT + LINEOUT + HP-Amp: (PM7=PM6=PM5=PM4=PM3= "1") (Note 23)				
VA: Headphone-Amp Normal Operation (S8 = "1"), No Input		14		mA
Headphone-Amp Power-Save-Mode (S8 = "0")	-	11	-	mA
VD+VT:		2		mA
HVDD: (S10 = "1")	-	2	-	mA
Power Down ($\overline{PD}$ = "L")				
VA+VD+HVDD+MVDD (Note 24)		200		μA

Note 19. Input from OPGL and OPGR pins. Analog Volume (OPGA=0dB) → Headphone Amplifier
Note 20. Input from OPGL and OPGR pins. Analog Volume (OPGA=0dB) → Monaural Amplifier
Note 21. Lch = -5.5dBV, Rch = no input or Rch = -5.5dBV, Lch = no input
Note 22. MPWR pin supplies 0mA.
Note 23. Then power supply current of MVDD is 0.2mA (typ.).
Note 24. In case of power-down, digital input pins of MCLK, BCLK, LRCK and SDTI are held "VD" or "DGND". Digital input pins of CCLK, REC_MUTE, CCLK, $\overline{CS}$, CDTI and MUTE are held "VT" or "DGND". $\overline{PD}$ pin is held "DGND".

FILTER CHARACTERISTICS

(Ta=25°C; VA=VD=2.6 ~ 3.3V; fs=48kHz; De-emphasis = OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (LPF):						
Passband (Note 25)	±0.1dB	PB	0		18.9	kHz
	-1.0dB		-	21.8	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband (Note 25)		SB	29.4			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 26)		GD	-	17.0	-	1/fs
Group Delay Distortion		ΔGD		0		us
ADC Digital Filter (HPF):						
Frequency Response (Note 25)	-3.0dB	FR	-	3.7	-	Hz
	-0.56dB		-	10	-	Hz
	-0.15dB		-	20	-	Hz
DAC Digital Filter:						
Passband (Note 25)	±0.1dB	PB	0		21.7	kHz
	-6.0dB		-	24.0	-	kHz
Stopband (Note 25)		SB	26.2			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 26)		GD	-	14.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response	0 ~ 20.0kHz	FR		±0.5		dB

Note 25. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.454*fs (@-1.0dB), DAC is PB=0.454*fs (@-0.1dB).

Note 26. The calculating delay time which occured by digital filtering, This time is from the input of analog signal to setting the 16 bit data of both channels on input register to the output register of ADC. And this time include group delay of HPF. For DAC, this time is from setting the 16 bit data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25°C; VA=VD=2.6 ~ 3.3V; VT=1.8 ~ 3.3V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (Note 27)	VIH	1.5	-	-	V
Low-Level Input Voltage (Note 27)	VIL	-	-	0.6	V
High-Level Output Voltage (Note 28) Iout=-200μA	VOH1	VD-0.2	-	-	V
Low-Level Output Voltage (Note 28) Iout=200μA	VOL1	-	-	0.2	V
High-Level Output Voltage (Note 29)	VOH2	75%VT	-	-	V
Low-Level Output Voltage (Note 29)	VOL2	-	-	25%VT	V
Input Leakage Current	Iin	-	-	±10	μA

Note 27. MCLK, BCLK, LRCK and SDTI pins

Note 28. SDTO and COMP pins

Note 29. $\overline{\text{CS}}$, CCLK, CDTI, $\overline{\text{PD}}$, REC_MUTE and MUTE pins

SWITCHING CHARACTERISTICS

(Ta=25°C; VA=VD=2.6 ~ 3.3V; VT=1.8 ~ 3.3V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock(MCLK) 256fs: Frequency	fCLK	2.048	12.288	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs: Frequency	fCLK	3.072	18.432	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
Channel Select Clock (LRCK): Frequency	fs	8	48	50	kHz
Duty	Duty	45	50	55	%
Audio Interface Timing					
BCLK Period	tBLK	312.5			ns
BCLK Pulse Width Low	tBLKL	130			ns
Pulse Width High	tBLKH	130			ns
LRCK Edge to BCLK "↑" (Note 30)	tLRB	50			ns
BCLK "↑" to LRCK Edge (Note 30)	tBLR	50			ns
LRCK to SDTO(MSB) Delay Time	tLRM			80	ns
BCLK "↓" to SDTO Delay Time	tBSD			80	ns
SDTI Latch Hold Time	tSDH	50			ns
SDTI Latch Set up Time	tSDS	50			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Latch Set Up Time	tCDS	50			ns
CDTI Latch Hold Time	tCDH	50			ns
$\overline{CS}$ "H" Time	tCSW	150			ns
$\overline{CS}$ "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to $\overline{CS}$ "↑"	tCSH	50			ns
Reset Timing					
$\overline{PD}$ Pulse Width	tPDW	150			ns
$\overline{PD}$ "↑" to SDTO Delay Time (Note 31)	tPDV		8224		1/fs

Note 30. BCLK rising edge must not occur at the same time as LRCK edge.

Note 31. These cycles are the numbers of LRCK rising from PDN pin rising.

■ Timing Diagram

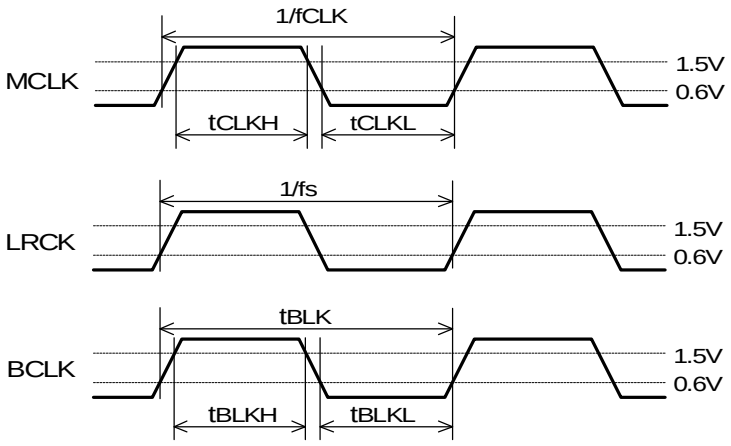


Figure 2. Clock Timing

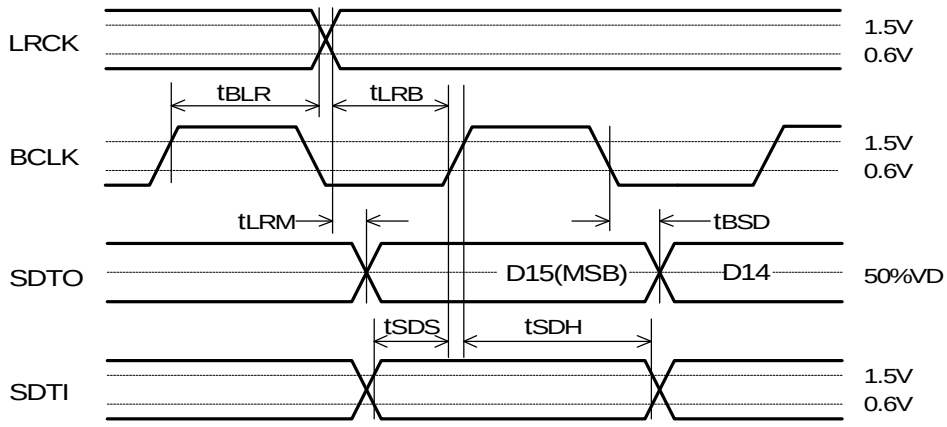


Figure 3. Audio Data Input/Output Timing

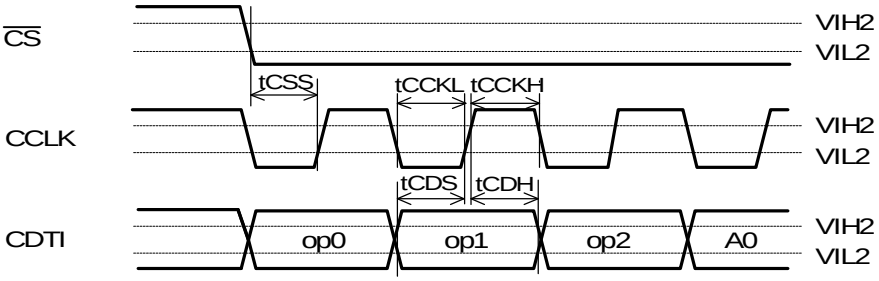


Figure 4. WRITE Command Input Timing 1

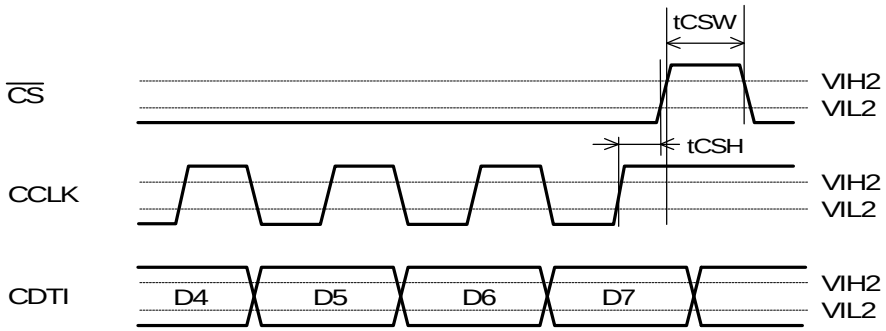


Figure 5. WRITE Data Input Timing 2

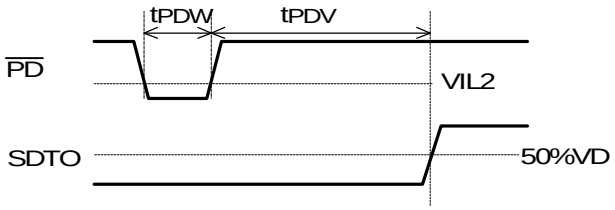


Figure 6. Reset Timing

OPERATION OVERVIEW

■ System Clock

The clock which are required to operate are MCLK (256fs/384fs), LRCK (fs), BCLK (32fs~). The master clock (MCLK) should be synchronized with LRCK but the phase is free of care.
The MCLK can be input 256fs or 384fs. When 384fs is input, the internal master clock is divided into 2/3 automatically.
* fs is sampling frequency.

When the synchronization is out of phase by changing the clock frequencies during normal operation, the AK4561 may occur click noise. In case of DAC, click noise is avoided by setting the inputs to "0".

All external clocks (MCLK, BCLK and LRCK) should always be present. If these clocks are not provided, the AK4561 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4561 should be in the power-down mode. (Refer to the "Power Management Mode".)

■ System Reset

AK4561 should be reset once by bringing $\overline{\text{PD}}$ pin "L" upon power-up. After the system reset operation, the all internal AK4561 registers become initial value.

Initializing cycle is 8224/fs=171.3ms@fs=48kHz. During initializing cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". Output data of ADC settles data equivalent for analog input signal after initializing cycle. This cycle is not for DAC.

As a normal initializing cycle may not be executed, nothing writes at address 02H during initializing cycle.

■ Digital High Pass Filter

The ADC has HPF for the DC offset cancel. The cut-off frequency of HPF is 3.7Hz (@fs=48kHz) and it is -0.15dB at 22Hz. It also scales with the sampling frequency (fs).

■ Audio Interface Format

Data is shifted in/out the SDTI/SDTO pins using BCLK and LRCK inputs. The serial data is MSB-first, 2's compliment format, ADC is MSB justified and DAC is LSB justified.

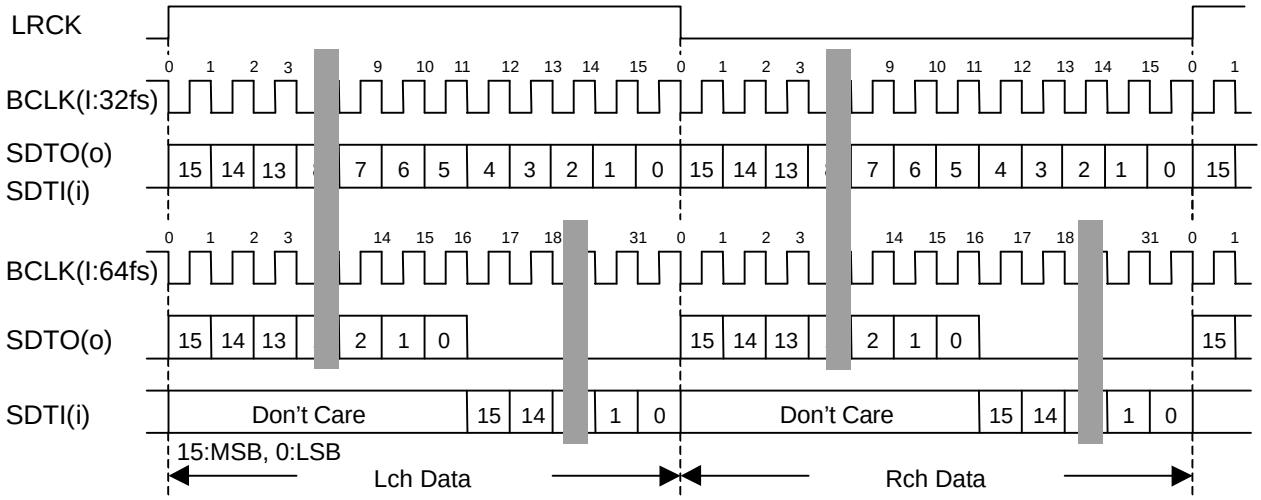


Figure 7. Audio Data Timing

■ Control Register Timing

The data on the 3-wire serial interface consists of op-code (3bit), address (LSB-first, 5bit) and control data (LSB-first, 8bit). The Transmitting data is output to each bit by "↓" of CCLK, the receiving data is latched by "↑" of CCLK. Writing data becomes effective by "↑" of $\overline{CS}$. $\overline{CS}$ should be held to "H" at no access.

CCLK always need 16 edges of "↑" during $\overline{CS}$ = "L" Address except 00H~0BH are inhibited.
Writing of the control registers are invalid when op2-0 bits are except "111".

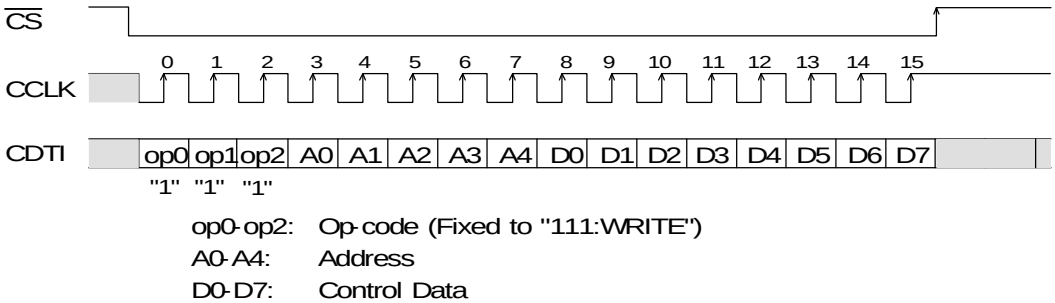


Figure 8. Control Data Timing

■ Register Map

The following registers are reset at $\overline{PD}$ pin = "L", then inhibits writing.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Signal Select 1	EQ	S6	S5	S4	S3	S2	S1	S0
01H	Signal Select 2	0	0	S12	S11	S10	S9	S8	S7
02H	Power Management Control	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
03H	Mode Control	FS	VOL2	VOL1	VOL0	MONO1	MONO0	DEM1	DEM0
04H	Timer Select	FDTM1	FDTM0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
05H	ALC Mode Control 1	0	0	ZELM	LMAT1	LMAT0	FDATT	RATT	LMTH
06H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
07H	Operation Mode	0	0	FR	COMP	0	FDIN	FDOUT	ALC
08H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
09H	Output PGA Control	0	0	0	OPGA4	OPGA3	OPGA2	OPGA1	OPGA0
0AH	Digital Delay 1	DLYE	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
0BH	Digital Delay 2	0	0	0	0	COE3	COE2	COE1	COE0

Table 1. AK4561 Register Map

Signal Select 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Signal Select 1	EQ	S6	S5	S4	S3	S2	S1	S0
RESET		1	0	1	0	1	0	0	0

S0: Select Internal / External MIC (Refer to Figure 11 and Figure 12)
- 0: Internal MIC (RESET)
- 1: External MIC

S1: Select HPF-Amp
- 0: Disable (RESET)
- 1: Enable

When S1 bit is "0", HPF-Amp becomes a unity gain buffer.
When External MIC (S0 bit = "1") is selected, S1 bit is ignored.

S2: Select input signal of ALC and change gain table of IPGA.
- 0: MIC (RESET)
- 1: LINE

S4-3: Select input signal of LINEOUT or Analog Volume (OPGA)

ON/OFF of DAC is selected by S3 bit, and ON/OFF of Analog Through Mode is selected by S4 bit.
- 00: All input signals are OFF. Then output voltage becomes common voltage.
- 01:DAC (RESET)
- 10: Analog Through Mode (Output signal of ALC)
- 11: Output signal of DAC and Analog Through are mixed.

S6-5: Select gain of Pre-Amp; +12dB ~ +24dB; 4dB step

S6	S5	Gain	
0	0	+12dB	
0	1	+16dB	RESET
1	0	+20dB	
1	1	+24dB	

Table 2. Pre-Amp Gain Table

EQ: Power management of EQ-Amp and Inverter-Amp
- 0: OFF. EQ-Amp and Inverter-Amp are always powered-down, then EQ bit is not relative.
- 1: ON. EQ-Amp and Inverter-Amp are powered-up/down by PM0 bit. (RESET)

Note: Pop noise may occur when EQ or S6-0 bits are changed.

Signal Select 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Signal Select 2	0	0	S12	S11	S10	S9	S8	S7
RESET		0	0	0	1	0	1	0	0

S7: Select input signal of analog volume (OPGA)
0: OFF. OPGA output voltage becomes VCOM voltage (RESET)
1: ON. OPGA is provided to the signal selected by S4-3 bits (DAC or Analog Through Mode).

S8: Select output signal of Headphone-Amp
0: OFF. Power-Save-Mode. HPL/HPR pins become Hi-z and HVCM pin is provided to VCOM voltage. (RESET)
1: ON

S9: Select input signal of BEEP
0: OFF
1: ON (RESET)

S10: Select LINEOUT
0: OFF (RESET)
Power-Save-Mode. LINEOUT is provided to VCOM_H voltage.
1: ON

S11: Select monaural output (Mixing = (L+R)/2)
0: OFF (RESET)
Power-Save-Mode, monaural output is provided to VCOM voltage.
1: ON

S12: Select monaural input
0: OFF (RESET)
1: ON. Output signal of analog volume is provided to monaural amplifier.

Note:
S7: When S7 bit changes from “1” to “0”, the pop noise can not occur. When S7 bit changes from “0” to “1” and S12-8 bits are changed, the pop noise occurs.

Power Management Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management Control	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
RESET		1	1	1	1	1	1	1	1

PM0: MIC Block (Pre-Amp, EQ-Amp, HPF-Amp and MPWR) Power Control.
0: OFF. Output pins are Hi-z.
1: ON. In case of EQ bit = "0", EQ-Amp is powered-down. (RESET)

PM1: IPGA (ALC) Power Control
0: OFF
1: ON (RESET)

PM2: ADC Power Control
0: OFF. SDTO pin becomes "L".
1: ON (RESET)
When ADC bit changes from "0" to "1", initializing cycle (8224/fs=171.3ms@fs=48kHz) starts. Digital data of ADC is generated after initializing cycle.

PM3: DAC Power Control
0: OFF
1: ON (RESET)

PM4: Common Voltage (VCOM, VCOM_H and MVCM) Power Control
0: OFF
1: ON (RESET)

PM5: Headphone Amplifier Power Control
0: OFF. HPL/HPR pins become Hi-z and HVCM pin becomes "L" (AGND).
1: ON (RESET)

PM6: MOUT Power Control
0: OFF. MOUT pin becomes Hi-z.
1: ON (RESET)

PM7: LINEOUT Power Control
0: OFF. Output pins become Hi-z.
1: ON (RESET)

Analog volume (OPGA) are enabled when PM6 bit = "1" or PM5 bit = "1".
These bits can be partially powered-down by ON/OFF ("1" / "0"). When $\overline{\text{PD}}$ pin goes "L", all the circuit in AK4561 can be powered-down regardless of these bits in the address.

When bit in this address goes all "0", all the circuits in AK4561 can be also powered-down. But contents of registers are kept.

When each block is operated, PM4 bit must go "1". PM4 bit can write "0" when all bits in this address can be "0".

Except the case of PM6=PM5=PM3=PM2=PM1= "0" or $\overline{\text{PD}}$ pin = "L", MCLK, BCLK and LRCK should not be stopped.

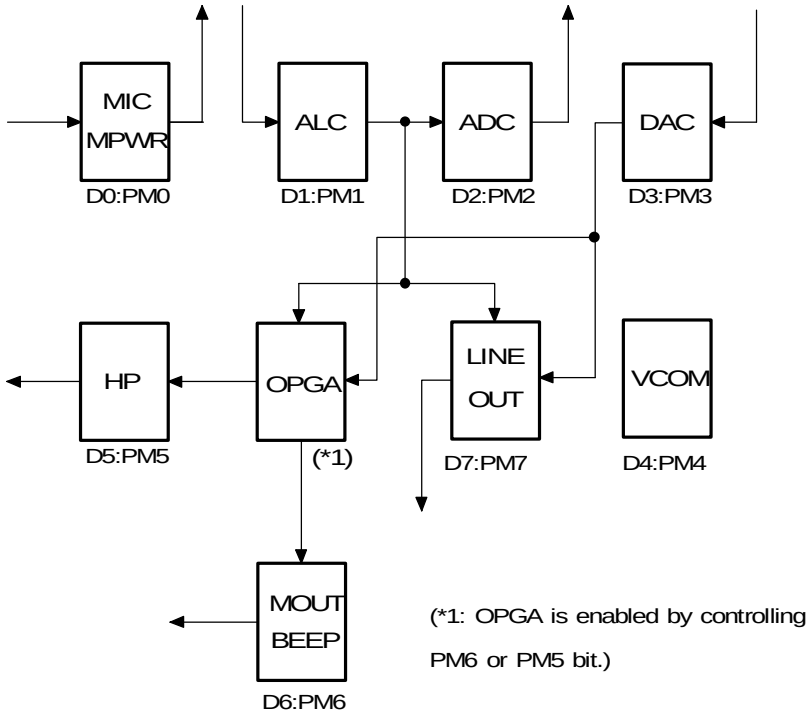


Figure 9. Power Management Control

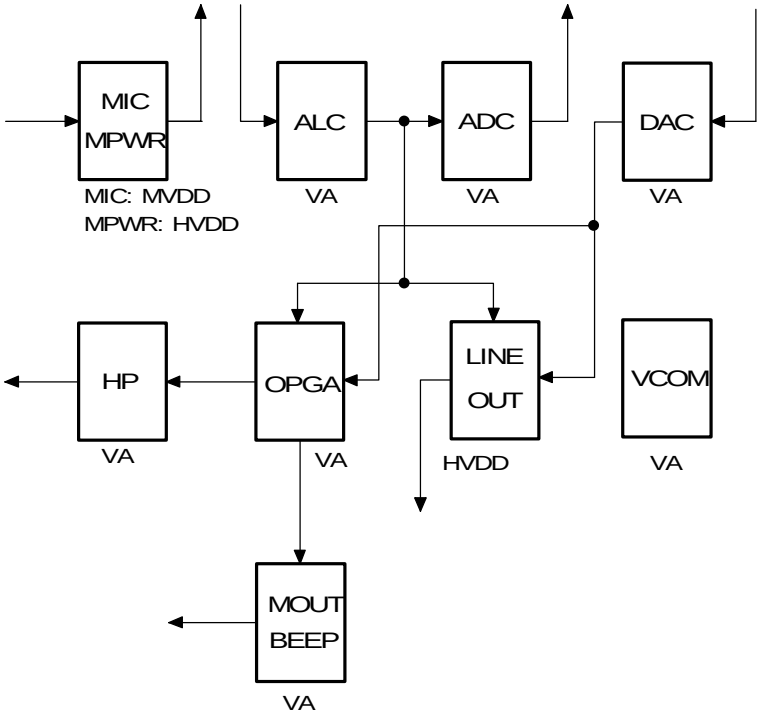


Figure 10. Analog Power Supply Source of Each Block

Mode Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control	FS	VOL2	VOL1	VOL0	MONO1	MONO0	DEM1	DEM0
RESET		1	0	1	0	0	0	0	1

DEM1-0: Select De-emphasis Frequency

The AK4561 includes the digital de-emphasis filter (tc = 50/15μs) by IIR filter. The filter corresponds to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter selected DEM0 and DEM1 registers are enabled for input audio data.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	RESET
1	0	48kHz	
1	1	32kHz	

Table 3. De-emphasis Frequencies

MONO1-0: Select digital data of DAC

MONO1	MONO0	LOUT	ROUT	
0	0	Lch	Rch	RESET
0	1	Lch	Lch	
1	0	Rch	Rch	
1	1	Rch	Lch	

Table 4. Select digital data of DAC

VOL2-0: LINEOUT Gain Setting

As signal level of LINEOUT is different by VA power supply voltage, a gain of LINEOUT is set by VOL2-0 bits.

VOL2	VOL1	VOL0	Gain	VA Voltage	
0	0	0	+8.1dB	2.60 ~ 2.65V	
0	0	1	+7.8dB	2.65 ~ 2.75V	
0	1	0	+7.5dB	2.75 ~ 2.85V	RESET
0	1	1	+7.2dB	2.85 ~ 2.95V	
1	0	0	+6.9dB	2.95 ~ 3.05V	
1	0	1	+6.6dB	3.05 ~ 3.15V	
1	1	0	+6.3dB	3.15 ~ 3.25V	
1	1	1	+6.0dB	3.25 ~ 3.30V	

Table 5. LINEOUT volume setting

FS: Select Sampling Frequency

0:fs=32kHz

1:fs=48kHz (RESET)

Recovery period (WTM1-0 bit), zero crossing timeout (ZTM1-0 bit) and FADEIN/FADEOUT period (FDTM1-0 bit), which can set the same period at fs=32kHz and 48kHz.

Timer Select

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Timer Select	FDTM1	FDTM0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
RESET		1	0	1	0	1	0	0	0

LTM1-0: ALC limiter operation period at zero crossing disable (ZELM = "0")

The IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period specified by LTM1-0 bits.

LTM1	LTM0		ALC Limiter Operation Period			
			48kz	44.1kHz	32kHz	
0	0	1/fs	21μs	23μs	31μs	RESET
0	1	2/fs	42μs	45μs	63μs	
1	0	4/fs	83μs	91μs	125μs	
1	1	8/fs	167μs	181μs	250μs	

Table 6. ALC Limiter Operation Period at zero crossing disable (ZELM = "0")

WTM1-0: ALC Recovery Waiting Period

A period of recovery operation when any limiter operation does not occur during ALC operation. Recovery operation is done at period set by WTM1-0 bits.

When the input signal level exceeds auto recovery waiting counter reset level set by LMTH bit, the auto recovery waiting counter is reset.

The waiting timer starts when the input signal level becomes below the auto recovery waiting counter reset level.

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

WTM1	WTM0	Period	
0	0	16.0ms	
0	1	32.0ms	
1	0	64.0ms	RESET
1	1	128.0ms	

Table 7. ALC Recovery Operation Waiting Period

ZTM1-0: Zero crossing timeout at writing operation by μP and ALC recovery operation and the zero crossing enable (ZELM= "1") of the ALC operation

When IPGA of each L/R channels do zero crossing or timeout independently, the IPGA value is changed by μP WRITE operation or ALC recovery operation or ALC limiter operation (ZELM = "1").

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

ZTM1	ZTM0	Period	
0	0	16.0ms	
0	1	32.0ms	
1	0	64.0ms	RESET
1	1	128.0ms	

Table 8. Zero Crossing Timeout

FDTM1-0: FADEIN/OUT Cycle Setting

The FADEIN/OUT operation is done by a period set by FDTM1-0 bits when FDIN or FDOUT bits are set to "1". When IPGA of each L/R channel do zero crossing or timeout independently, the IPGA value is changed.

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

FDTM1	FDTM0	Period	
0	0	16.0ms	
0	1	32.0ms	
1	0	64.0ms	RESET
1	1	128.0ms	

Table 9. FADEIN/OUT Period

ALC Mode Control 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	ALC Mode Control 1	0	0	ZELM	LMAT1	LMAT0	FDATT	RATT	LMTH
RESET		0	0	0	0	0	0	0	0

LMTH: ALC Limiter Detection Level / Recovery Waiting Counter Reset Level

LMTH	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	ADC Input ≥-5.0dB	-5.0dB > ADC Input ≥ -7.0dB	RESET
1	ADC Input ≥ -3.0dB	-3.0dB > ADC Input ≥ -5.0dB	

Table 10. ALC Limiter Detection Level / Recovery Waiting Counter Reset Level

RATT: ALC Recovery GAIN Step

During the ALC Recovery operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is 30H, RATT = "1" is set, IPGA changes to 32H by the ALC recovery operation, the input signal level is gained by 1dB (=0.5dB x 2).
When the IPGA value exceeds the reference level (REF6-0), the IPGA value does not increase.

RATT	GAIN STEP	
0	1	RESET
1	2	

Table 11. ALC Recovery GAIN Step Setting

FDATT: FADEIN/OUT ATT Step

During the FADEIN/OUT operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is 30H, FDATT = "1" is set, IPGA changes to 32H(at FADEIN operation) or 2EH (at FADEOUT operation) by the FADEIN/OUT operation, the input signal level is changed by 1dB (=0.5dB x 2).
When the IPGA value exceeds the reference level (REF6-0), the IPGA value does not increase.

FDATT	ATT STEP	
0	1	RESET
1	2	

Table 12. FADEIN/OUT ATT Step Setting

LMAT1-0: ALC Limiter ATT Step

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level set by LMTH, the number of steps attenuated from current IPGA value is set. For example, when the current IPGA value is 68H in the state of LMAT1-0 bit = "11", it becomes IPGA = 64H by the ALC limiter operation, the input signal level is attenuated by 2dB (=0.5dB x 4).
When the attenuation value exceeds IPGA = "00" (MUTE), it clips to "00".

LMAT1	LMAT0	ATT STEP	
0	0	1	RESET
0	1	2	
1	0	3	
1	1	4	

Table 13. ALC Limiter ATT Step Setting

ZELM: Enable zero crossing detection at ALC Limiter operation

0: Disable (RESET)
1: Enable

In case of ZELM = "1", IPGA of each L/R channel do zero crossing or timeout independently, the IPGA value is changed by ALC operation. Zero crossing timeout is the same as ALC recovery operation. In case of ZELM = "0", the IPGA value is changed immediately.

ALC Mode Control 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
RESET		0	1	1	0	0	0	0	0

REF6-0: Set the Reference value at ALC Recovery Operation

During the ALC recovery operation, if the IPGA value exceeds the setting reference value by Gain operation, IPGA does not become the larger than the reference value.

For example, when REF=30H, RATT=2, IPGA=2FH and IPGA will become 2FH + 2step = 31H by the ALC recovery operation, but the IPGA value becomes 30H as REF value is 30H.

	DATA	GAIN(dB)		STEP	LEVEL
		MIC	LINE		
RESET	60H	+26.0	+0.0	0.5dB	73
	5FH	+25.5	-0.5		
	5EH	+25.0	-1.0		
	•	•	•		
	2CH	+0.0	-26.0		
	2BH	-0.5	-26.5		
	•	•	•		
	19H	-9.5	-35.5		
	18H	-10.0	-36.0		
	17H	-11.0	-37.0	1dB	8
	16H	-12.0	-38.0		
	•	•	•		
	11H	-17.0	-43.0		
	10H	-18.0	-44.0		
	0FH	-20.0	-46.0	2dB	12
	0EH	-22.0	-48.0		
	•	•	•		
	05H	-40.0	-66.0		
	04H	-42.0	-68.0		
	03H	-46.0	-72.0	4dB	3
	02H	-50.0	-76.0		
	01H	-54.0	-80.0		
	00H	MUTE	MUTE		1

Table 14. Setting Reference Value at ALC Recovery Operation

Operation Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Operation Mode	0	0	FR	COMP	0	FDIN	FDOUT	ALC
RESET		0	0	0	0	0	0	0	0

ALC: ALC Enable Flag
0: Disable (RESET)
1: Enable
FDOUT: FADEOUT Enable Flag
0: Disable (RESET)
1: Enable
FDIN: FADEIN Enable Flag
0: Disable (RESET)
1: Enable

* When FADEIN or FADEOUT operation is done, ALC bit should always be “1”.

COMP: Comparator Output Data
0: OFF. COMP pin goes “L”. (RESET)
1: ON. COMP pin generates the analog signal compared from HPF-Amp.
FR: Select ALC operation Mode
0: The ALC operation corresponds to impulse noise. (RESET)
1: The ALC operation is the same as AK4516A.

Input PGA Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
RESET		0	0	1	0	1	1	0	0

IPGA6-0: Input Analog PGA; 97Levels

DATA	GAIN(dB)		STEP	LEVEL
	MIC	LINE		
60H	+26.0	+0.0	0.5dB	73
5FH	+25.5	-0.5		
5EH	+25.0	-1.0		
•	•	•		
RESET 2CH	+0.0	-26.0		
2BH	-0.5	-26.5		
•	•	•		
19H	-9.5	-35.5		
18H	-10.0	-36.0		
17H	-11.0	-37.0	1dB	8
16H	-12.0	-38.0		
•	•	•		
11H	-17.0	-43.0		
10H	-18.0	-44.0		
0FH	-20.0	-46.0	2dB	12
0EH	-22.0	-48.0		
•	•	•		
05H	-40.0	-66.0		
04H	-42.0	-68.0		
03H	-46.0	-72.0	4dB	3
02H	-50.0	-76.0		
01H	-54.0	-80.0		
00H	MUTE	MUTE		1

Table 15. Input Gain Setting

Output PGA Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Output PGA Control	0	0	0	OPGA4	OPGA3	OPGA2	OPGA1	OPGA0
RESET		0	0	0	1	1	1	1	1

OPGA4-0: Output analog PGA; 32 Level; 0dB ~ -50dB, Mute.

These bits can change volume of Headphone-Amp and Monaural-Amp.

This volume includes zero crossing detection, and it does L/R channels independently. Zero crossing timeout is 32ms.

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

	DATA	GAIN(dB)	STEP	LEVEL
RESET	1FH	+0	1dB	17
	1EH	-1		
	1DH	-2		
	•	•		
	10H	-15		
	0FH	-16		
	0EH	-18	2dB	11
	0DH	-20		
	•	•		
	05H	-36		
	04H	-38		
	03H	-42	4dB	3
	02H	-46		
	01H	-50		
	00H	Mute		1

Table 16. ATT value of Analog Volume

Digital Delay 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Digital Delay 1	DLYE	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
RESET		0	0	0	0	0	0	0	0

DLY6-0: Setting a delay quantity of Digital Delay Circuit

The ADC's data can be delayed to maximum 90tap by a resolution of 1/64fs (=0.3μs@fs=48kHz).

	DATA	Tap	GAIN(dB)
	59H	90	90/64fs
	58H	89	89/64fs
	57H	88	88/64fs
	56H	87	87/64fs
	55H	86	86/64fs
	•	•	•
	04H	5	5/64fs
	03H	4	4/64fs
	02H	3	3/64fs
	01H	2	2/64fs
RESET	00H	1	1/64fs

Table 17. ATT value of Analog Volume

DLYE: Digital Delay Circuit Enable Flag

0: Disable. Digital delay circuit is disabled. Then its circuit is powered-down. (RESET)

1: Enable. Digital delay circuit is operated by a value set by DLY6-0 and COE3-0 bits.

Digital Delay 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Digital Delay 2	0	0	0	0	COE3	COE2	COE1	COE0
RESET		0	0	0	0	0	0	0	0

COE3-0: Setting of coefficient of digital delay circuit

After output data of ADC is delayed, the coefficient value subtracted from the opposite channel is set by COE3-0 bits.

COE3	COE2	COE1	COE0	coefficient
1	1	1	1	0.9375
1	1	1	0	0.875
1	1	0	1	0.8125
1	1	0	0	0.75
1	0	1	1	0.6875
1	0	1	0	0.625
1	0	0	1	0.5625
1	0	0	0	0.5
0	1	1	1	0.4375
0	1	1	0	0.375
0	1	0	1	0.3125
0	1	0	0	0.25
0	0	1	1	0.1875
0	0	1	0	0.125
0	0	0	1	0.0625
0	0	0	0	0

RESET

Table 18. Setting of coefficient of Digital Delay Circuit

FUNCTION DETAIL

■ MIC BLOCK

MIC block includes 2-inputs selectors, Internal MIC or External MIC Mode can be selected by S0 bit. (Refer to Figure 11 and Figure 12)
When Internal MIC is selected, the phase of HPF-Amp is inverted.

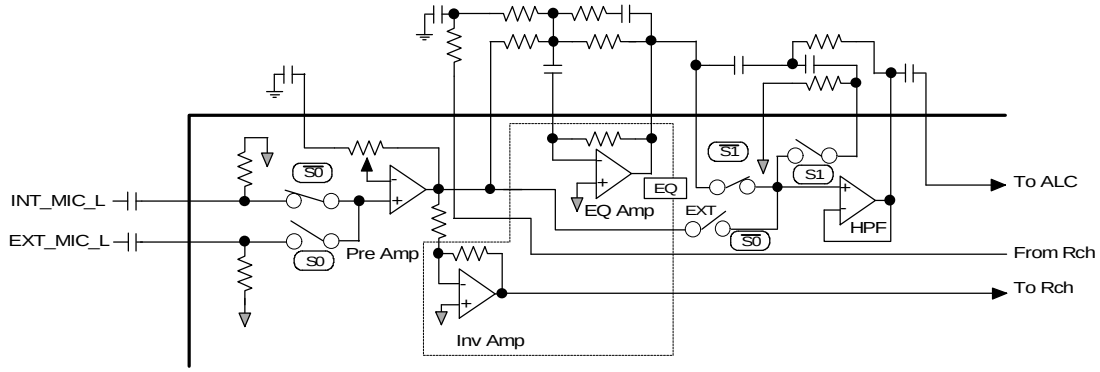


Figure 11. Internal path at selecting Internal MIC Mode (HPF OFF)

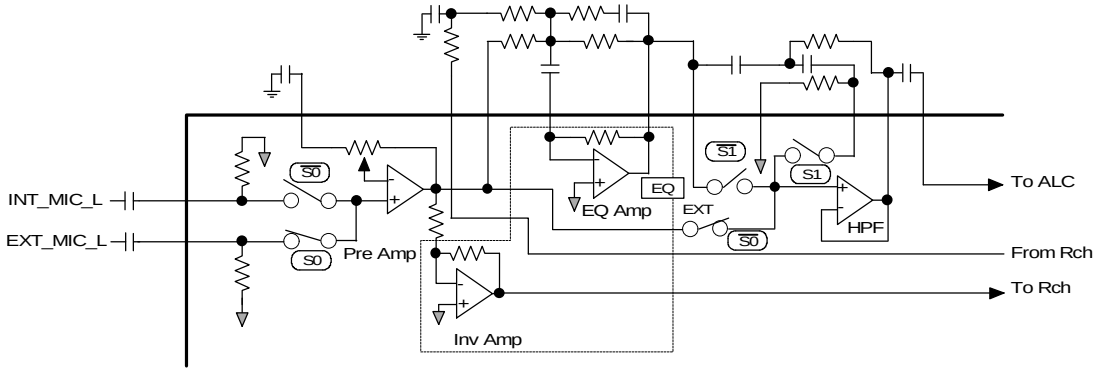


Figure 12. Internal path at selecting External MIC Mode (HPF OFF)

1. Pre-Amp

Pre-Amp is non-inverting amplifier and internally biased to MVCM voltage with 100kΩ (typ.). Gain value of Pre-Amp is adjusted by S6-5 bits. Their value is +12dB~+24dB and 4dB step.

Input impedance is changed by the set of gain. Input impedance value is precision in typ±30%.

S6	S5	Gain	Ri (typ)
0	0	+12dB	2.4kΩ
0	1	+16dB	1.5kΩ
1	0	+20dB	950Ω
1	1	+24dB	600Ω

RESET

An external capacitor needs to cancel DC gain. Cut-off frequency is decided by internal input resistor (Ri) and an external capacitor (C).

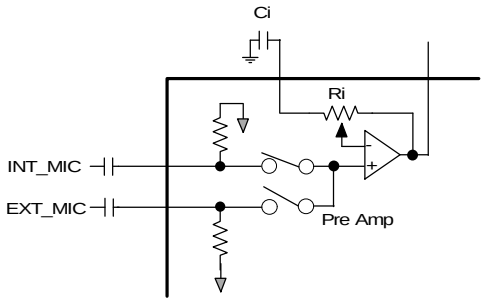


Figure 13. Pre-Amp Block

2. EQ-Amp

EQ-Amp is block to emphasize a stereo feeling at using Internal MIC Mode. EQ-Amp can be emphasized by adding the output signal from pre-amplifier and the opposite channel differentially.
When External MIC Mode is selected, EQ-Amp does not connect.

Power ON/OFF of EQ-Amp and Inverter-Amp is enabled by EQ bit. When EQ bit is "1", they can be ON/OFF by PM0 bit. When EQ bit is "0", these amplifiers are OFF then PM0 bit is not relative.

3. HPF-Amp

To cancel wind-noise, AK4561 has the HPF-Amp which is non-inverting amplifier, 2nd order high pass filter and gain of 0dB. The HPF-Amp can be ON/OFF by controlling the internal registers. In case of OFF, HPF-Amp becomes a unity gain buffer. This HPF-Amp can use when Internal MIC Mode is selected. In case of External MIC Mode, the control of HPF-Amp is invalid and becomes a unity gain buffer.

4. Power Supply for MIC

Power Supply for microphone is supplied from MPWR pin. Output voltage is typically 2.0V and MPWR pin can supply the current until 3mA.
When PM0 bit is "0", the power supply current can be stopped.

■ BEEP Input

When S9 bit is "1", input signal from BEEP pin can be output from MOUT pin. Normally, BEEP pin is connected with AC coupling.
Input impedance of BEEP pin is typically 50kΩ and centered around VCOM voltage. Maximum input voltage to BEEP pin is –5.5dBV.

■ Analog Volume (OPGA)

The AK4561 includes the 0dB ~ -50dB & MUTE analog volume with zero crossing detection for headphone and speaker. Zero crossing is detected on L/R channels independently. Zero crossing timeout (To) is 16ms.
These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

OPGA is not written during counting zero crossing timers. In case of writing control register continually, the change of OPGA should be written after zero crossing timeout and over. If OPGA is changed by writing to control register before zero crossing detection, OPGA value of L/R channels may not give a difference level.

In case of writing to the control register continually, the control register should be written by an interval more than zero crossing timeout. If an appointed interval is written, there is possible to the different value the IPGA value of L/R channels.

Usually, to remove the offset of DAC, it needs a capacitor (Ca) between LOUT2/ROUT2 and OPGL/OPGR. The cut-off frequency is decided by capacity of Ca and input impedance (typ. 110kΩ) of OPGL/OPGR.

Power supply for analog volume enables when PM6 or PM5 bits is "1".

The initial value is 0dB at exiting power-down.

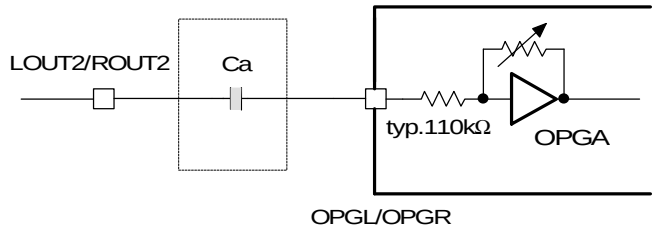


Figure 14. Connect LOUT2/ROUT2 with OPGL/OPGR

■ LINE input

In case of LINE input, input impedance of LIN/RIN is 184kΩ (typ.) and centered around the VCOM voltage. When input voltage is +2dBV, LIN/RIN pins should be input to –5.5dBV@VA=2.8V and less after dividing resistors externally.
When S2 bit is "1", LINE input is selected. Then IPGA table of ALC is changed to LINE side.

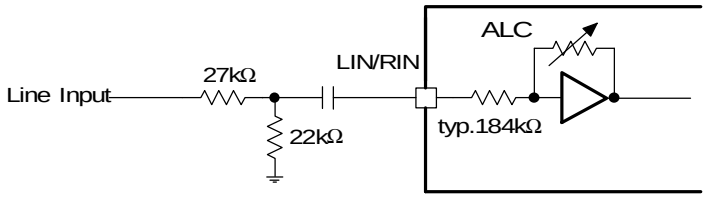


Figure 15. Example of LINEIN at VA=2.8V

■ Monaural Output

MOUT pin is provided to the output signal mixed by (L+R)/2 from analog volume (OPGA) by (L+R)/2 or the input signal from BEEP pin. Then the mixed signal and the input signal from BEEP pin are added by 1:1.
Maximum output signal is –5.5dBV and load impedance is minimum 5kΩ. The input signal from signal is inverted.

These signals can be stopped when S11 bit is "0". Then MOUT pin goes VCOM voltage and MOUT buffer becomes Power-Save-Mode. (Refer to Figure 17)

When $\overline{\text{PD}}$ pin changes from "L" to "H" after power-up, MOUT pin is powered-up in normal operation. (Refer to Figure 16)

In the Power-Down-Mode ($\overline{\text{PD}}$ pin = "L" or PM6 bit = "0"), output voltage of MOUT pin gradually change from AGND to VCOM voltage by the time constants of an internal resistor (R1; typ.200kΩ) and an external capacitor (C1). (Refer to Figure 18)

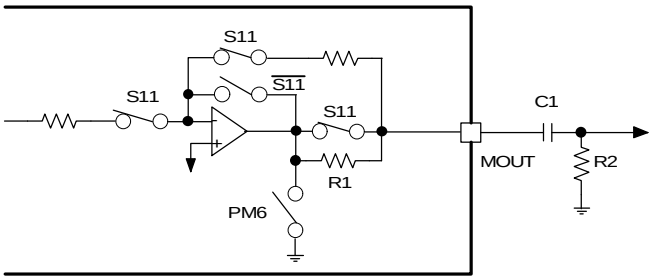


Figure 16. Normal Operation

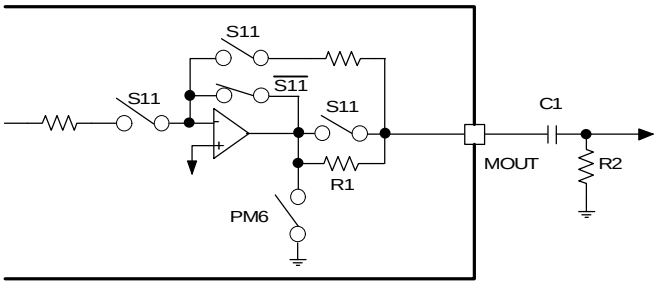


Figure 17. Power-Save-Mode

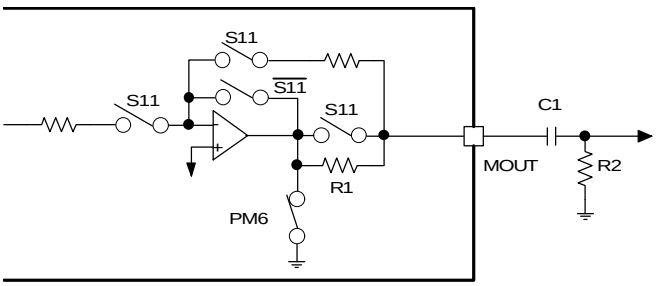


Figure 18. Power-Down-Mode

■ MUTE pin Function

When MUTE pin is “H”, output signals of LINEOUT and Headphone amplifiers are muted by force, and these signals are output to common voltage.
Monaural output is muted to the input signal of analog volume (OPGA), but is not muted to the input signal of BEEP pin.
When MUTE pin is “L”, the AK4561 is normal operation.

When MUTE pin changes from “L” to “H”, pop noise does not occur from output signals of headphone and monaural amplifiers, but the pop noise occurs from LINEOUT.
When MUTE pin changes from “H” to “L”, pop noise occurs from output signals of headphone, monaural and LINEOUT amplifiers.

■ REC_MUTE Function

When REC_MUTE pin is “H”, output data of ADC become “L” by force after data of Lch or Rch is provided to all 16bit.
When REC_MUTE pin is “L”, the AK4561 becomes normal operation.

■ Analog Through Mode

This mode can be input to playback circuits after adding ALC output signal and shutter signal. This mode can be controlled by PM4-3 bits.

■ LINEOUT

The signals of DAC or Analog Through Mode are gained to +7.5dB (@VA= 2.8V, Vol2-0 bit = "010") internally, and its signal is output from LINEOUT. This gain can be changed by VOL2-0 bits.
Output level of LINEOUT is +2dBV and centered HVCM voltage. Load resistance is min. 10kΩ. (Refer to Figure 19)

Power supply voltage for LINEOUT is supplied from HVDD voltage. The supplied HVDD voltage does not change output level of LINEOUT. But if HVDD voltage is low, a distortion characteristic of LINEOUT is bad.

LOUT1 and ROUT1 outputs are muted by S10 bit. Then LOUT1 and ROUT1 pins is output to HVCM voltage and enter Power-Save-Mode. (Refer to Figure 20). When PM7 bit is "0", LOUT1 and ROUT1 pins become Power-Down-Mode and output signal is Hi-z. (Refer to Figure 21)

When $\overline{\text{PD}}$ pin changes from "L" to "H" after power-up, LOUT1 and ROUT1 pins become Power-Save-Mode. In Power-Save-Mode, LOUT1 and ROUT1 pins gradually become HVCM voltage via an internal resistor (R1: typ.200kΩ) from Hi-z to decrease a pop noise. And when Power OFF, the pop noise can be decreased by controlling via Power-Save-Mode.

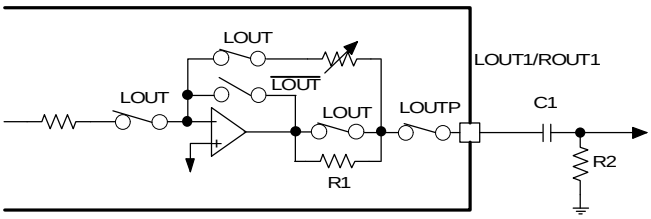


Figure 19. LINEOUT Normal Operation

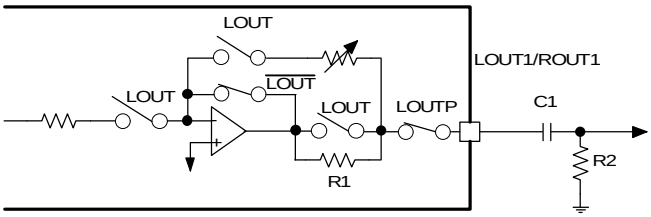


Figure 20. LINEOUT Power-Save-Mode

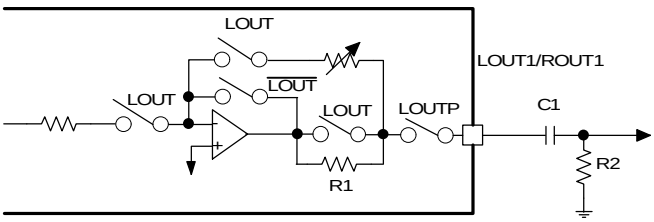


Figure 21. LINEOUT Power-Down-Mode

■ Headphone Amplifiers

The output circuit of headphone amplifier does not need a capacitor to cancel DC because the headphone amplifier includes center amplifier (HVCM). Load impedance of headphone amplifier is minimum 55Ω.

The output signals are muted when S8 bit is "0", the headphone amplifiers become Power-Save-Mode. Then HPL/HPR pin go Hi-z and HVCM pin is output to VCOM voltage. (Refer to Figure 23)

When PM5 bit is "0", the headphone amplifiers can be powered-up completely. Then HPL/HPR pins become Hi-z and HVCM pin becomes "L" (AGND). (Refer to Figure 24)

When $\overline{\text{PD}}$ pin changes from "L" to "H" after power-up, the output signals from headphone amplifier is muted, the headphone amplifiers are powered-up by Power-Save-Mode. After that, S8 bit should be changed into "0" before headphone amplifier is done by the normal operation.

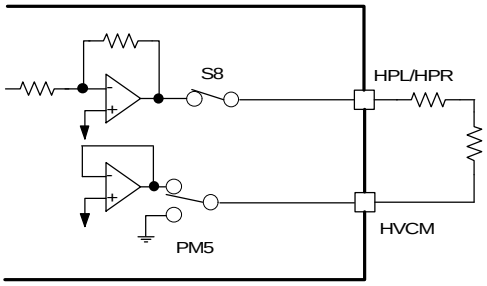


Figure 22. Headphone-Amps Normal Operation

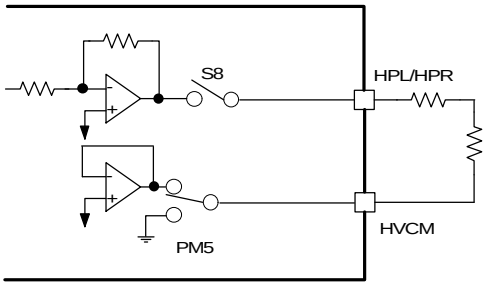


Figure 23. Headphone-Amps Power-Save-Mode

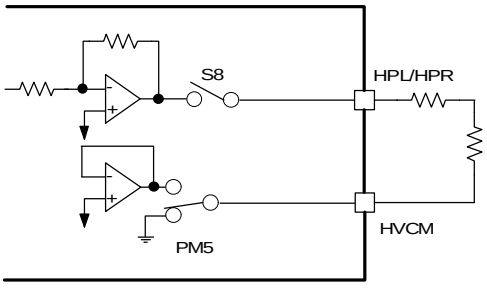


Figure 24. Headphone-Amps Power-Down-Mode

■ Digital Delay Circuit

When DLYE bit is "1", digital data (L1 and R1) of ADC can be delayed to a maximum 90tap (DLY6-0 bits) by a resolution of 1/64fs (=3µs@fs=48kHz). The coefficient value subtracted from the opposite channel is set by COE3-0 bit.

When DLYE bit is "0", the digital delay circuit is powered-down.

L2 = L1 – (ATT x (Delay x R1))
R2 = R1 – (ATT x (Delay x L1))

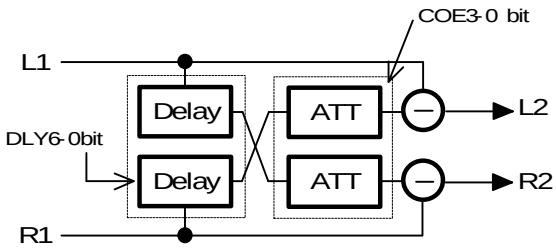


Figure 25. Digital Delay Circuit

DLYE, DLY6-0 and COE3-0 bits should be changed after ADC is powered-down. During the ADC is normal operation, pop noise may occur by changing these bits. The following sentences are an example of changing these bits.

1. Powered-down ADC (PM2 bit = "0")
2. Change DLYE, DLY6-0, COE3-0 bit
3. The power-down of ADC is released (PM2 bit = "1")
   Then ADC starts initialization cycle.

■ Comparator Output

The input DC voltage form VTH pin is compared with analog output from HPF-Amp. COMP pin goes "H" when either Lch or Rch of analog output exceeds threshold level, if it does not exceed the threshold level, COMP pin goes "L".

This threshold level can be set by the input DC voltage from VTH pin. VTH pin should be supplied to DC voltage (threshold of negative) divided by a resistor between MIC_B pin and MVSS pin. VTH pin can be supplied until minimum (MVCM – MVDD x 0.35). For example, the input voltage of VTH pin is 0.4V when MVDD is 2.8V. The threshold of positive side is converted by internal inverting amplifier.

■ ALC Operation

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceed ALC limiter detection level (LMTH), IPGA value is attenuated by ALC limiter ATT step (LMAT1-0) automatically. Then the IPGA value is changed commonly for L/R channels.

In case of ZELM = "0", timeout period is set by LTM1-0 bits. The operation for attenuation is done continuously until the input signal level becomes LMTH or less. After finishing the operation for attenuation, if ALC bit does not change into "0", the operation of attenuation repeats when the input signal level exceed LMTH. (Refer to Figure 26)

In case of ZELM = "1", timeout period is set by ZTM1-0 bits. The IPGA value is attenuated by zero crossing detection automatically. (Refer to Figure 27)

When FR bit is "0", the ALC operation corresponds to the impulse noise in additional to the ALC operation of AK4516A. When the impulse noise is input, the ALC recovery operation becomes the faster period than a normal recovery operation. When FR bit is "1", the ALC operation in AK4561 is the same as AK4516A's.

[Explanation for ALC operation]

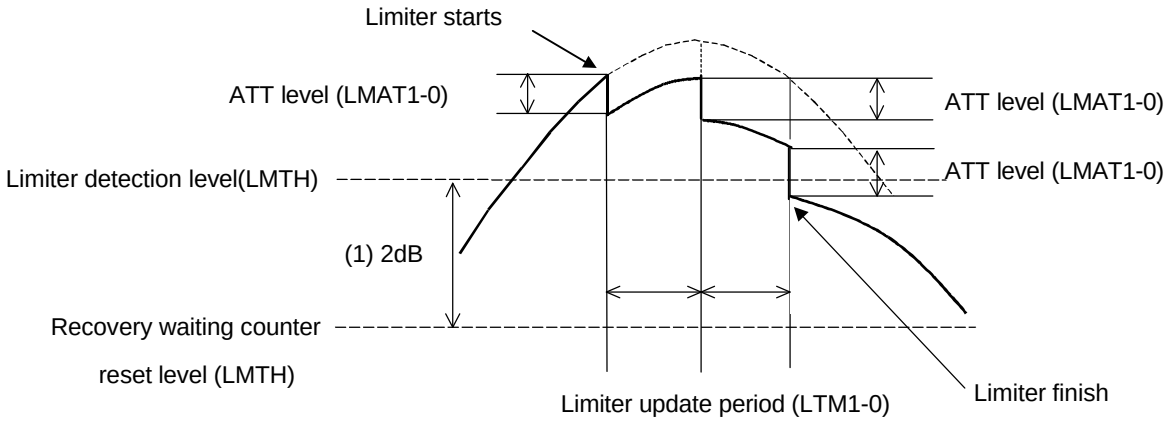


Figure 26. Disable ALC zero crossing detection (ZELM = "0")

(1). When the signal is input between 2dB, the AK4561 does not operate the ALC limiter and recovery.

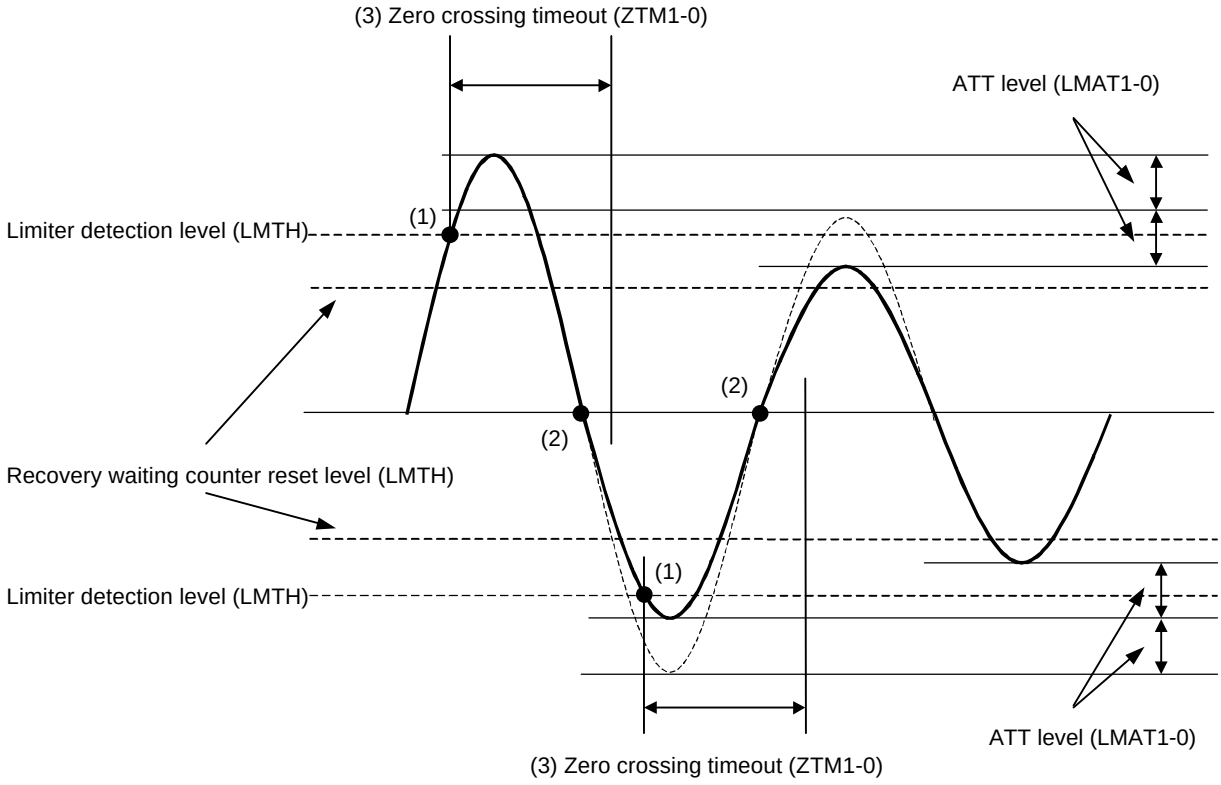


Figure 27. In case of continuing the limiter operation (ZELM = "1")

(1) When the input level exceeds the ALC limiter detection level, the ALC limiter operation starts. Zero crossing counter starts at the same time.
(2) Zero crossing detection. When the input signal is detected, the IPGA value is attenuated until the value set by LMAT1-0 and the ALC limiter operation is finished.
(3) Zero crossing timeout is set by ZTM1-0 bits. But the first zero crossing timeout cycle after starting the limiter operation may be the short cycle by the state of the last zero crossing counter. (For example, in case of doing the limiter operation during the recovery operation)

2. ALC Recovery Operation

The ALC recovery operation waits until a time of setting WTM1-0 bits after completing the ALC limiter. If the input signal does not exceed “Recovery waiting counter reset level ”, the ALC recovery operation is done. The IPGA value increases automatically by this operation up to the set reference level (REF6-0 bits). Then the IPGA value is set for L/R commonly. The ALC recovery operation is done at a period set by WTM1-0 bits.
When L/R channels are detected by zero crossing operation during WTM1-0, the ALC recovery operation waits until WTM1-0 period and the next recovery operation is done.

During the ALC recovery operation, when either input signal level of Lch or Rch exceeds the ALC limiter detection level (LMTH), the ALC recovery operation changes into the ALC limiter operation immediately
In case of “(Recovery waiting counter reset level) ≤ Input Signal < (Limiter detection level)” during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. Therefore, in case of “(Recovery waiting counter reset level) > Input Signal”, the waiting timer of ALC recovery operation starts.

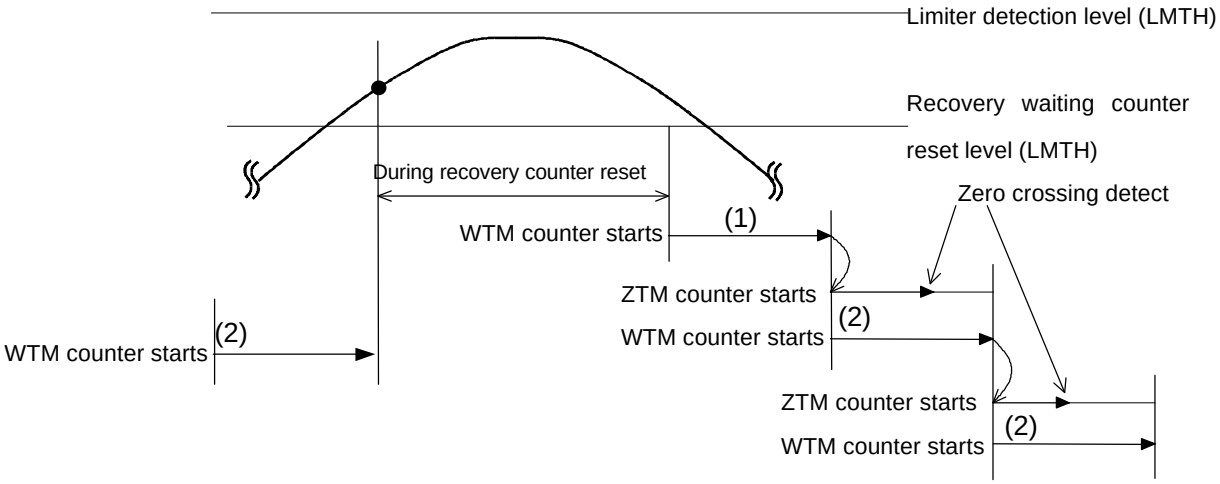


Figure 28. The transition from the limiter operation to the recovery operation

(1). When the input signal is below the ALC recovery waiting counter reset level, the ALC recovery operation waits the time set by WTM1-0 bits. If the input signal does not exceed the ALC limiter detection level or the ALC recovery waiting counter reset level, the ALC recovery operation is done only once.
(2). The IPGA value is changed by the zero crossing operation in ALC recovery operation, but the next counter of the ALC recovery waiting timer is also starting.

Other:

When a channel of one side enters the limiter operation during the waiting zero crossing, the present ALC recovery operation stops, according as the small value of IPGA (a channel of waiting zero crossing), the ALC limiter operation is done.
When both channels are waiting for the next ALC recovery operation, the ALC limiter operation is done from the IPGA value of a point in time.
During the ALC operation, the value of writing in IPGA6-0 bits is ignored.

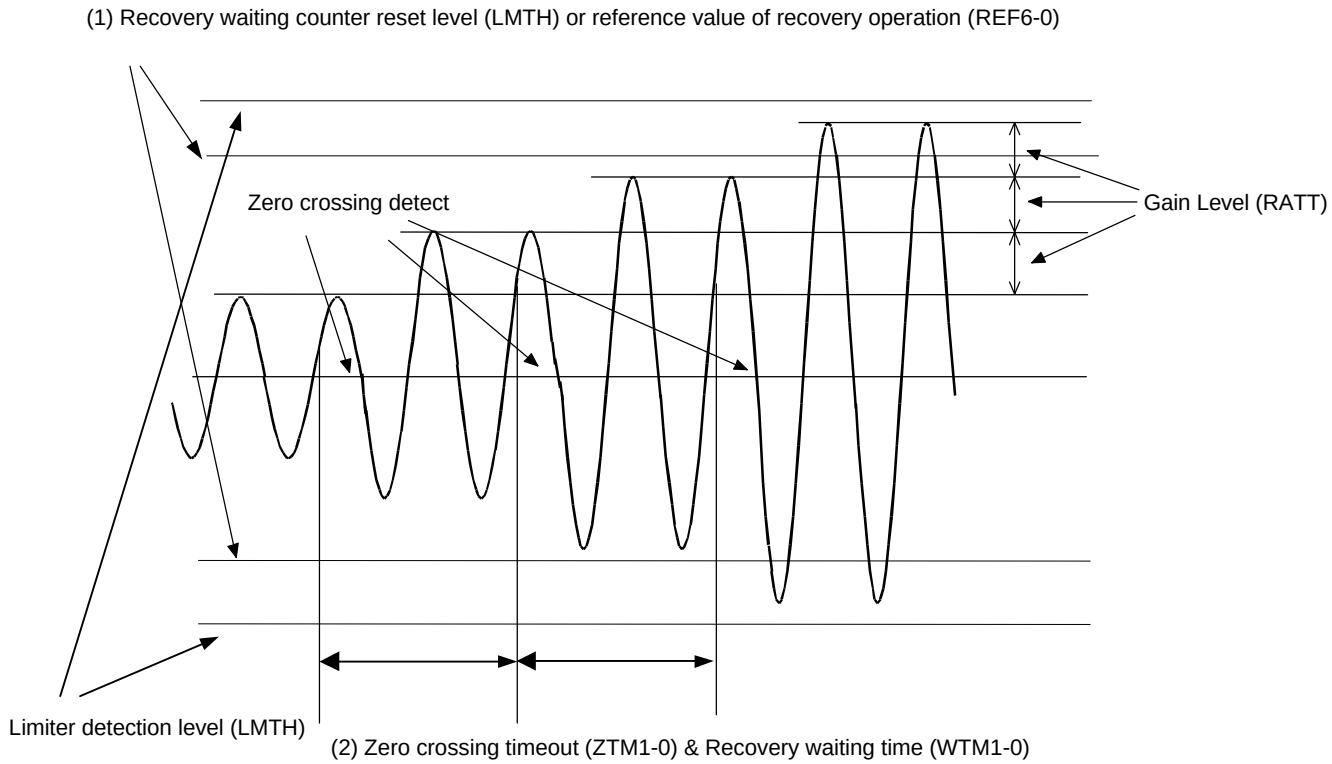


Figure 29. The continuous ALC Recovery Operation

(1). When the input signal exceeds the ALC recovery waiting counter reset level, the ALC recovery operation stops, the ALC recovery operation is repeated when input signal level is below "LMTH" again. When the IPGA value by repeating the ALC recovery operation reaches the reference level (REF6-0 bits), the ALC recovery operation stops.
(2). ZTM bit sets zero crossing timeout and WTM bit sets the ALC recovery operation period. When the ALC recovery waiting time (WTM1-0 bits) is shorter than zero crossing timeout period of ZTM1-0 bit, the ALC recovery is operated by the zero crossing timeout period of ZTM1-0 bit. Therefore, in this case the auto recovery operation period is not constant.

3. Attention of IPGA writing operation

During the ALC operation, internal control register indicates the different value to the current IPGA value. And if the writing value before and after the ALC operation is same, the IPGA value is not updated.
If the IPGA is the same value before and after the ALC operation, it needs to write the dummy command during the ALC operation.

In Figure 30, the last IPGA value is reflected by doing the following sequence.

WR(IPGA=60H) → WR(ALC= "1") → WR(ALC= "0") → WR(IPGA=60H)

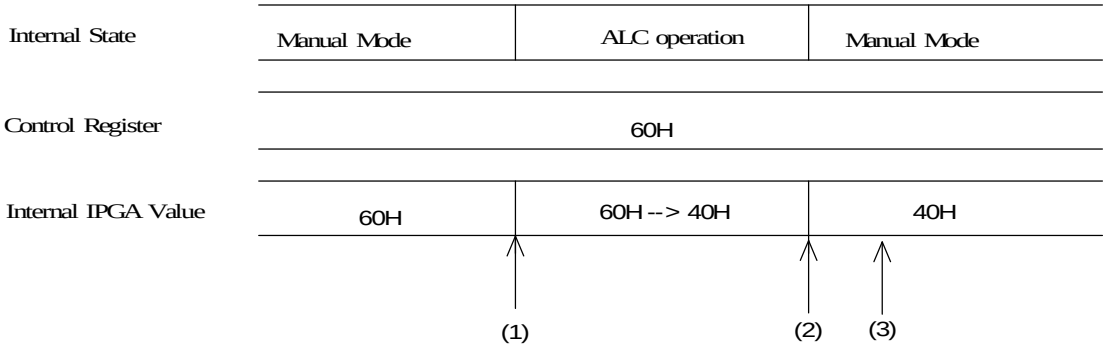


Figure 30. IPGA value during ALC operation 1

(1) WR(ALC = "1"): Enter ALC mode from Manual mode
(2) WR(ALC = "0"): Finish ALC mode and enter Manual mode
The IPGA becomes a value after finishing ALC operation. (In Figure 30, the IPGA value assumes 40H.)
(3) WR(IPGA=60H): If the written value to control register is the same as the current value, the written value is ignored, therefore the IPGA value keeps 40H (the value after finishing the ALC operation).

In Figure 31, the last IPGA value is reflected by doing the following sequence.

WR(IPGA=60H) → WR(ALC = "1") → WR(IPGA=00H) → WR(ALC = "0") → WR(IPGA=60H)

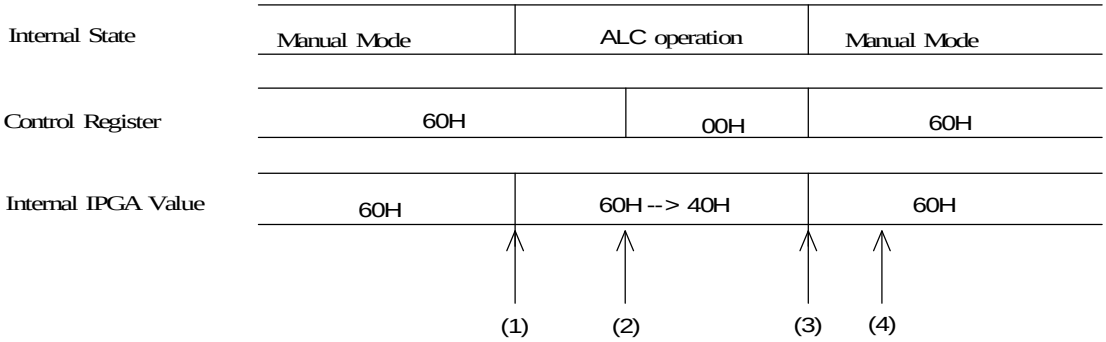


Figure 31. IPGA value during ALC operation 2

(1) WR(ALC = "1"): Enter ALC mode from Manual mode
(2) WR(IPGA="00"): Write IPGA=00H to control register.
The IPGA value of fact is not reflected during ALC operation.
(3) WR(ALC = "0"): Finish ALC mode and enter Manual mode
(4) WR(IPGA=60H): IPGA value is changed as between the last written value to control register (IPGA=00H) and the IPGA value at finishing ALC operation is different value.

4. IPGA writing operation at ALC operation OFF (ALC bit = "0")

The zero crossing detection of IPGA is done to L/R channels independently. Zero crossing timeout can be set by ZTM1-0 bits. When the control register is written from μP, the zero crossing counter for L/R channels commonly is reset and its counter starts. When the signal detects zero crossing or zero crossing timeout, the written value from μP becomes a valid for the first time.
In case of writing to the control register continually, the control register should be written by an interval more than zero crossing timeout. If an appointed interval is written, there is possible to the different value the IPGA value of L/R channels. For example, when the present IPGA value is updated by zero crossing detection in a channel of one side and other channel is not updated, if the new data is written in IPGA, the updated channel is keeping the last IPGA value and other channel is updated to a new IPGA value by the last zero crossing counter. Therefore, zero crossing counter does not reset when the zero crossing detection is waiting.

If the written value is the same as the current value, the writing value is ignored.

During ALC operation, the following registers are inhibits.
• LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0, ZELM

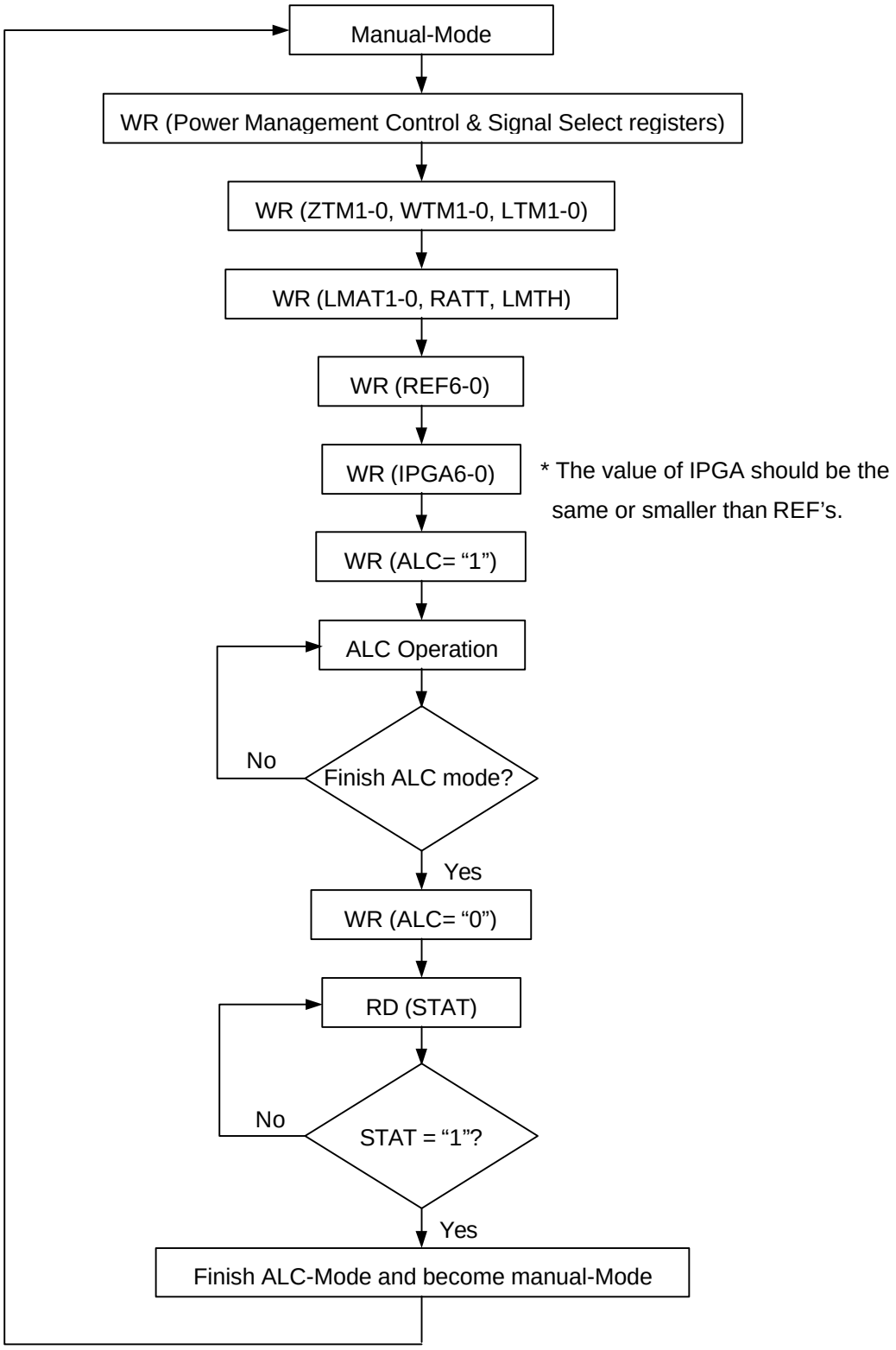


Figure 32. Registers set-up sequence at ALC operation

■ FADEIN Mode

In FADEIN Mode, the IPGA value is increased at the value set by FDATT when FDIN bit changes from "0" to "1". The update period can be set by FDTM1-0 bits. The FADEIN Mode is always detected by the zero crossing operation. This operation is kept over the REF value or until the limiter operation at once. If the limiter operation is done during FADAIN cycle, the FADEIN operation becomes the ALC operation.

NOTE: When FDIN and FDOUT bits are "1", FDOUT operation is enabled.

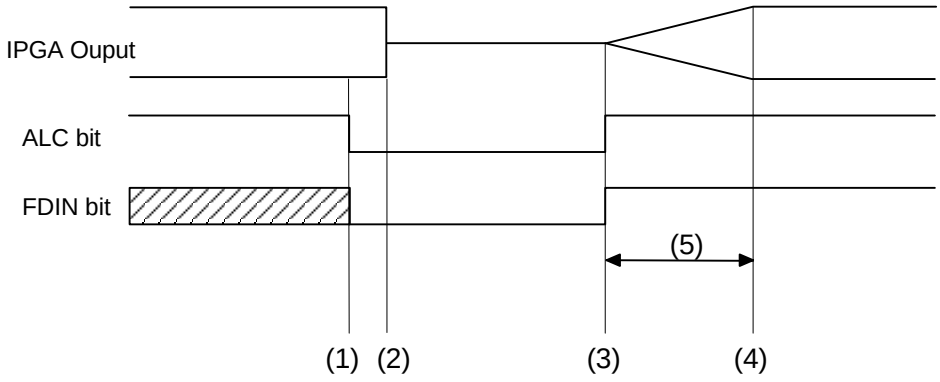


Figure 33. Example for controlling sequence in FADEIN operation

(1) WR (ALC = FDIN = "0"): The ALC operation is disabled. To start the FADEIN operation, FDIN bit is written in "0".
(2) WR (IPGA = "MUTE"): The IPGA output is muted.
(3) WR (ALC = FDIN = "1"): The FADEIN operation starts. The IPGA changes from the MUTE state to the FADEIN operation.
(4) The FADEIN operation is done until the limiter detection level (LMTH) or the reference level (REF6-0). After completing the FADEIN operation, the AK4561 becomes the ALC operation.
(5) FADEIN time can be set by FDTM1-0 and FDATT bits
E.g. FDTM1-0 = 32ms, FDATT = 1step
(96 x FDTM1-0) / FDATT = 96 x 32ms / 1 = 3.07s

■ FADEOUT Mode

In FADEOUT mode, the present IPGA value is decreased until the MUTE state when FDOUT bit changes from "0" to "1". This operation is always detected by the zero crossing operation.
If the large signal is input to the ALC circuit during the FADEOUT operation, the ALC limiter operation is done. However a total time of the FADEOUT operation is the same time, even if the limiter operation is done. The period of FADEOUT is set by FDTM1-0 bits, a number of step can be set by FDATT bit.
When FDOUT bit changes into "0" during the FADEOUT operation, the ALC operation start from the preset IPGA value. When FDOUT and ALC bits change into "0" at the same time, the FDOUT operation stops and the IPGA becomes the value at that time.

NOTE: When FDIN and FDOUT bits are "1", FDOUT bit is enabled.

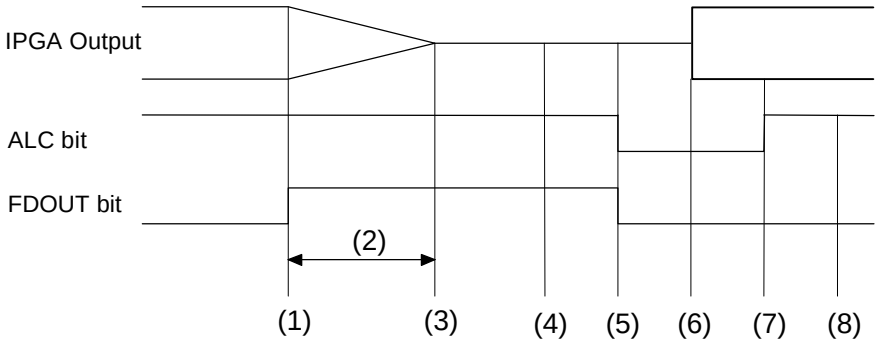
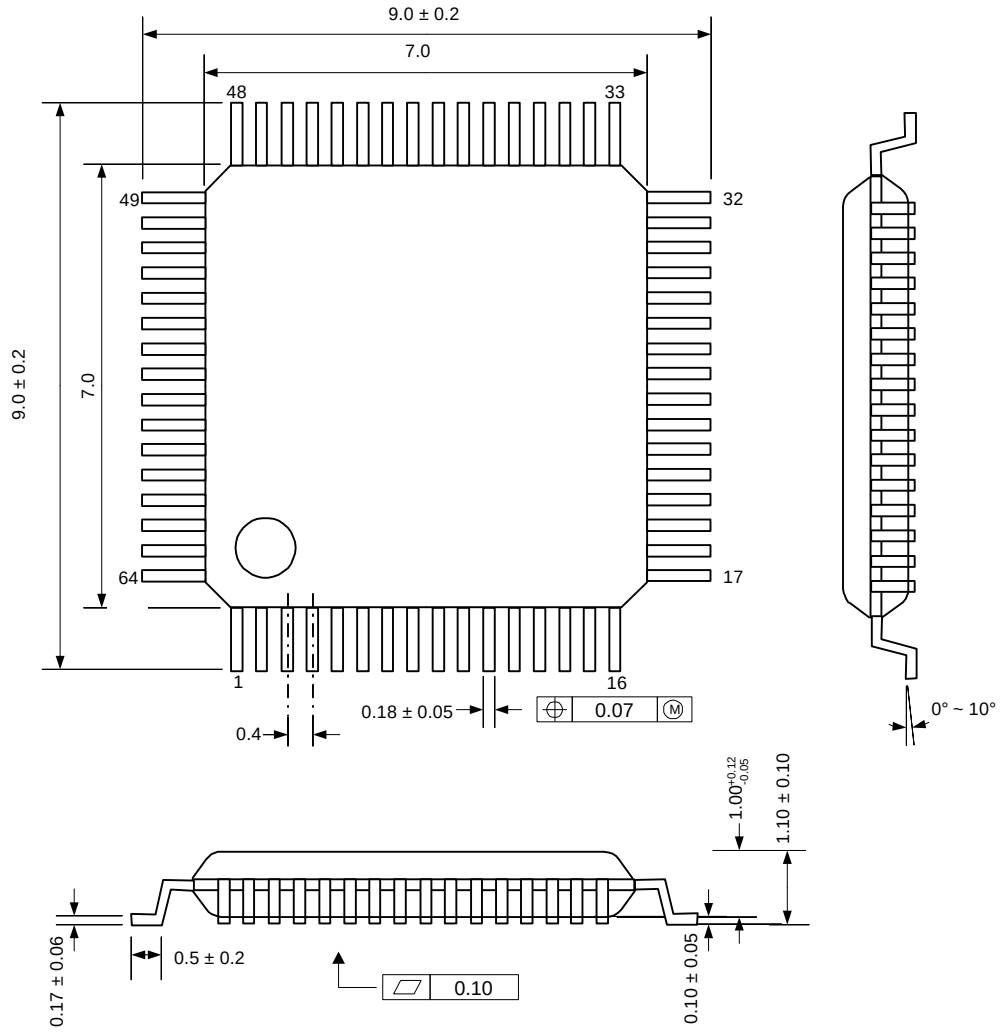


Figure 34. Example for controlling sequence in FADEOUT operation

(1) WR (FDOUT = "1"): The FADEOUT operation starts. Then ALC bit should be always "1".
(2) FADEOUT time can be set by FDTM1-0 and FDATT bits.
During the FADEIN operation, the zero crossing timeout period is ignored and becomes the same as the FADEIN period.
E.g. FDTM1-0 = 32ms, FDATT = 1step
(96 x FDTM1-0) / FDATT = 96 x 32ms / 1 = 3.07s
(3) The FADEOUT operation is completed. The IPGA value is the MUTE state. If FDOUT bit is keeping "1", the IPGA value is keeping the MUTE state.
(4) Analog and digital outputs mutes externally. Then the IPGA value is the MUTE state.
(5) WR (ALC = FDOUT = "0"): Exit the ALC and FADEOUT operations
(6) WR (IPGA): The IPGA value changes the initial value (exiting MUTE state).
(7) WR (ALC = "1", FDOUT = "0"): The ALC operation restarts. But the ALC bit should not write until completing zero crossing operation of IPGA.
(8) Release a mute function of analog and digital outputs externally.

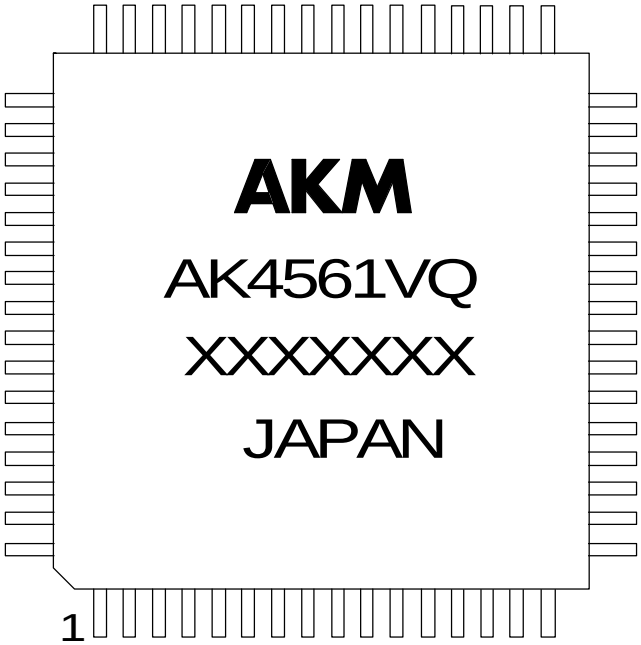
PACKAGE



■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

MARKING



- Asashi kasei Logo
- Marketing Code: AK4561VQ
- Date Code: XXXXXXX (7 digits)
  First 4 digits: weekly code, Remains 3 digits: code management in office
- Country of Origin: JAPAN