FPD750SOT343

Datasheet v3.0

LOW NOISE HIGH LINEARITY PACKAGED PHEMT

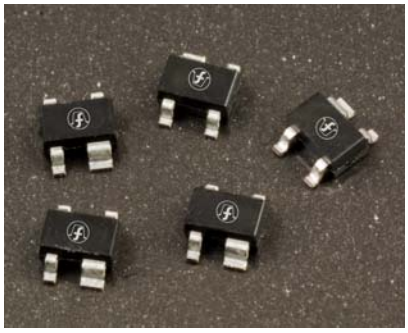
FEATURES (1850MHZ):

- 0.5 dB N.F.min.
- 20 dBm Output Power (P1dB)
- 16.5 dB Small-Signal Gain (SSG)
- 37 dBm Output IP3
- RoHS compliant (Directive 2002/95/EC)

GENERAL DESCRIPTION:

The FPD750SOT343 is a packaged depletion mode pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 750 µm Schottky barrier Gate. The Filtronic 0.25µm process ensures class-leading noise performance. The use of a small footprint plastic package allows for cost effective system implementation.

PACKAGE:



ROHS:

TYPICAL APPLICATIONS:

- 802.11a,b,g and WiMax LNAs
- PCS/Cellular High Linearity LNAs
- Other types of wireless infrastructure systems.

TYPICAL PERFORMANCE[1]:

RF PARAMETER	SYMBOL	CONDITIONS	0.9GHZ	1.85GHZ	2.6GHZ	3.5GHZ	UNITS
Power at 1dB Gain Compression	OP1dB	VDS = 3.3 V; IDS = 40mA	20	19	20	20.5	dBm
Small Signal Gain	SSG	VDS = 3.3 V; IDS = 40mA	22	16.5	14	11	dB
Power-Added Efficiency	PAE	VDS = 3.3 V; IDS = 40mA POUT = P1dB	50	45	45	50	%
Maximum Stable Gain (|S21/S12|)	MSG	VDS = 3.3 V; IDS = 40mA	24	20	18	16	dB
Noise Figure	N.F.	VDS = 3.3 V; IDS = 40mA	0.5	0.6	0.7	0.8	dB
Output Third-Order Intercept Point POUT = 9 dBm per Tone	OIP3	VDS = 3.3V; IDS = 40mA VDS = 3.3V; IDS = 80mA	32 35	31 37	31 35	32 38	dBm

ELECTRICAL SPECIFICATIONS[2]:

RF/DC PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	f			2.0		GHz
Power at 1dB Gain Compression	P1dB	VDS = 3.3 V; IDS = 40mA	17			dBm
Small Signal Gain	SSG	VDS = 3.3 V; IDS = 40mA	16			dB
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	185	230	280	mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		200		mS
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 0.75 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 0.75 mA	13	16		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 0.75 mA	13	18		V
Thermal Resistivity (see Notes)	θJC	VDS > 3V		143		°C/W

Note: 1. Based on measured data taken on applications circuits. 2. All devices are 100% RF and DC tested at 2GHz with $Z_S = Z_L = 50$ Ohms 3. $T_{AMBIENT} = 22°C$

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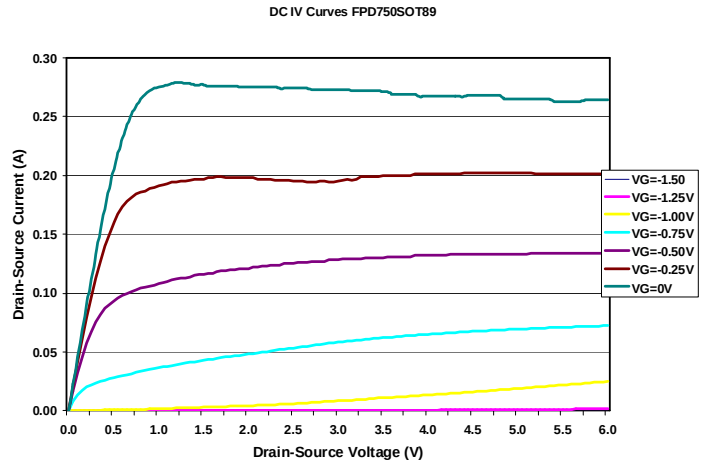
ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < -0.5V	6V
Gate-Source Voltage	VGS	0V < VDS < +6V	-3V
Drain-Source Current	IDS	For VDS < 2V	IDss
Gate Current	IG	Forward or reverse current	7.5mA
RF Input Power[2]	PIN	VDS = 3.3V	22dBm
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-55°C to 150°C
Total Power Dissipation[4]	PTOT	See De-Rating Note below	1.1W
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits	80%

Notes:
[1] $T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device
[2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously
[4] Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power
Total Power Dissipation to be de-rated as follows above 22°C:
$P_{TOT} = 1.1 - (1/\Theta jc) \times T_{PACK}$
where T_{PACK}= source tab lead temperature above 22°C & Θjc = 143ºC/W

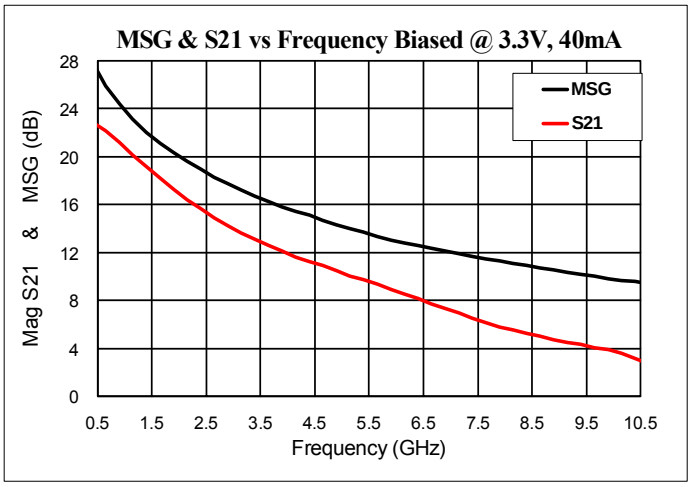
BIASING GUIDELINES:

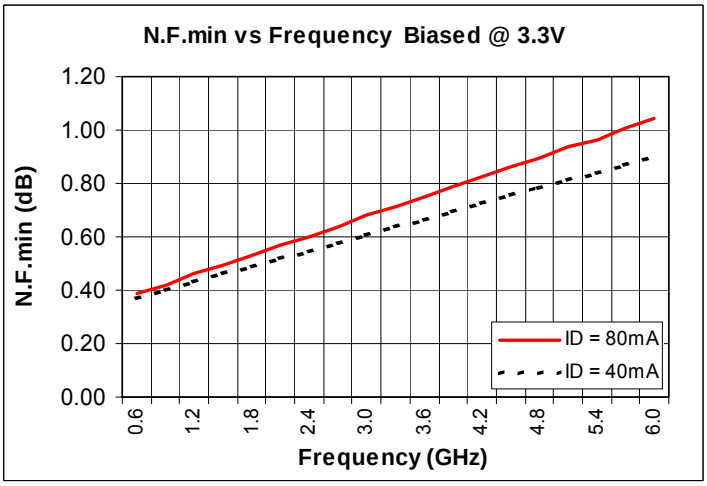
- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.
- For standard Class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Class A/B bias of 25-33% offers an optimised solution for NF and OIP3.



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the V_{DS} > 1.3V will generally cause errors in the current measurements, even in stabilized circuits.

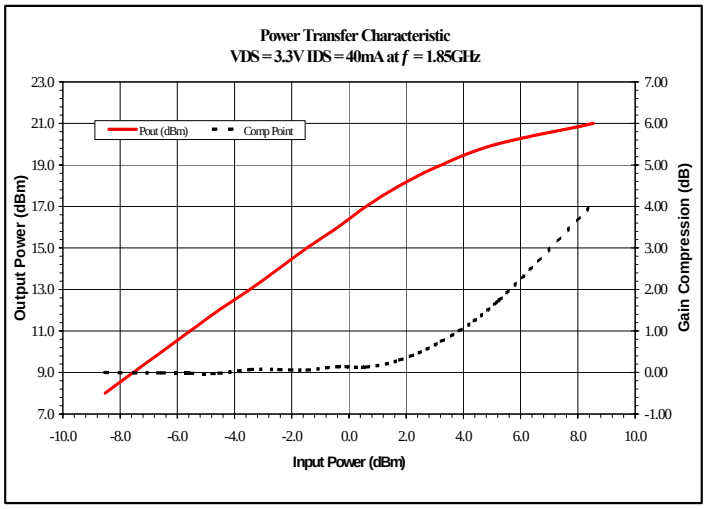
TYPICAL FREQUENCY REPONSE:

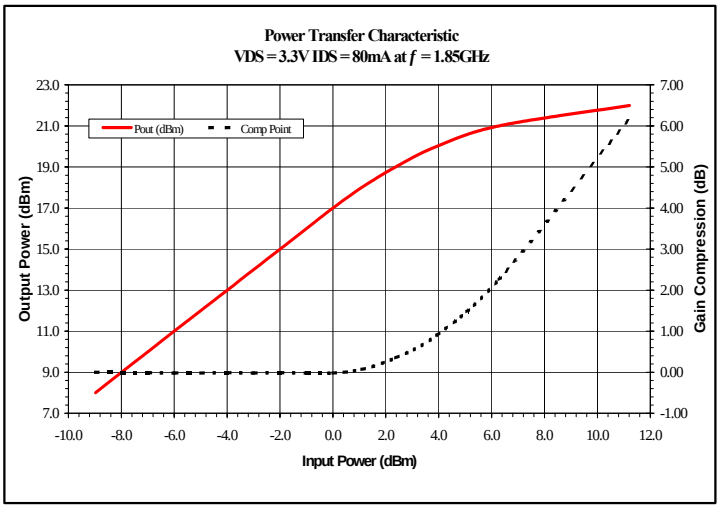




NOTE: Typical Gain and Noise figure variation against frequency is shown above. The devices were biased nominally at V_{DS} = 3.3V, I_{DS} = 40mA. The test devices were tuned for minimum noise figure and maximum gain using tuners at the device input and output ports.

TYPICAL RF PERFORMANCE @ 1.85 GHz:





NOTE: Typical power transfer curves at two bias conditions are shown above. The data is taken with the device mounted on evaluation board tuned at 1.85GHz for low noise and gain as shown in the reference design given on page 6.

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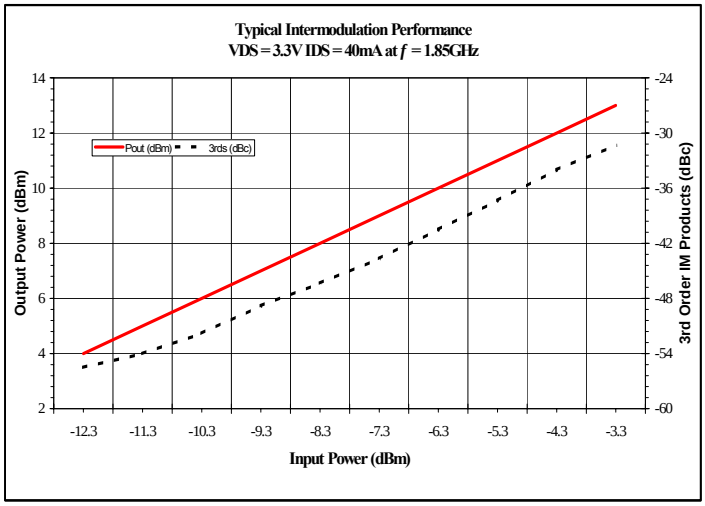
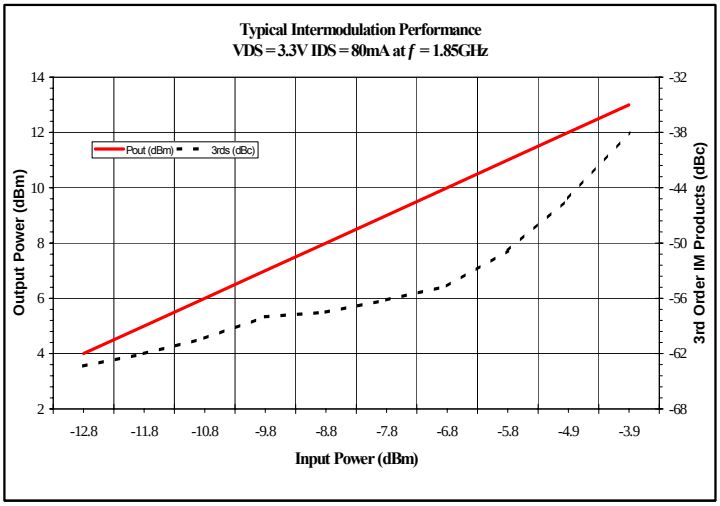
TYPICAL RF PERFORMANCE @ 1.85 GHz:





NOTE: Typical intermodulation performance is shown above. The data is taken with the device mounted on evaluation board tuned at 1.85GHz for low noise and gain as shown in the reference design given on page 6. The FPD750SOT343 has enhanced Intermodulation performance with an OIP3 value of up to P1dB+16dBm. This effect can be seen when the device is biased at ID=80mA by the bough in the 3rd order product plot line .

NOISE PARAMETERS:

Biased at VDS=3.3V, IDS=40mA

Freq. (GHz)	N.F.min (dB)	Γopt		Rn/50
		Mag	Angle	
0.60	0.37	0.770	12.2	0.108
0.90	0.40	0.689	21.2	0.100
1.20	0.43	0.614	30.6	0.092
1.50	0.46	0.546	40.4	0.084
1.80	0.49	0.485	50.6	0.077
2.10	0.52	0.431	61.1	0.069
2.40	0.55	0.383	72.1	0.063
2.70	0.58	0.342	83.4	0.057
3.00	0.61	0.307	95.1	0.053
3.30	0.64	0.280	107.2	0.049
3.60	0.67	0.258	119.8	0.046
3.90	0.70	0.244	132.7	0.043
4.20	0.73	0.236	146.0	0.042
4.50	0.76	0.236	159.6	0.040
4.80	0.78	0.242	173.7	0.040
5.10	0.81	0.254	-171.9	0.041
5.40	0.84	0.273	-157.0	0.044
5.70	0.87	0.299	-141.8	0.050
6.00	0.90	0.332	-126.1	0.061

Biased at VDS=3.3V, IDS=80mA

Freq. (GHz)	N.F.min (dB)	Γopt		Rn/50
		Mag.	Angle	
0.60	0.39	0.732	11.5	0.129
0.90	0.42	0.644	22.1	0.115
1.20	0.46	0.564	33.0	0.102
1.50	0.50	0.492	44.2	0.090
1.80	0.53	0.428	55.9	0.079
2.10	0.57	0.372	67.9	0.070
2.40	0.60	0.324	80.2	0.063
2.70	0.64	0.283	93.0	0.057
3.00	0.68	0.251	106.2	0.053
3.30	0.71	0.227	119.7	0.050
3.60	0.75	0.210	133.6	0.049
3.90	0.79	0.202	147.9	0.048
4.20	0.83	0.201	162.5	0.048
4.50	0.86	0.208	177.5	0.049
4.80	0.90	0.223	-167.1	0.051
5.10	0.94	0.247	-151.4	0.056
5.40	0.97	0.277	-135.2	0.065
5.70	1.01	0.317	-118.7	0.080
6.00	1.05	0.364	-101.8	0.106

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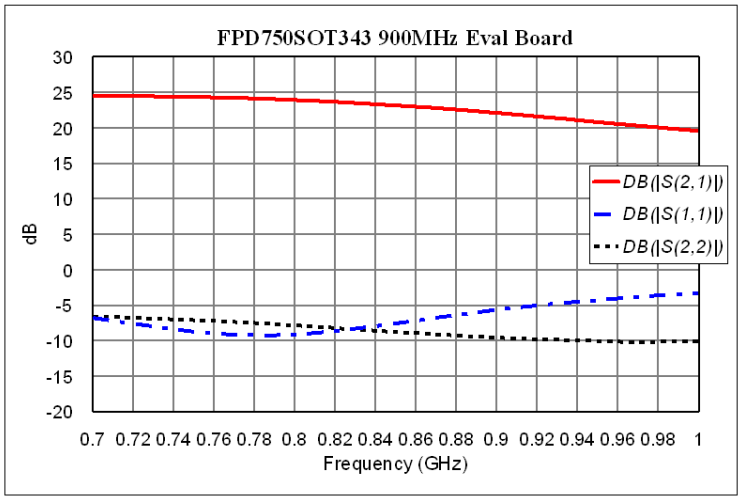
REFERENCE DESIGN (0.9GHZ):

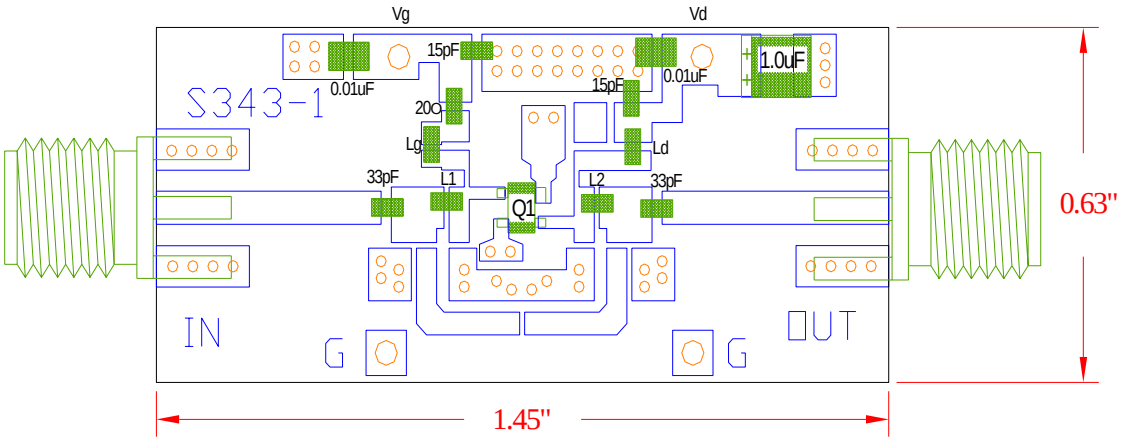
FREQUENCY	GHZ	0.9
Gain	dB	22
P1dB	dBm	20
OIP3[1]	dBm	32
N.F.	dB	0.5
S11	dB	-5
S22	dB	-10
Vd	V	3.3
Vg	V	-0.4 to -0.6
Id	mA	40

1. OIP3 measured at Pout of 9dBm per tone



Measured Gain and Return Loss

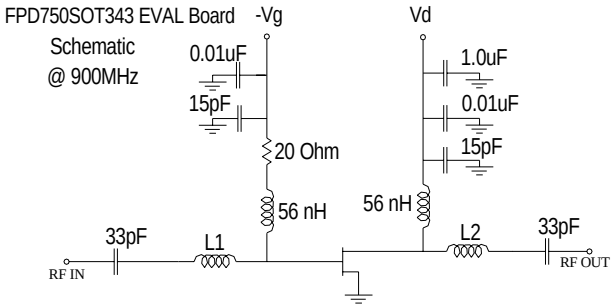
BOARD LAYOUT:



Component Values

Component	Value	Description
Lg	56nH	LL1608 Toko chip inductor
Ld	56nH	LL1608 Toko chip inductor
L1	15nH	LL1608 Toko chip inductor
L2	4.7nH	LL1608 Toko chip inductor

Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides



D.C. Blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20 Ohm Chip resistor from Vishay is used on the gate D.C. bias line for stability.

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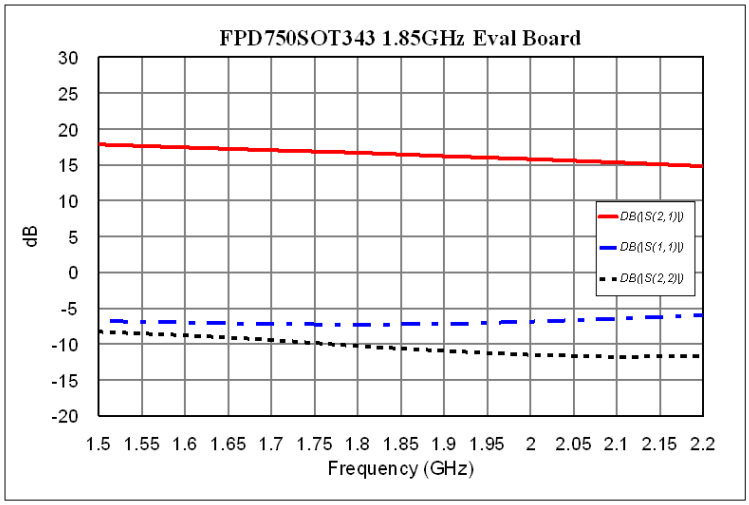
REFERENCE DESIGN (1.85GHZ):

FREQUENCY	GHZ	1.85
Gain	dB	16.5
P1dB	dBm	19
OIP3[1]	dBm	31
N.F.	dB	0.6
S11	dB	-6
S22	dB	-10
Vd	V	3.3
Vg	V	-0.4 to -0.6
Id	mA	40

1.OIP3 measured at Pout of 9dBm per tone



Measured Gain and Return Loss

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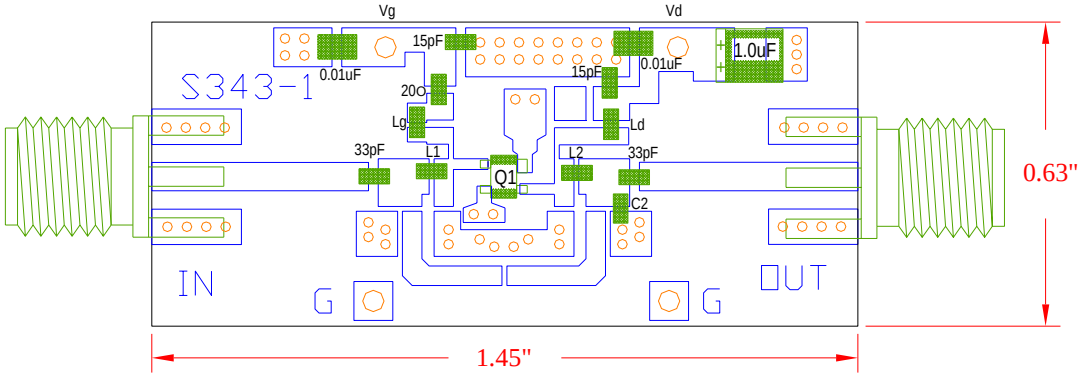
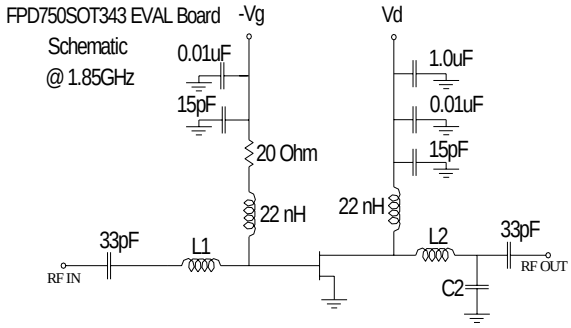


Component Values

Component	Value	Description
Lg	22nH	LL1608 Toko chip inductor
Ld	22nH	LL1608 Toko chip inductor
L1	2.2nH	LL1005 Toko chip inductor
L2	1.8nH	LL1005 Toko chip inductor
C2	1.0pF	ATC 600S Chip Capacitor

Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides



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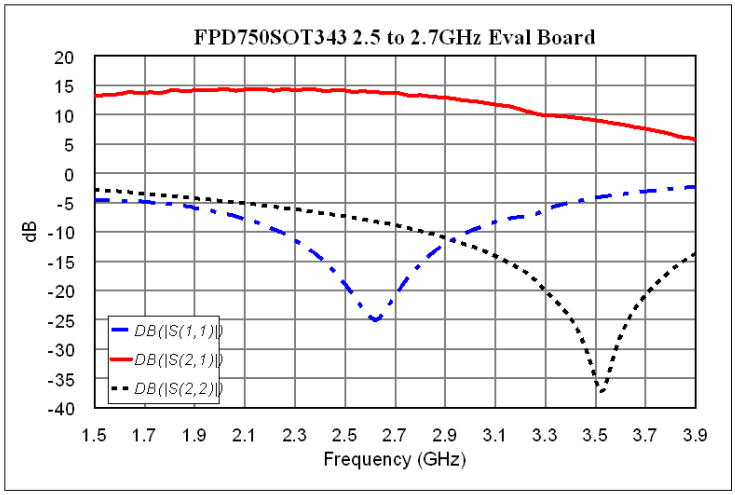
REFERENCE DESIGN (2.6GHZ):

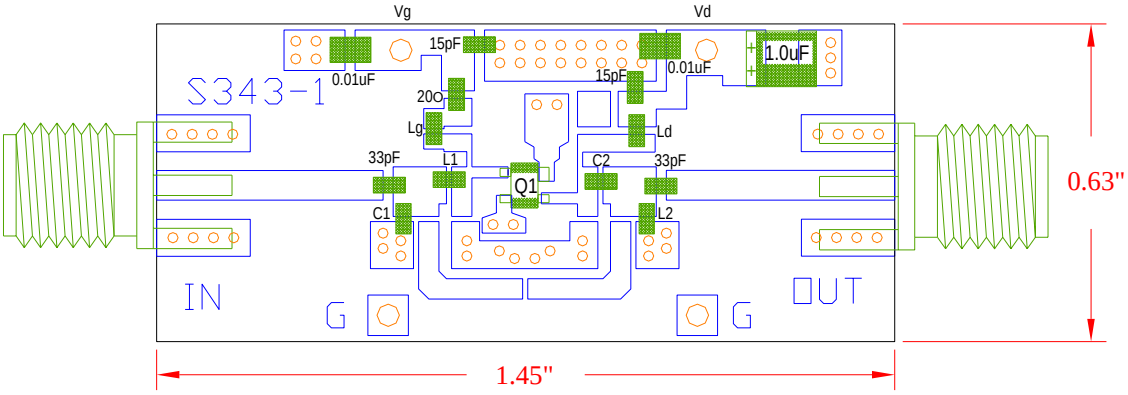
FREQUENCY	GHZ	2.5	2.6	2.7
Gain	dB	14.2	14	13.5
P1dB	dBm	20	21	21
OIP3[1]	dBm	30.5	31	31
N.F.	dB	0.8	0.7	0.75
S11	dB	-20	-25	-20
S22	dB	-7	-8	-10
Vd	V	3.3		
Vg	V	-0.4 to -0.6		
Id	mA	40		

1. OIP3 measured at Pout of 9dBm per tone



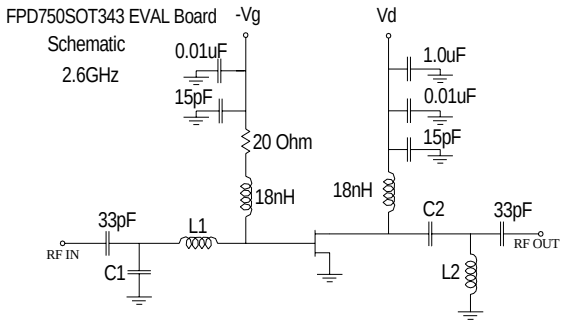
Measured Gain and Return Loss

BOARD LAYOUT:



Component Values

Component	Value	Description
Lg	18nH	LL1608 Toko chip inductor
Ld	18nH	LL1608 Toko chip inductor
L1	1.2nH	LL1005 Toko chip inductor
L2	2.7nH	LL1005 Toko chip inductor
C1	1.0pF	ATC 600S Chip Capacitor
C2	1.8pF	ATC 600S Chip Capacitor



Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides

D.C. Blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20 Ohm Chip resistor from Vishay is used on the gate D.C. bias line for stability.

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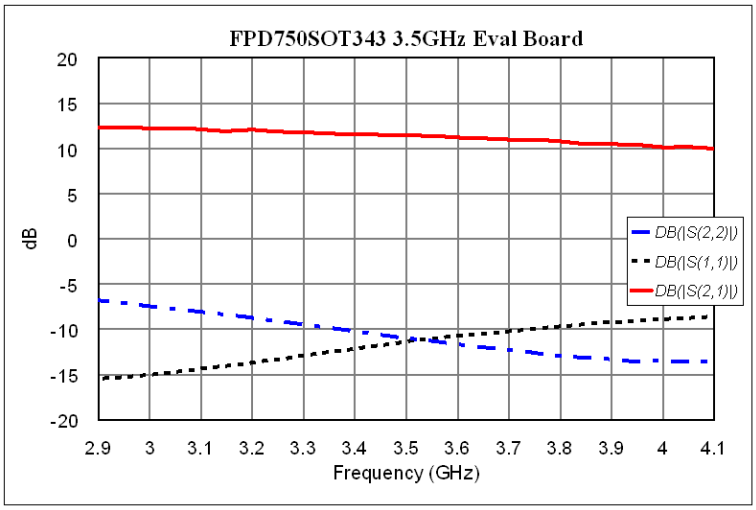
REFERENCE DESIGN (3.5GHZ):

FREQUENCY	GHZ	3.5
Gain	dB	11
P1dB	dBm	20.5
OIP3[1]	dBm	32
N.F.	dB	0.75
S11	dB	-11
S22	dB	-11
Vd	V	3.3
Vg	V	-0.4 to -0.6
Id	mA	40

1. OIP3 measured at Pout of 9dBm per tone



Measured Gain and Return Loss

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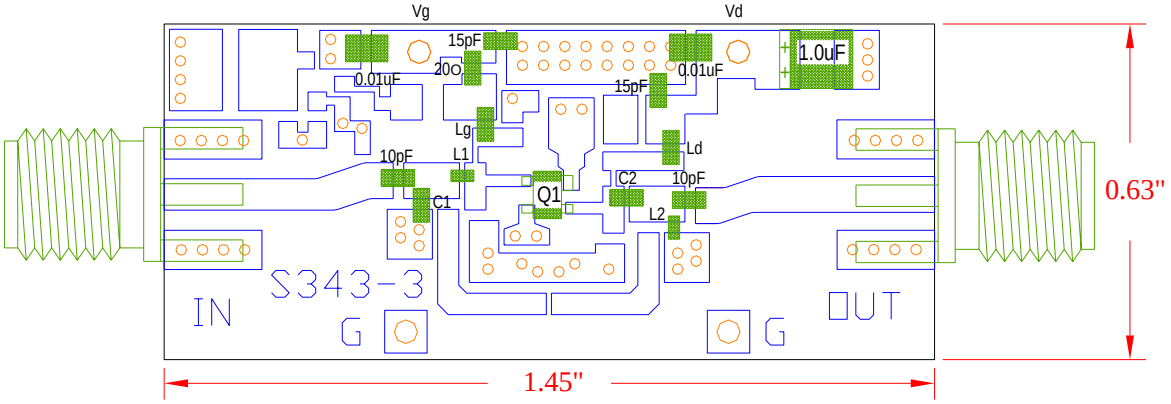
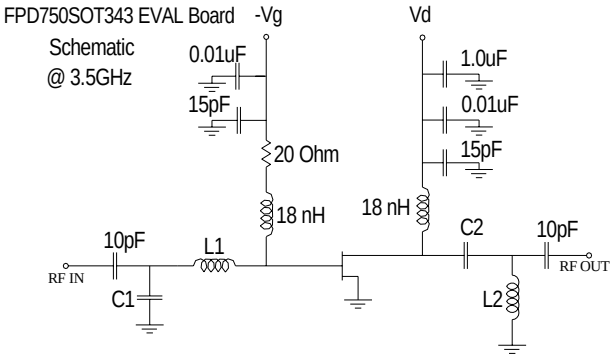


Component Values

Component	Value	Description
Lg	18nH	LL1608 Toko chip inductor
Ld	18nH	LL1608 Toko chip inductor
L1	1.0nH	0402CS Coil Cr. inductor
L2	2.7nH	0402CS Coil Cr. inductor
C1	0.3pF	ATC 600S Chip Capacitor
C2	0.8pF	ATC 600S Chip Capacitor

Eval board material - 31mil thick Rogers 4003 with 1/2 Ounce Cu on both sides.



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S-PARAMETERS (BIASED @ 3.3V, 40mA)

Freq	S11		S21		S12		S22	
(GHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
0.60	0.875	-51.0	12.561	139.4	0.034	67.2	0.294	-40.8
0.90	0.788	-72.8	11.024	123.3	0.046	59.0	0.248	-59.5
1.20	0.707	-92.2	9.608	110.0	0.057	53.0	0.216	-76.2
1.50	0.641	-109.4	8.377	98.5	0.065	48.1	0.186	-91.7
1.80	0.590	-124.7	7.354	88.5	0.072	44.2	0.162	-106.8
2.10	0.557	-138.4	6.547	79.6	0.079	40.6	0.150	-121.3
2.40	0.532	-151.0	5.881	71.5	0.086	37.5	0.138	-133.8
2.70	0.515	-162.2	5.341	64.0	0.092	34.3	0.132	-145.4
3.00	0.501	-172.8	4.886	56.9	0.099	31.2	0.126	-155.7
3.30	0.491	178.2	4.519	50.2	0.105	28.2	0.119	-164.8
3.60	0.484	169.6	4.202	43.6	0.112	24.9	0.116	-175.0
3.90	0.484	161.3	3.950	37.2	0.118	21.5	0.110	176.0
4.20	0.483	153.4	3.728	30.7	0.125	17.9	0.107	165.7
4.50	0.489	145.3	3.525	24.1	0.131	14.0	0.110	153.9
4.80	0.494	136.9	3.340	17.5	0.137	9.8	0.115	142.7
5.10	0.503	128.7	3.173	11.1	0.143	5.6	0.125	129.9
5.40	0.515	120.5	3.020	4.5	0.148	1.2	0.141	119.8
5.70	0.528	112.3	2.874	-2.2	0.153	-3.4	0.161	110.4
6.00	0.545	104.4	2.725	-8.8	0.156	-8.0	0.185	101.6

S-PARAMETERS (BIASED @ 3.3V, 80mA)

Freq	S11		S21		S12		S22	
(GHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
0.60	0.852	-53.8	14.400	137.0	0.029	69.0	0.256	-38.6
0.90	0.755	-76.0	12.398	120.7	0.039	62.1	0.210	-55.1
1.20	0.671	-95.6	10.653	107.5	0.048	57.1	0.180	-69.8
1.50	0.605	-112.6	9.200	96.4	0.056	53.2	0.151	-82.8
1.80	0.556	-127.8	8.027	86.7	0.063	49.8	0.128	-96.3
2.10	0.525	-141.4	7.115	78.1	0.071	46.5	0.115	-109.7
2.40	0.502	-153.7	6.372	70.3	0.078	43.5	0.104	-121.0
2.70	0.487	-164.7	5.773	63.0	0.085	40.5	0.097	-132.3
3.00	0.475	-175.1	5.272	56.2	0.091	37.3	0.090	-141.3
3.30	0.465	176.1	4.868	49.6	0.098	34.3	0.083	-149.7
3.60	0.459	167.8	4.522	43.2	0.105	30.9	0.079	-159.5
3.90	0.458	159.6	4.246	37.0	0.112	27.5	0.073	-167.0
4.20	0.459	152.1	4.006	30.6	0.119	23.9	0.068	-177.9
4.50	0.464	144.2	3.787	24.2	0.126	19.9	0.069	169.0
4.80	0.469	136.1	3.588	17.8	0.132	15.7	0.071	154.1
5.10	0.479	128.2	3.408	11.5	0.138	11.5	0.079	137.9
5.40	0.492	120.1	3.246	5.1	0.144	7.0	0.094	125.7
5.70	0.506	112.2	3.094	-1.5	0.149	2.3	0.113	114.4
6.00	0.524	104.4	2.937	-8.0	0.153	-2.3	0.138	105.2

Specifications subject to change without notice
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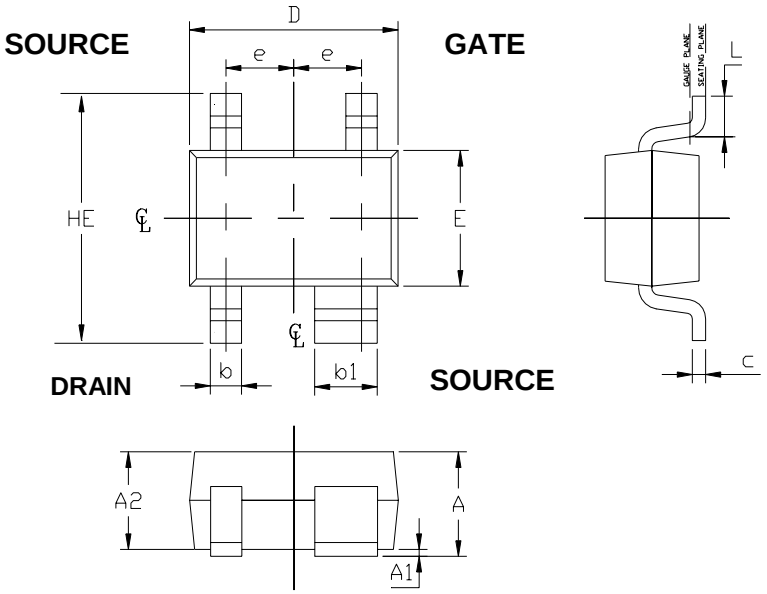
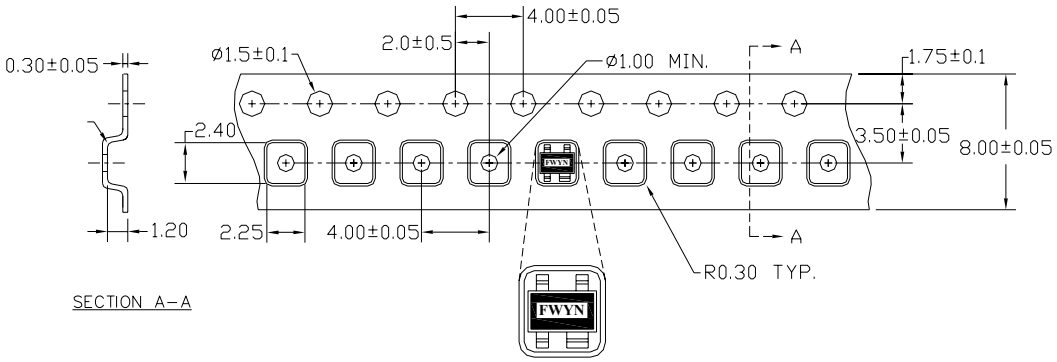
PACKAGE OUTLINE:

(dimensions in millimeters – mm)



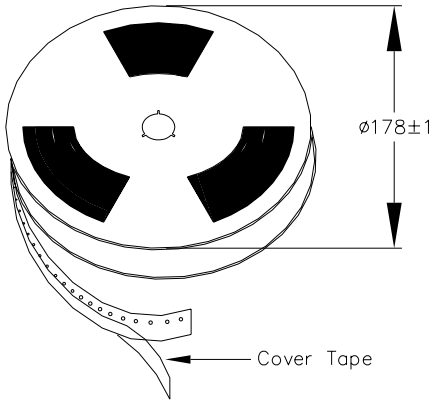
SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.65 BSC	
b	0.25	0.40
b1	0.55	0.70
c	0.10	0.18
L	0.26	0.46

TAPE DIMENSIONS AND PART ORIENTATION



DIMENSIONS ARE IN MM

- Leader tape with empty Cavities = 350mm(min.)
- Trailer tape with empty Cavities = 160mm(min.)
- Devices per reel = 3000



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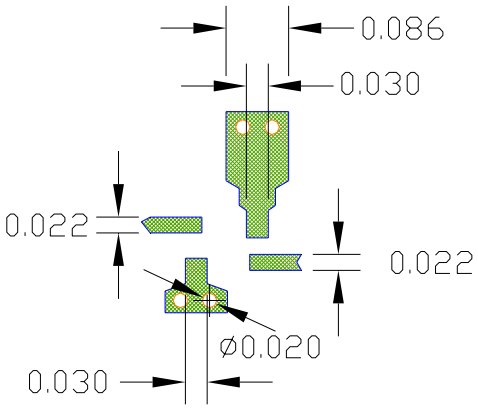
PCB Foot Print



Units in inches

Preferred Assembly Instructions:

This package is compatible with both lead free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260°C.

Handling Precautions:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD/MSL Rating:

These devices should be treated as Class 1A (250V - 500V) using the human body model as defined in JEDEC Standard No. 22-A114.

The device has a MSL rating of Level 1. To determine this rating, preconditioning was performed to the device per, the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, Moisture / Reflow sensitivity classification for non-hermetic solid state surface mount devices

Application Notes & Design Data:

Application Notes and design data including S-parameters, noise parameters and device model are available on request.

Reliability:

A MTTF of 4.2 million hours at a channel temperature of 150°C is achieved for the process used to manufacture this device.

Disclaimers:

This product is not designed for use in any space based or life sustaining/supporting equipment.

Ordering Information:

Part Number	Description
FPD750SOT343	Packaged pHEMT
FPD750SOT343E	Lead free Packaged pHEMT
FPD750SOT343CE	RoHS Compliant Packaged pHEMT with enhanced passivation (Recommended for New Designs)
EB750SOT343-BB	0.9 GHz evaluation board
EB750SOT343-BA	1.85 GHz evaluation board
EB750SOT343-BC	2.0 GHz evaluation board
EB750SOT343-BE	2.4 GHz evaluation board
EB750SOT343-BG	2.6 GHz evaluation board
EB750SOT343-AH	3.5 GHz evaluation board

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