v01.0212

# HMC897LP4E

## FILTER - TUNABLE, BAND PASS SMT 9 - 19 GHz

### Typical Applications

The HMC897LP4E is ideal for:

- Test & Measurement Equipment
- Military RADAR & EW/ECM
- SATCOM & Space
- Industrial & Medical Equipment

### Features

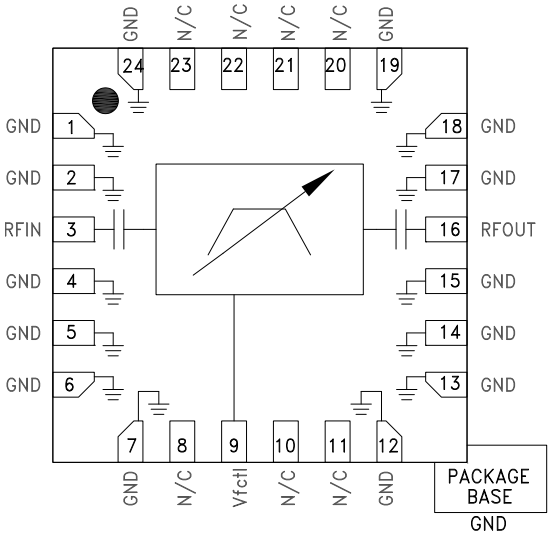
Fast Tuning Response

Excellent Wideband Rejection

Single Chip Replacement for Mechanically Tuned Designs

24 Lead 4x4 mm SMT Package

### Functional Diagram




### General Description

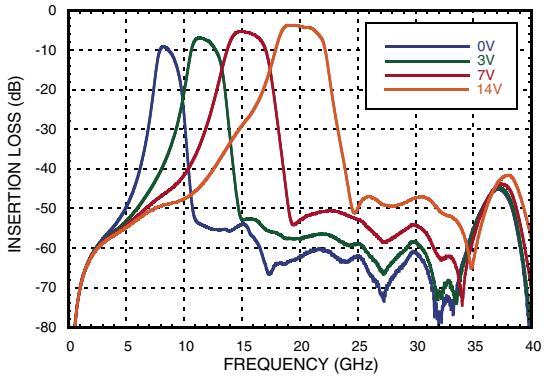
The HMC897LP4E is a MMIC band pass filter which features a user selectable passband frequency. The 3 dB filter bandwidth is approximately 18%. The 20 dB filter bandwidth is approximately 35%. The center frequency can be varied between 9 and 19 GHz by applying an analog tune voltage between 0 and 14V. This tunable filter can be used as a much smaller alternative to physically large switched filter banks and cavity tuned filters. The HMC897LP4E has excellent microphonics due to the monolithic design, and provides a dynamically adjustable solution in advanced communications applications.

### Electrical Specifications, $T_A$ = +25°C

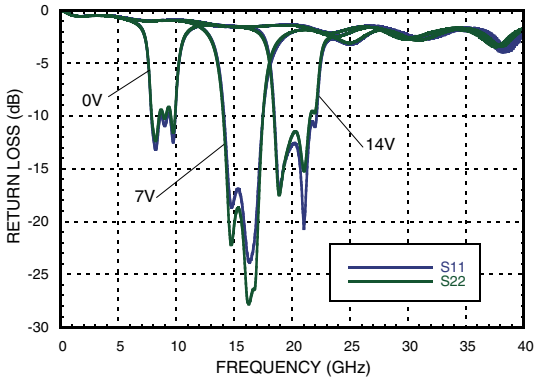
| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| $F_{center}$ Tuning Range | 9 | | 19 | GHz |
| 3 dB Bandwidth | | 18 | | % |
| Low Side Rejection Frequency (Rejection >20 dB) | | 0.81 *$F_{center}$ | | GHz |
| High Side Rejection Frequency (Rejection >20 dB) | | 1.17 *$F_{center}$ | | GHz |
| Low Side Sub-Harmonic Rejection (Rejection >40 dB) | | 0.58 *$F_{center}$ | | GHz |
| High Side Sub-Harmonic Rejection (Rejection >40 dB) | | 1.23 *$F_{center}$ | | GHz |
| Re-entry Frequency (Rejection <30 dB) | | >40 | | GHz |
| Insertion Loss | | 6.5 | | dB |
| Return Loss | | 9.5 | | dB |
| Input IP3 (Pin = 0 to +20 dBm) | | 30 | | dBm |
| Input Power @ 5° Shift In Insertion Phase (Vfctl = 0V) | | 10 | | dBm |
| Input Power @ 5° Shift In Insertion Phase (Vfctl > = 1V) | | 15 | | dBm |
| Frequency Control Voltage ($V_{fctl}$) | 0 | | 14 | V |
| Source/Sink Current ($I_{fctl}$) | | | ±1 | mA |
| Residual Phase Noise [1] (100 kHz Offset) | | -160 | | dBc/Hz |
| $F_{center}$ Drift Rate | | -1.65 | | MHz/°C |
| Tuning Characteristics [2]<br>tFULLBAND (0% Vfctl to 90% RF) | | 200 | | ns |

[1] Optimum residual phase noise performance requires the use of a low noise driver circuit.
[2] Tuning speed is dependent on driver circuit. Data measured with a high speed op-amp driver and includes driver slew rate delay.

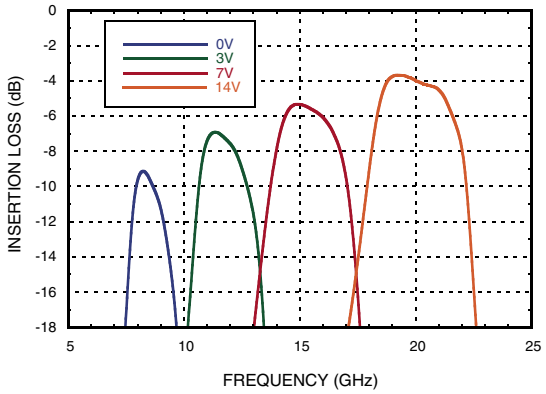
### Broadband Insertion Loss vs. Vfctl



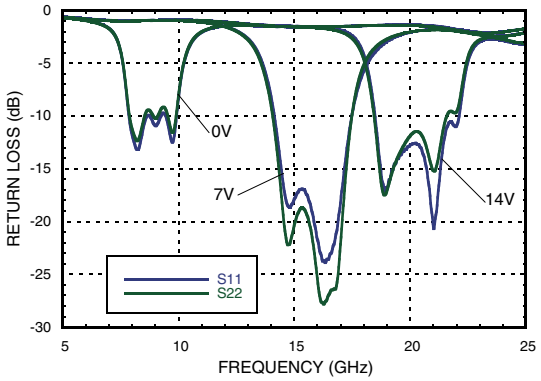

### Broadband Return Loss vs. Vfctl



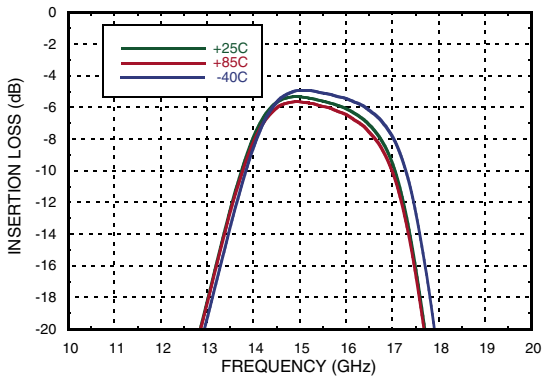

### Insertion Loss vs. Vfctl



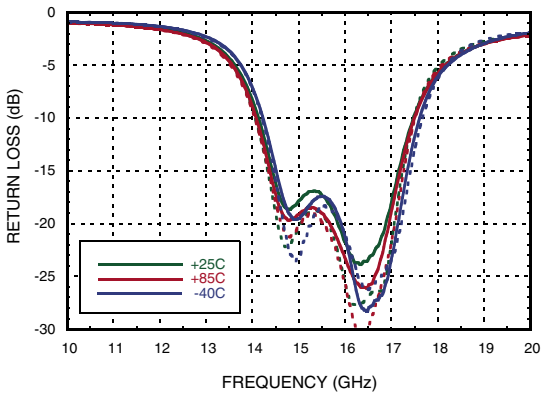

### Return Loss vs. Vfctl



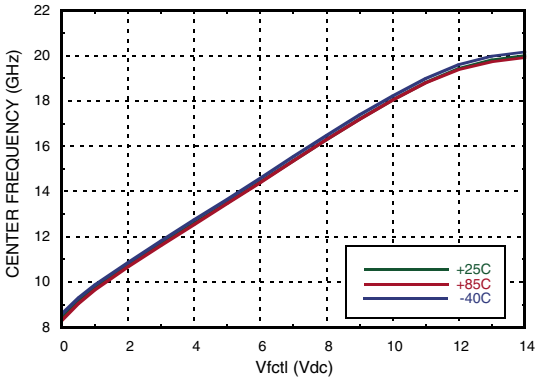

### Insertion Loss vs. Temperature, Vfctl = 7V



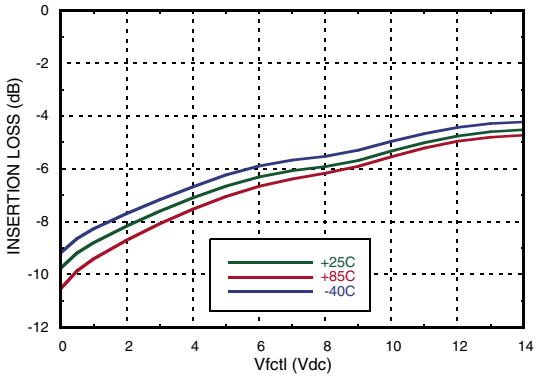

### Return Loss vs. Temperature, Vfctl = 7V



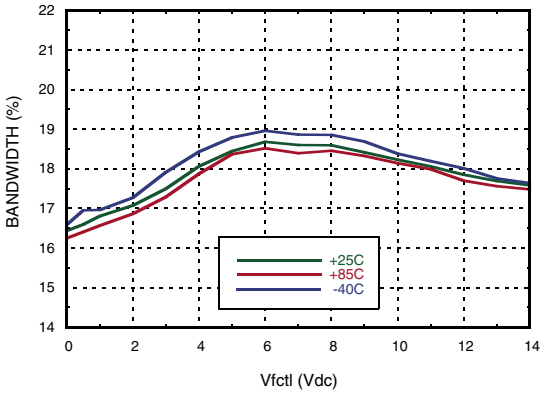
### Center Frequency vs. Temperature



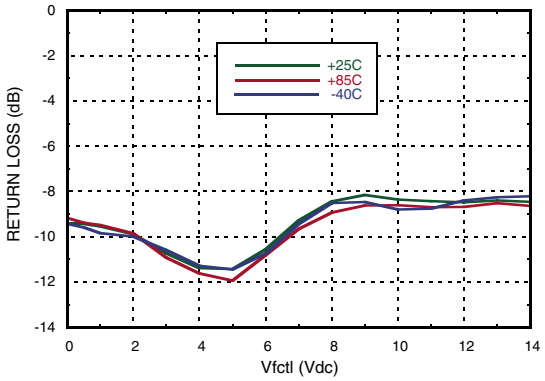

### Insertion Loss vs. Temperature



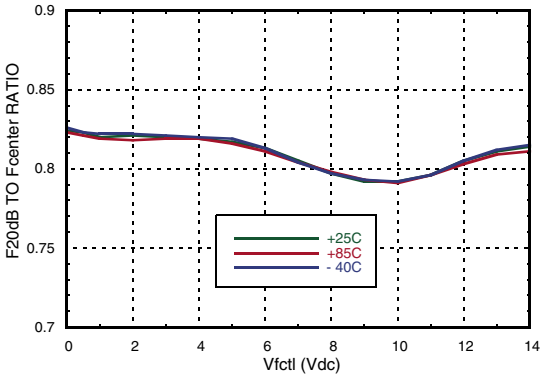

### 3 dB Bandwidth vs. Temperature



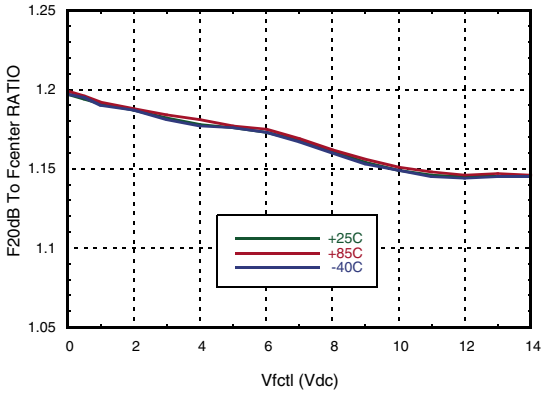

### Maximum Return Loss in a 2 dB Bandwidth vs. Temperature




### Low Side Rejection Ratio vs. Temperature [1]

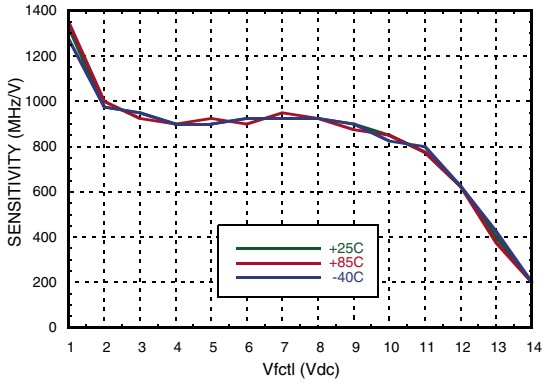



### High Side Rejection Ratio vs. Temperature [1]

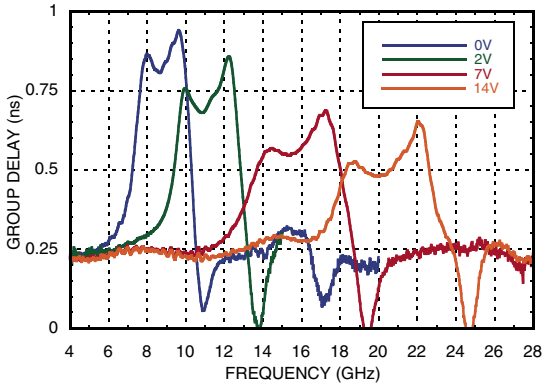



[1] Rejection ratio is defined as the ratio of the frequency at which the relative insertion loss is 20 dB to *f*center

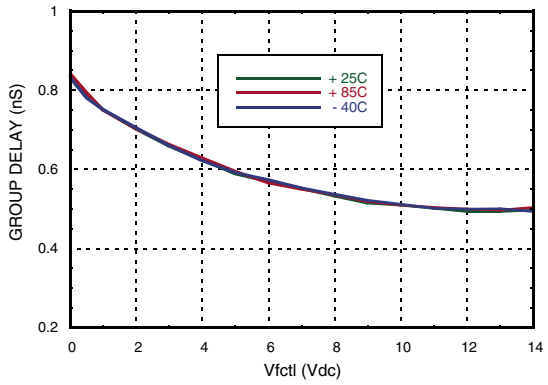
### Tuning Sensitivity vs. Temperature



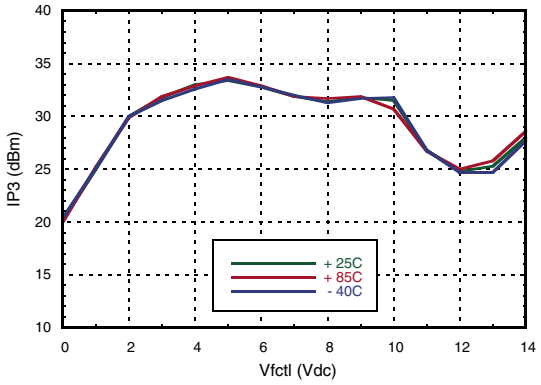

### Group Delay



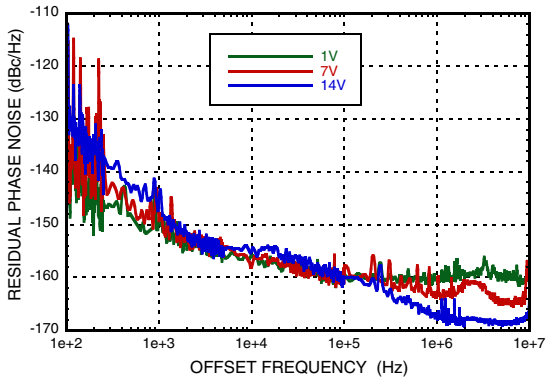

### Group Delay vs. Fcenter vs. Temperature



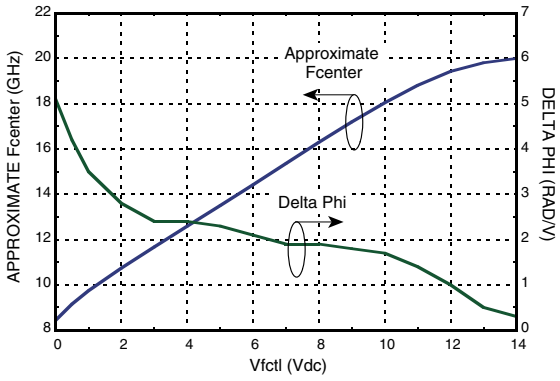

### Input IP3 vs. Temperature



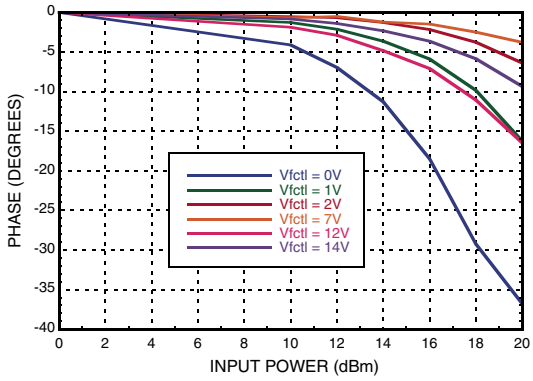

### Residual Phase Noise



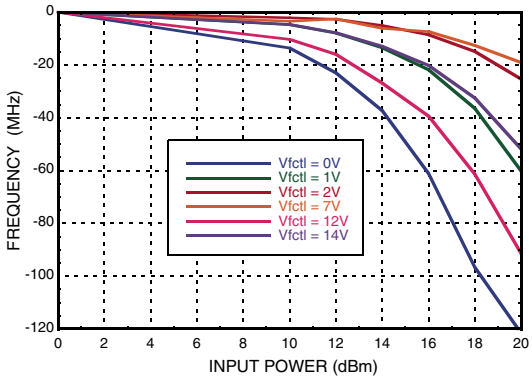

### Phase Sensitivity vs. Vfctl



### Phase Shift vs. Pin




### Frequency Shift vs. Pin




### Absolute Maximum Ratings

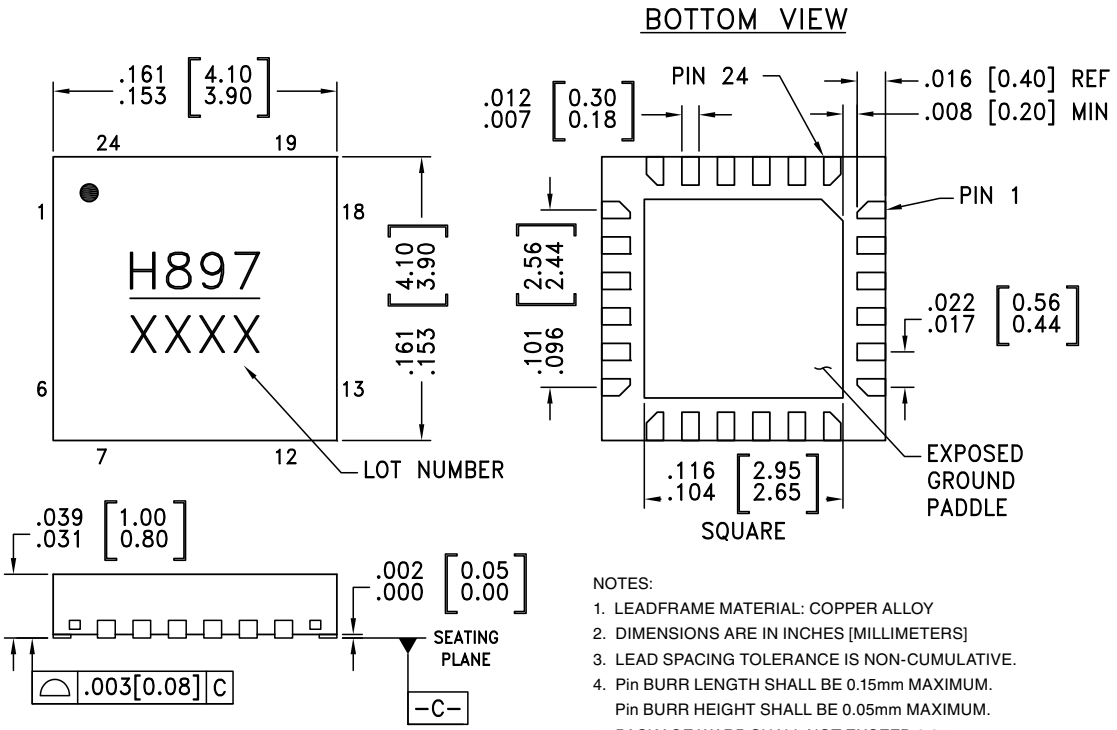
| | |
|---|---|
| Frequency Control Voltage (Vfctl) | -0.5 to +15V |
| RF Power Input | 27 dBm |
| Storage Temperature | -65 to +150 °C |
| ESD Sensitivity (HBM) | Class 1A |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

### Reliability Information

| | |
|---|---|
| Junction Temperature to Maintain 1 Million Hour MTTF | 150 °C |
| Nominal Junction Temperature (T= 85 °C and Pin = 27 dBm) | 108 °C |
| Operating Temperature | -40 to +85 °C |

## Outline Drawing




NOTES:

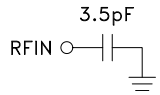
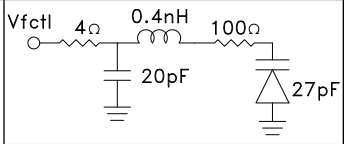
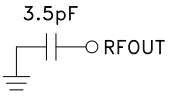
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. Pin BURR LENGTH SHALL BE 0.15mm MAXIMUM. Pin BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

## Package Information

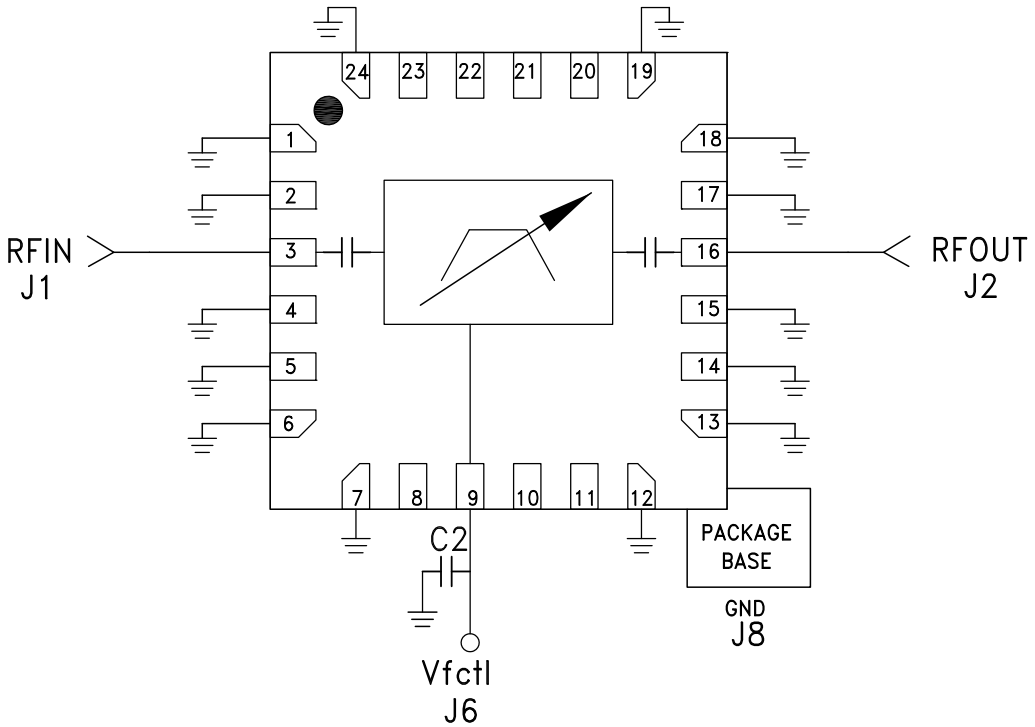
| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [1] |
|---|---|---|---|---|
| HMC897LP4E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 [2] | H897<br>XXXX |

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

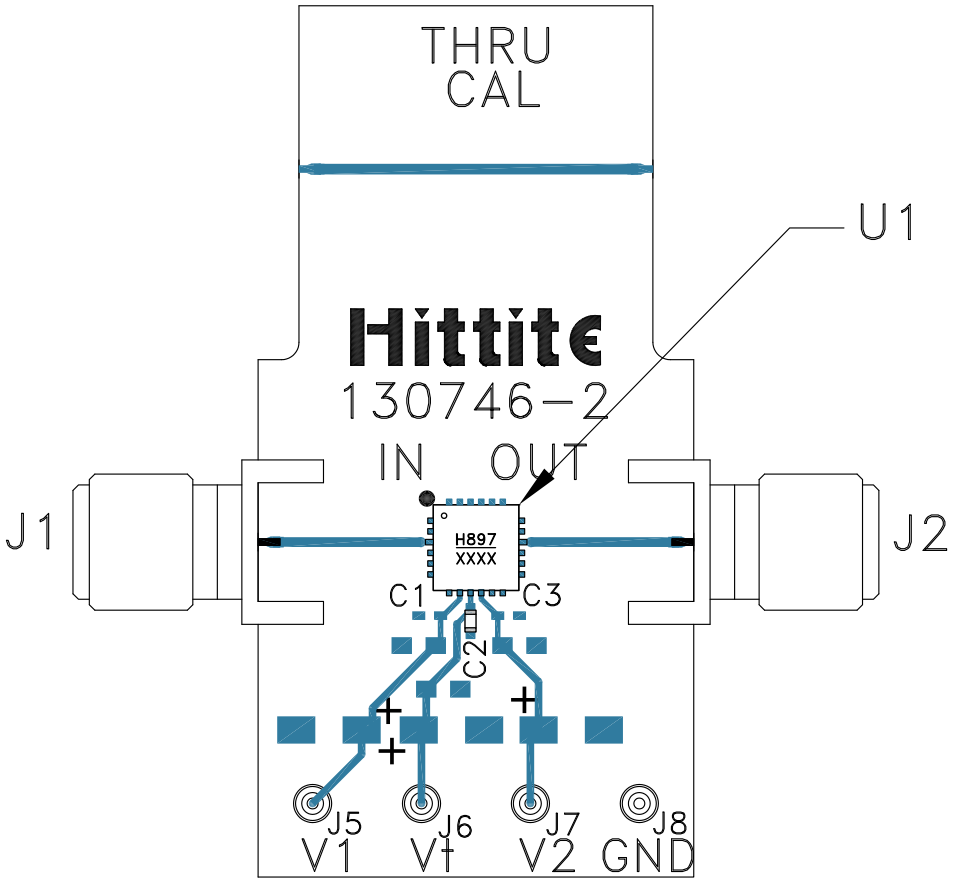
## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 8, 10, 11, 20 - 23 | N/C | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |
| 1, 2, 4 - 7, 12 - 15, 17 - 19, 24 | GND | These pins and exposed paddle must be connected to RF/DC ground. |   |
| 3 | RFIN | This pin is AC coupled and matched to 50 Ohms. |   |
| 9 | Vfctl | Center frequency control voltage. |   |
| 16 | RFOUT | This pin is AC coupled and matched to 50 Ohms. |   |

## Application Circuit



## Evaluation PCB




## List of Materials for Evaluation PCB 131086 [1]

| Item | Description |
|---|---|
| J1, J2 | PCB Mount K-Connector |
| J6, J8 | DC Pin |
| C2 | 100 pF Capacitor, 0402 Pkg. |
| U1 | HMC897LP4E Filter - Tunable |
| PCB [2] | 130746 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.