

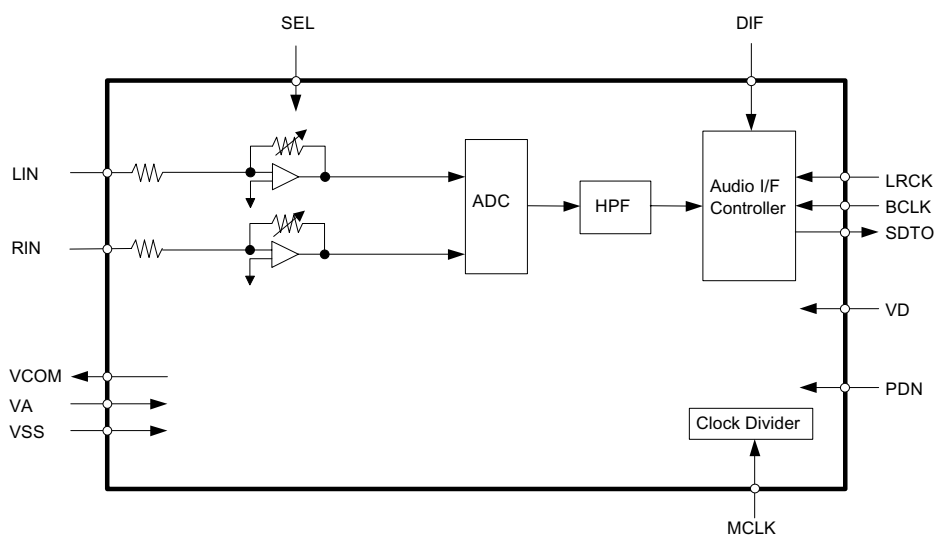


FEATURES

The AK5355 is a low voltage 16bit A/D converter for digital audio systems. The AK5355 also includes an Input Gain Amplifier, making it suitable for microphone applications or low-input signal levels. The analog signal input of the AK5355 is single-ended, eliminating the need for external filters. The AK5355 is housed in a space-saving 16-pin TSSOP package.

FEATURES

1. Resolution: 16bits
2. Recording Functions
 - Gain Amplifier (0dB / +15dB)
 - Digital HPF for DC-offset cancellation ($f_c=3.4\text{Hz}@f_s=44.1\text{kHz}$)
3. ADC Characteristics
 - Single-ended Input
 - Input Level: $1.8\text{Vpp}@V_A=3.0\text{V}$ (= 0.6 x V_A)
 - S/(N+D): 85dB
 - DR, S/N: 91dB
4. Master Clock: 256fs/384fs/512fs
5. Audio Data Format: MSB First, 2's compliment
 - 16bit MSB justified or I²S
8. Power Supply
 - V_A, V_D : 2.1 ~ 3.6V (typ. 3.0V)
9. Power Supply Current: 5mA
10. T_a = -40 ~ 85°C
11. Package: 16pin TSSOP



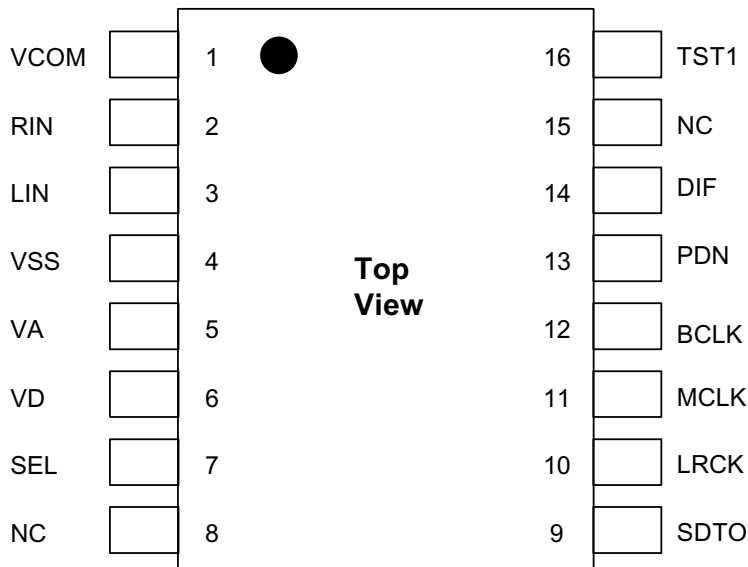
■ Ordering Guide

AK5355VT
AKD5355

-40 ~ +85°C

16pin TSSOP (0.65mm pitch)
Evaluation Board for AK5355

■ Pin Layout



PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|-----|----------|-----|--|
| 1 | VCOM | O | ADC Common Voltage Output Pin |
| 2 | RIN | I | Rch Input Pin |
| 3 | LIN | I | Lch Input Pin |
| 4 | VSS | - | Ground Pin |
| 5 | VA | - | Analog Power Supply Pin, +3.0V |
| 6 | VD | - | Digital Power Supply Pin, +3.0V |
| 7 | SEL | I | Input Gain Select Pin “L”: 0dB, “H”: +15dB |
| 8 | NC | - | NC Pin (No internal bonding) |
| 9 | SDTO | O | Audio Serial Data Output Pin |
| 10 | LRCK | I | Input/Output Channel Clock Pin |
| 11 | MCLK | I | Master Clock Input Pin |
| 12 | BCLK | I | Audio Serial Data Clock Pin |
| 13 | PDN | I | Reset & Power Down Pin “L” : Reset & Power down, “H” : Normal operation |
| 14 | DIF | I | Audio Data Format Select Pin “L”: MSB justified, “H”: I ² S |
| 15 | NC | - | NC Pin (No internal bonding) |
| 16 | TST1 | I | TEST pin (Pull-down Pin) This pin should be left floating or connected to VSS |

Note: All digital input pins should not be left floating.

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|---------------------------------|
| ABSOLUTE MAXIMUM RATINGS |
|---------------------------------|

(VSS=0V; Note 1)

| Parameter | | Symbol | Min | max | Units |
|---|---------|--------|------|--------|-------|
| Power Supply | Analog | VA | -0.3 | 4.6 | V |
| | Digital | VD | -0.3 | 4.6 | V |
| Input Current (Any Pin Except Supplies) | | IIN | - | ±10 | mA |
| Analog Input Voltage (LIN, RIN pins) | | VINA | -0.3 | VA+0.3 | V |
| Digital Input Voltage | | VIND | -0.3 | VD+0.3 | V |
| Ambient Temperature (power applied) | | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

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|---|
| RECOMMENDED OPERATING CONDITIONS |
|---|

(VSS=0V; Note 1)

| Parameter | | Symbol | min | typ | max | Units |
|--------------|------------------|--------|-----|-----|-----|-------|
| Power Supply | Analog (VA pin) | VA | 2.1 | 3.0 | 3.6 | V |
| | Digital (VD pin) | VD | 2.1 | 3.0 | VA | V |

Note 1. All voltages with respect to ground.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

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| ANALOG CHARACTERISTICS |
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(Ta=25°C; VA, VD=3.0V; fs=44.1kHz; Signal Frequency=1kHz; Measurement frequency=10Hz ~ 20kHz; unless otherwise specified)

| Parameter | min | typ | max | Units | |
|---|--------------|------|------|-------|-----------------|
| Resolution | | | 16 | bits | |
| Input PGA Characteristics (IPGA): | | | | | |
| Input Voltage (Note 2) | Gain = 0dB | 1.65 | 1.8 | 1.95 | V _{pp} |
| | Gain = +15dB | 0.29 | 0.32 | 0.35 | V _{pp} |
| Input Impedance | Gain = 0dB | 27 | 40 | | kΩ |
| | Gain = +15dB | 20 | 30 | | kΩ |
| ADC Analog Input Characteristics: (Note 3) | | | | | |
| S/(N+D) (-0.5dBFS Output) | Gain = 0dB | 75 | 85 | | dB |
| | Gain = +15dB | 70 | 80 | | dB |
| D-Range (-60dBFS Output, A-weight) | Gain = 0dB | 84 | 91 | | dB |
| | Gain = +15dB | 76 | 84 | | dB |
| S/N (A-weight) | Gain = 0dB | 84 | 91 | | dB |
| | Gain = +15dB | 76 | 84 | | dB |
| Interchannel Isolation | Gain = 0dB | 90 | 100 | | dB |
| | Gain = +15dB | 80 | 90 | | dB |
| Interchannel Gain Mismatch | Gain = 0dB | | 0.2 | 0.5 | dB |
| | Gain = +15dB | | 0.2 | 1.0 | dB |
| Power Supplies | | | | | |
| Power Supply Current: VA+VD | | | | | |
| Normal Operation (PDN="H") | | | 5 | 7.5 | mA |
| Power Down (PDN="L") (Note 4) | | | 10 | 100 | μA |

Note 2. Analog input voltage (full-scale voltage) scales with VA.

Gain = 0dB; 0.6 x VA

Gain = +15dB; 0.107 x VA

Note 3. ADC measurements are input from LIN/RIN and routed through input gain amplifier.

The internal HPF cancels the offset of input gain amplifier and ADC.

Note 4. In case of power-down mode, all digital input pins including clocks pins (MCLK, BCLK and LRCK) are held at VD or VSS. PDN pin is held at VSS.

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| FILTER CHARACTERISTICS |
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(Ta=25°C; VA, VD=2.1 ~ 3.6V; fs=44.1kHz)

| Parameter | Symbol | min | typ | max | Units | |
|---|----------------------------|------|------|------|-------|-----|
| ADC Digital Filter (Decimation LPF): | | | | | | |
| Passband (Note 5) | ±0.1dB -1.0dB -3.0dB | PB | 0 | | 17.4 | kHz |
| | | | | 20.0 | | kHz |
| | | | | 21.1 | | kHz |
| Stopband (Note 5) | SB | 27.0 | | | kHz | |
| Passband Ripple | PR | | | ±0.1 | dB | |
| Stopband Attenuation | SA | 65 | | | dB | |
| Group Delay (Note 6) | GD | | 17.0 | | 1/fs | |
| Group Delay Distortion | ΔGD | | 0 | | μs | |
| ADC Digital Filter (HPF): | | | | | | |
| Frequency Response (Note 5) | -3dB -0.5dB -0.1dB | FR | | 3.4 | | Hz |
| | | | | 10 | | Hz |
| | | | | 22 | | Hz |

Note 5. The passband and stopband frequencies scale with fs (sampling frequency).

For examples, PB=0.454 x fs(@ADC: -1.0dB).

Note 6. The calculated delay time caused by digital filtering. This time is from the input of an analog signal to setting the 16bit data of both channels to the output register of the ADC and includes the group delay of the HPF.

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| DC CHARACTERISTICS |
|---------------------------|

(Ta=25°C; VA, VD=2.1 ~ 3.6V)

| Parameter | Symbol | min | typ | max | Units |
|--|--------|--------|-----|-------|-------|
| High-Level Input Voltage (Except for TST1 pin) | VIH | 75%VD | - | - | V |
| Low-Level Input Voltage (Except for TST1 pin) | VIL | - | - | 25%VD | V |
| High-Level Output Voltage (Iout=-80μA) | VOH | VD-0.4 | - | - | V |
| Low-Level Output Voltage (Iout=80μA) | VOL | - | - | 0.4 | V |
| Input Leakage Current (Note 7) | Iin | - | - | ± 10 | μA |

Note 7. TST1 pin is pulled-down internally (typ. 100kΩ)

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| SWITCHING CHARACTERISTICS |
|----------------------------------|

(Ta=25°C; VA, VD=2.1 ~ 3.6V; CL=20pF)

| Parameter | Symbol | min | typ | max | Units |
|------------------------------------|--------|-----------|---------|----------|-------|
| Control Clock Frequency | | | | | |
| Master Clock (MCLK) | | | | | |
| 256fs: Frequency | fCLK | 2.048 | 11.2896 | 12.8 | MHz |
| Pulse Width Low | tCLKL | 28 | | | ns |
| Pulse Width High | tCLKH | 28 | | | ns |
| 384fs: Frequency | fCLK | 3.072 | 16.9344 | 19.2 | MHz |
| Pulse Width Low | tCLKL | 23 | | | ns |
| Pulse Width High | tCLKH | 23 | | | ns |
| 512fs: Frequency | fCLK | 4.096 | 22.5792 | 25.6 | MHz |
| Pulse Width Low | tCLKL | 16 | | | ns |
| Pulse Width High | tCLKH | 16 | | | ns |
| Channel Clock (LRCK) Frequency | fs | 8 | 44.1 | 50 | kHz |
| Duty Cycle | duty | 45 | | 55 | % |
| Audio Interface Timing | | | | | |
| BCLK Period | tBLK | 312.5 | | | ns |
| BCLK Pulse Width Low | tBLKL | 130 | | | ns |
| Pulse Width High | tBLKH | 130 | | | ns |
| BCLK “↓” to LRCK | tBLR | -tBLKH+50 | | tBLKL-50 | ns |
| LRCK Edge to SDTO (MSB) | tDLR | | | 80 | ns |
| BCLK “↓” to SDTO | tDSS | | | 80 | ns |
| Reset / Initializing Timing | | | | | |
| PDN Pulse Width | tPW | 150 | | | ns |
| PDN “↑” to SDTO (Note 8) | tPWV | | 4128 | | 1/fs |

Note 8. This is the number of LRCK rising after the PDN pin is pulled high.

■ Timing Diagram

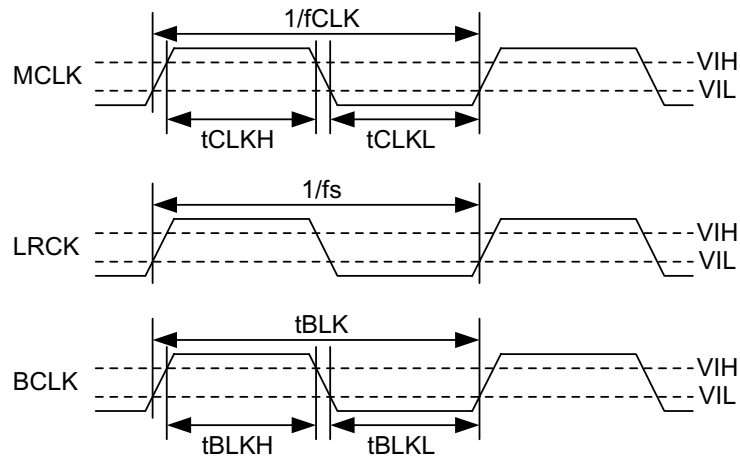


Figure 1. Clock Timing

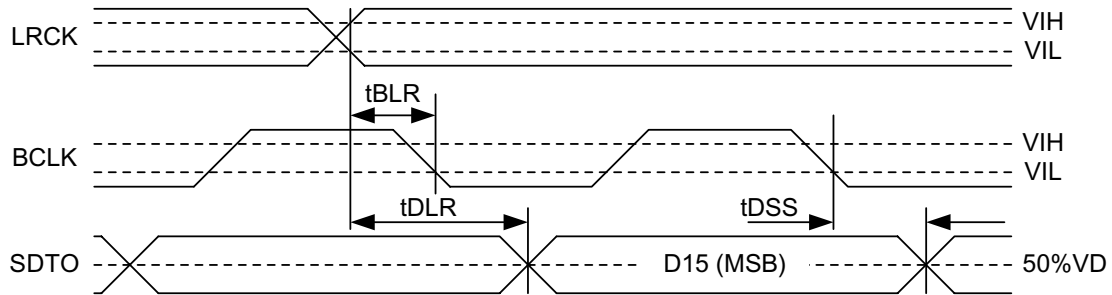


Figure 2. Audio Data Input/Output Timing (Audio I/F = No.0)

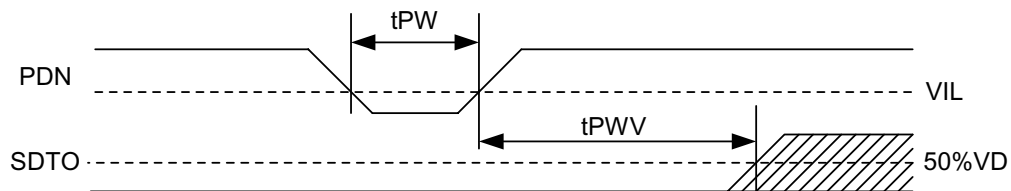


Figure 3. Reset Timing

OPERATION OVERVIEW

■ System Clock

The clocks required to operate are MCLK (256fs/384fs/512fs), LRCK (fs) and BCLK (32fs~). The master clock (MCLK) should be synchronized with LRCK. The phase between these clocks does not matter. The frequency of MCLK can be input as 256fs, 384fs or 512fs. When the 384fs or 512fs is input, the internal master clock is divided into 2/3 or 1/2 automatically.

*fs is sampling frequency.

All external clocks (MCLK, BCLK and LRCK) should always be present whenever the ADC is in operation. If these clocks are not provided, the AK5355 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK5355 should be placed in power-down mode.

■ Audio Data I/F Format

The SDTO, BCLK and LRCK pins are connected to an external controller. The audio data format has two modes, MSB-first and 2's compliment. The data format is set using the DIF pin.

| No. | DIF pin | SDTO (ADC) | LRCK | BCLK | Figure |
|-----|---------|-----------------------------|--------------------|--------|----------|
| 0 | L | 16bit MSB justified | Lch: "H", Rch: "L" | ≥ 32fs | Figure 4 |
| 1 | H | I ² S Compatible | Lch: "L", Rch: "H" | ≥ 32fs | Figure 5 |

Table 1. Audio Data Format

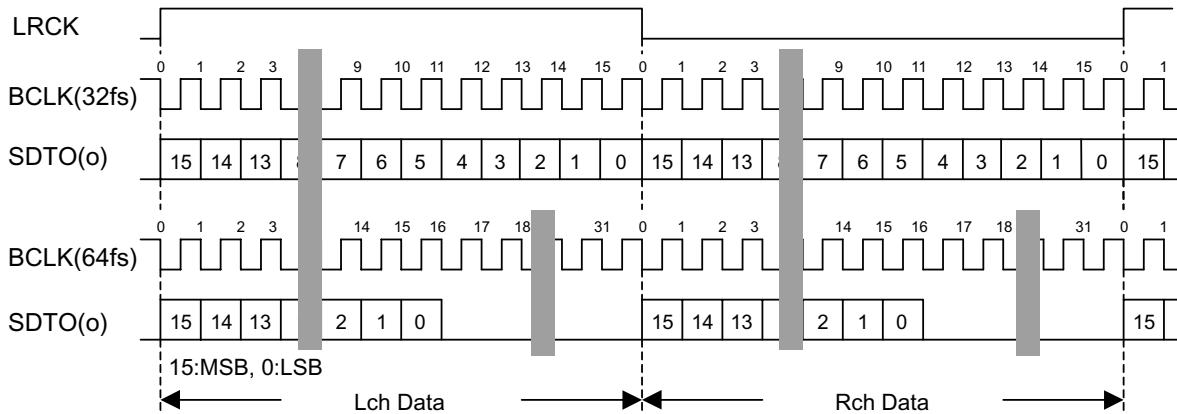


Figure 4. Audio Data Timing (No.0)

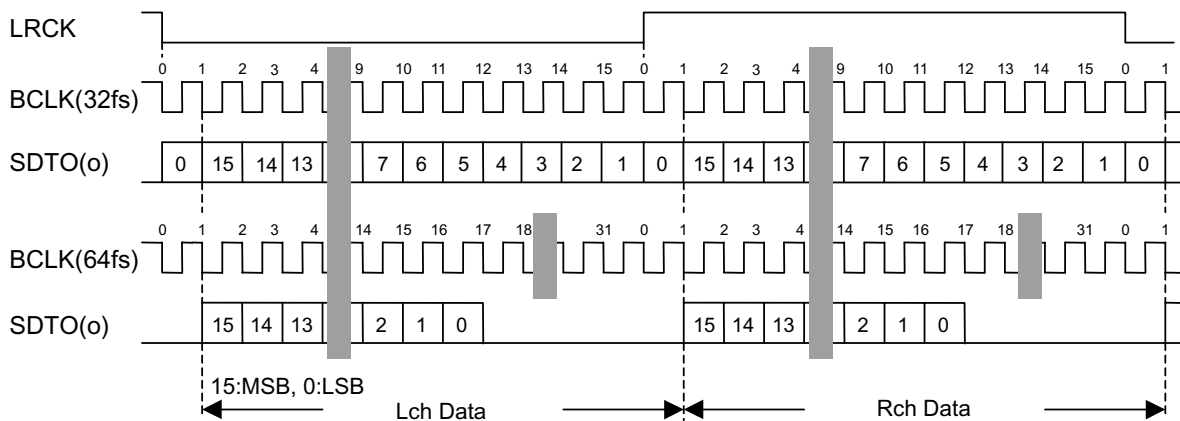


Figure 5. Audio Data Timing (No. 1)

■ Digital High Pass Filter

The AK5355 has a Digital High Pass Filter (HPF) to cancel DC-offset in both the ADC and input gain amplifier. The cut-off frequency of the HPF is 3.4Hz at $f_s=44.1\text{kHz}$. This cut-off frequency scales with the sampling frequency (f_s).

■ Input Gain Amplifier

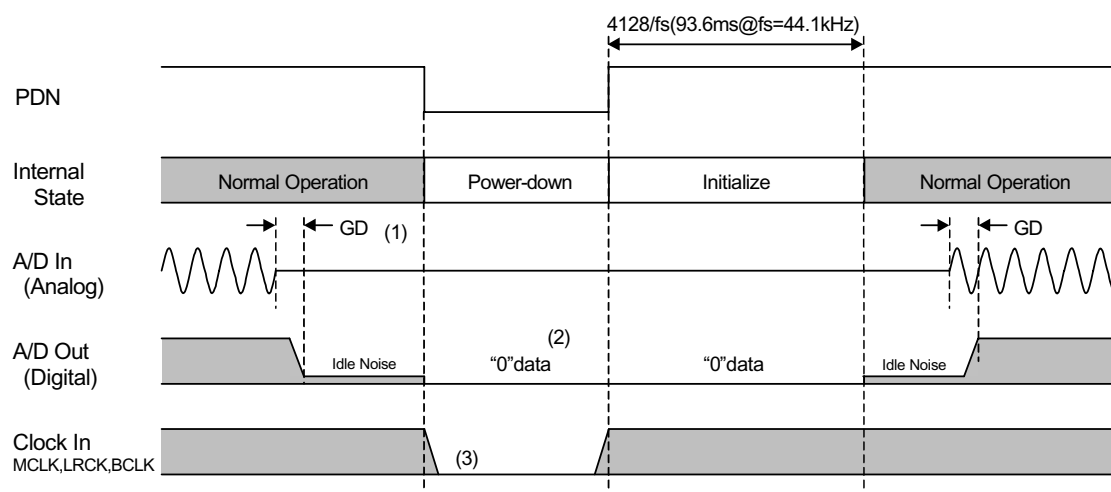
The AK5355 includes an input gain amplifier. The gain can be changed to 0dB or +15dB by using the SEL pin. Input impedance is 40k Ω typically.

| SEL pin | Gain |
|---------|-------|
| L | 0dB |
| H | +15dB |

Table 2. Input Gain Amplifier

■ Power down

The AK5355 is placed in the power-down mode by bringing PDN "L". The digital filter is also reset at the same time. This reset should always be done after power-up. An analog initialization cycle starts after exiting the power-down mode. The output data SDTO becomes available after 4128 cycles of LRCK clock. During initialization, the ADC digital data outputs of both channels are forced to a 2's complement "0". The ADC outputs settle to the data corresponding to the input signals at the end of initialization (Settling time equals the group delay time approximately).



Notes:

- (1) Digital output corresponding to the analog input is delayed by the Group Delay amount (GD).
- (2) A/D output is "0" data in the power-down state.
- (3) When the external clocks (MCLK, BCLK and LRCK) are stopped, the AK5355 should be placed in the power-down state.

Figure 6. Power-down/up sequence example

■ System Reset

The AK5355 should be reset once by bringing PDN "L" upon power-up. The AK5355 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK5355 is in the power-down mode until MCLK and LRCK are input.

SYSTEM DESIGN

Figure 7 shows the system connection diagram. An evaluation board [AKD5355] is available which demonstrates the application circuit, optimum layout, power supply arrangements and measurement results.

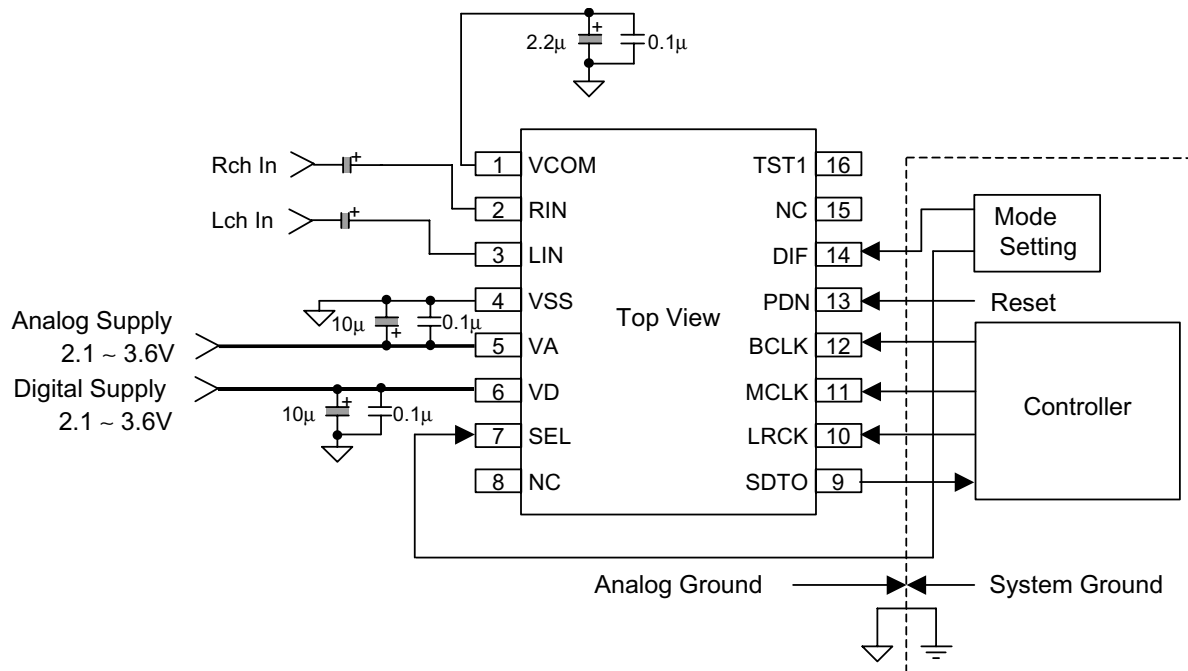


Figure 7. System Connection Diagram Example

■ MIC Device Connection Example

Figure 8 shows the connection example of MIC Device. In this case, a mono microphone is connected to LIN pin the AK5355. Unused RIN pin can be open. The power supply for the microphone is provided via 4.4kΩ (2.2kΩ + 2.2kΩ) from analog power supply. The power supply noise provided to the microphone should be care because the microphone gain is usually high, around 40dB. In Figure 8, 1st order LPF by 2.2kΩ and 10μF is inserted between the power supply and the microphone.

The AK5355 has a gain of +15dB in analog stage. However, as the usual application needs a gain of around 40dB or 50dB, the shortage of gain, 25dB or 35dB, should be covered by digital processing like DSP. The total S/N in each gain level is shown in Table 3

| Analog Gain | Digital Gain | S/N |
|-------------|--------------|------|
| +15dB | 0dB | 83dB |
| +15dB | +25dB | 58dB |
| +15dB | +35dB | 48dB |

Table 3. S/N of each gain level

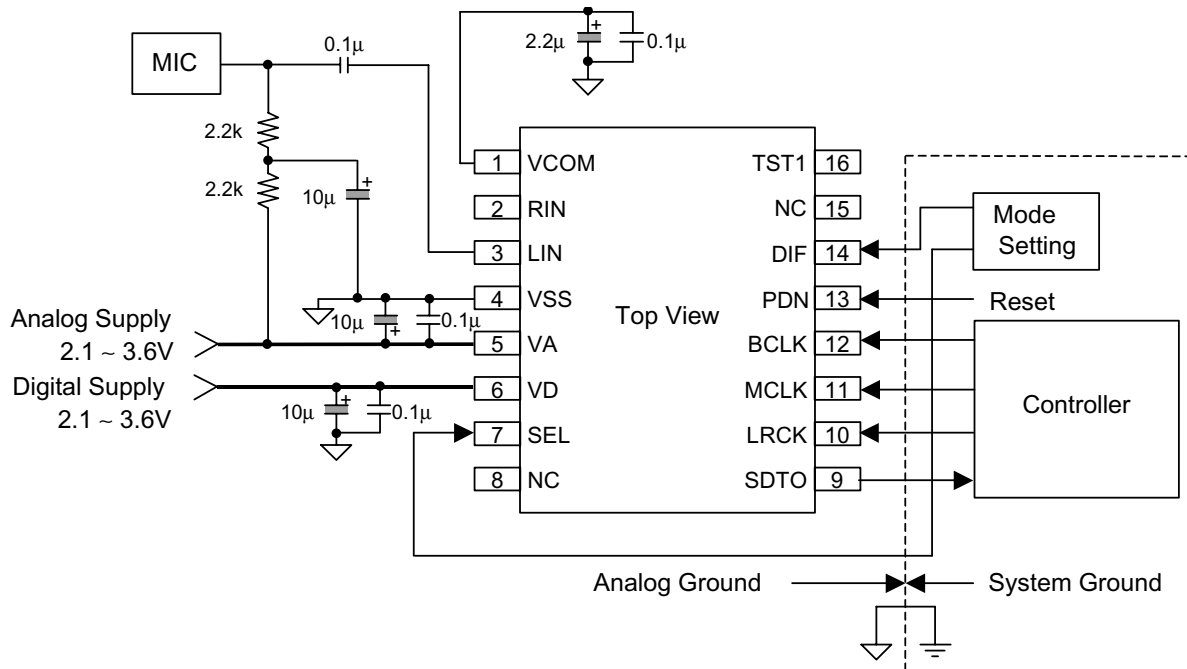


Figure 8. MIC Device Connection Example

1. Grounding and Power Supply Decoupling

The AK5355 requires careful attention to power supply and grounding arrangements. VA is usually supplied from the analog supply in the system. VD is a power supply pin to interface with the external ICs and is supplied from the digital supply in the system. VSS of the AK5355 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5355 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

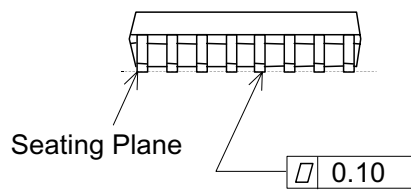
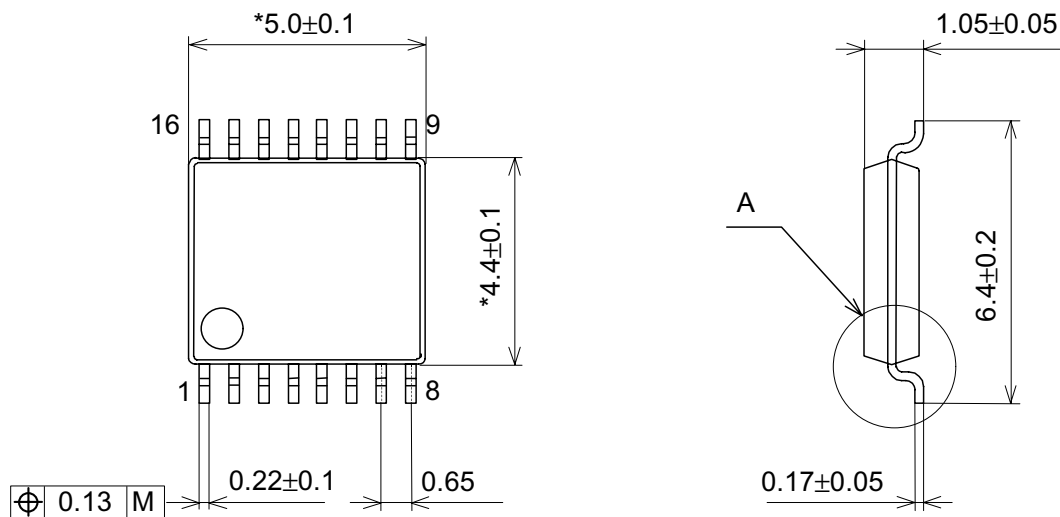
The input to VA Voltage sets the analog input range. A 0.1 μ F ceramic capacitor and a 10 μ F electrolytic capacitor are normally connected to VA and VSS pins. VCOM is a signal ground of this chip. An electrolytic 2.2 μ F in parallel with a 0.1 μ F ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clock, should be kept away from the VA, VD and VCOM pins in order to avoid unwanted coupling into the AK5355.

3. Analog Inputs

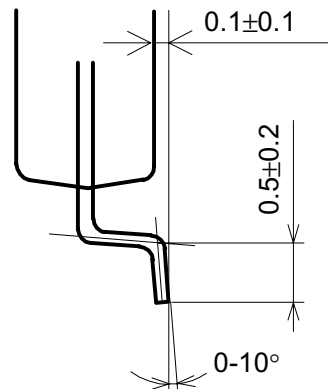
The analog inputs are single-ended and the input resistance is 40k Ω (typ). The input signal range scales with nominally (0.6 x VA) Vpp (typ) @ GAIN = 0dB centered around the internal common voltage (typ. 0.45 x VA). Usually, the input signal cuts DC with a capacitor. The cut-off frequency is $f_c = (1/2\pi RC)$. The ADC output data format is 2's complement. The DC offset including the ADC's own DC offset is removed by the internal HPF ($f_c = 3.4\text{Hz} @ f_s = 44.1\text{kHz}$).

PACKAGE

16pin TSSOP (Unit: mm)



Detail A

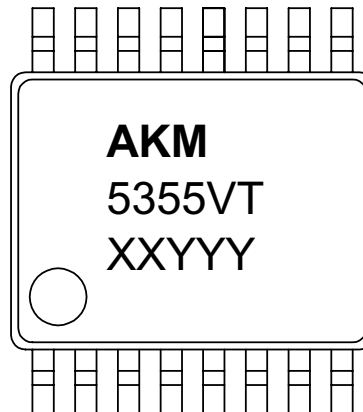


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

| | |
|-------------------------------|------------------------|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

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|----------------|
| MARKING |
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- 1) Pin #1 indication
- 2) Date Code : XXYYYY (5 digits)
 XX : Lot#
 YYY : Date Code
- 3) Marketing Code : 5355VT
- 4) Asahi Kasei Logo

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