AK5356

Low Power 20-Bit ADC with MIC-Amp & PGA

GENERAL DESCRIPTION

The AK5356 is a low voltage 20bit A/D converter for digital audio system. The AK5356 also includes microphone amplifier and analog input PGA, making it suitable for microphone applications or low-input signal levels. As digital power supply of the AK5356 corresponds to 1.8V, the interface with microprocessor can operate at low voltage. The AK5356 is housed in a space-saving 28-pin QFN package.

FEATURES

1. MIC Block
- **MIC Power**
- **Pre-Amplifier (+13dB / +18dB / +28dB / +33dB)**

2. 20bit 2ch ADC
- **2-Input Stereo Selector**
- **Analog Input PGA: +28dB ~ - 52dB, Mute**
- **S/(N+D): 84dB**
- **DR, S/N: 89dB**
- **Monaural Mixing**
- **Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)**

3. 3-wire Serial Control I/F

4. Master Clock: 256fs/384fs

5. Audio Data Format: MSB First, 2's compliment
- **16/20bit MSB justified or 16/20bit I^2S compatible**

6. Power Supply Voltage
- **AVDD: 2.0 ~ 3.3V**
- **MVDD: 2.4 ~ 3.3V**
- **DVDD: 1.8 ~ 3.3V**

7. Power Supply Current
- **MIC Block: 3.4mA**
- **IPGA+ADC: 6mA**

8. Ta = - 40 ~ 85°C

9. Package: 28pin QFN

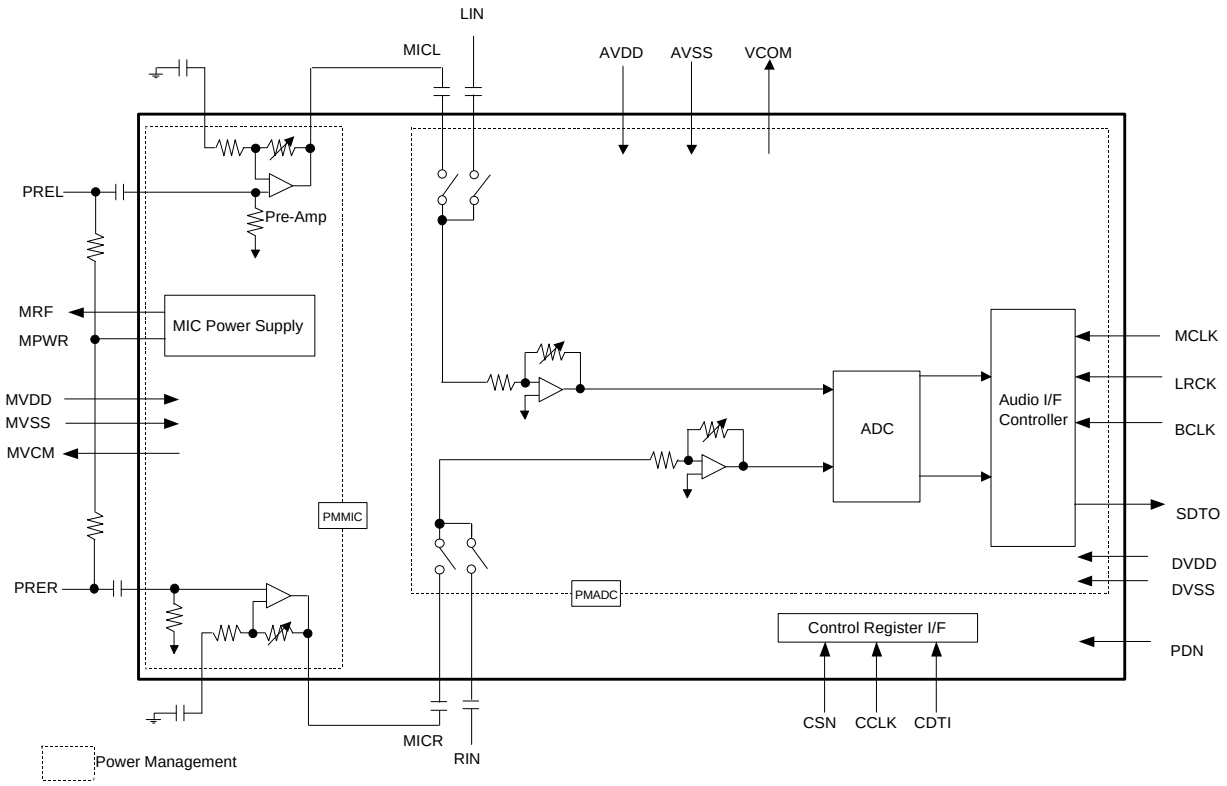
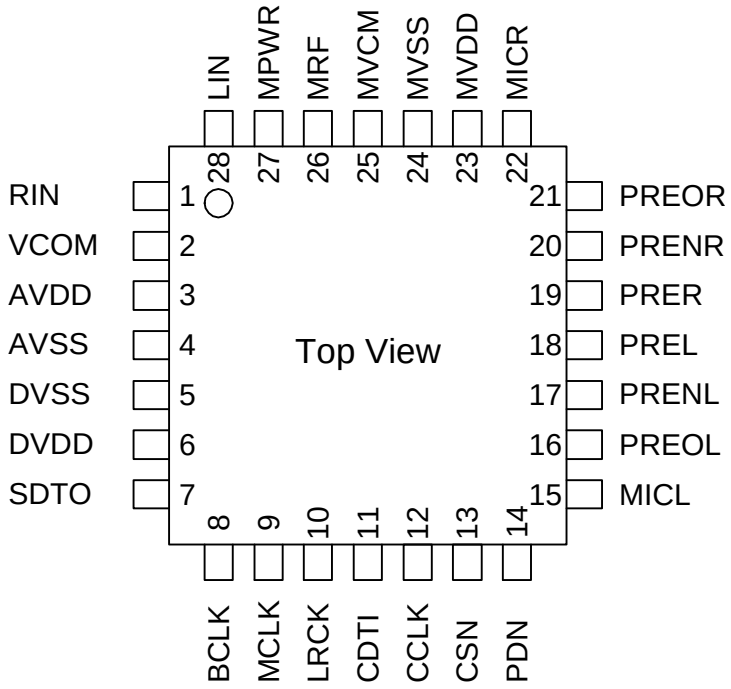


Figure 1. AK5356 Block Diagram

■ Ordering Guide

AK5356VN	-40 ~ +85°C	28pin QFN (0.5mm pitch)
AKD5356	Evaluation Board for AK5356	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	RIN	I	Rch Line Input Pin
2	VCOM	O	ADC Common Voltage Output Pin
3	AVDD	-	Analog Power Supply Pin, +2.5V
4	AVSS	-	Analog Ground Pin
5	DVSS	-	Digital Ground Pin
6	DVDD	-	Digital Power Supply Pin, +2.5V
7	SDTO	O	Audio Serial Data Output Pin
8	BCLK	I	Audio Serial Data Clock Pin
9	MCLK	I	Master Clock Input Pin
10	LRCK	I	Input/Output Channel Clock Pin
11	CDTI	I	Control Data Input Pin
12	CCLK	I	Control Clock Input Pin
13	CSN	I	Chip Select Pin
14	PDN	I	Reset & Power Down Pin "L": Reset & Power down, "H": Normal operation
15	MICL	I	Lch MIC Input Pin
16	PREOL	O	Lch Pre-Amp Output Pin
17	PRENL	I	Lch Pre-Amp Negative Input Pin
18	PREL	I	Lch Pre-Amp Positive Input Pin
19	PRER	I	Rch Pre-Amp Positive Input Pin
20	PRENR	I	Rch Pre-Amp Negative Input Pin
21	PREOR	O	Rch Pre-Amp Output Pin
22	MICR	I	Rch MIC Input Pin
23	MVDD	-	MIC Block Power Supply Pin, +2.7V
24	MVSS	-	MIC Block Ground Pin
25	MVCM	O	MIC Block Common Voltage Output Pin
26	MRF	O	MIC Power Supply Ripple Filter Pin
27	MPWR	O	MIC Power Supply Pin
28	LIN	I	Lch Line Input Pin

Note: All digital input pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS, MVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supply	Analog	AVDD	-0.3	4.6	V
	MIC	MVDD	-0.3	4.6	V
	Digital	DVDD	-0.3	4.6	V
	| DVSS – AVSS | (Note 2)	ΔGND1	-	0.3	V
	| MVSS – AVSS | (Note 2)	ΔGND2	-	0.3	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA1	-0.3	AVDD+0.3	V
(Note 4)		VINA2	-0.3	MVDD+0.3	V
Digital Input Voltage (Note 5)		VIND	-0.3	DVDD+0.3	V
Ambient Temperature (power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS and MVSS must be connected to the same analog ground plane.
Note 3. MICL, MICR, LIN and RIN pins
Note 4. PREL, PRER, PRENL and PRENR pins
Note 5. MCLK, BCLK, LRCK, CSN, CCLK, CDTI and PDN pins

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, MVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supply	Analog	AVDD	2.0	2.5	3.3	V
	MIC	MVDD	2.4	2.7	3.3	V
	Digital	DVDD	1.8	2.5	AVDD	V

Note 1. All voltages with respect to ground

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.5V, MVDD=2.7V; AVSS, DVSS, MVSS=0V; fs=44.1kHz; Signal Frequency =1kHz; Measurement Frequency=10Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Pre-Amp Characteristics:					
Input Resistance	Positive Input Pin (Note 6)	50	100	200	kΩ
	Negative Input Pin (Note 7)	100	190	400	Ω
Gain Error (+13dB, +18dB, +28dB, +33dB)		-1.5	0	+1.5	dB
Maximum Output Voltage(Gain=+13dB,+18dB,+28dB,+33dB) (THD+N ≤ 0.1%) (Note 8)		-3	-1.5		dBV
S/(N+D) (Vout = -29.2dBV)	Gain = +33dB	54	60		dB
	Gain = +28dB	–	65	–	dB
	Gain = +18dB	–	74	–	dB
	Gain = +13dB	–	78	–	dB
Output Noise Voltage (No Input, Rg = 600Ω, A-weighted)	Gain = +33dB		-91	-86	dBV
	Gain = +28dB	–	-96	–	dBV
	Gain = +18dB	–	-105	–	dBV
	Gain = +13dB	–	-109	–	dBV
Interchannel Gain Mismatch (Gain = +13dB, +18dB, +28dB, +33dB)				0.5	dB
Interchannel Isolation	Gain = +33dB	75	90		dB
	Gain = +28dB, +18dB, +13dB	–	100	–	dB
Load Resistance		5			kΩ
Load Capacitance				10	pF
Power Supply Rejection (Note 9)	Gain = +33dB	–	46	–	dB
	Gain = +28dB	–	52	–	dB
	Gain = +18dB	–	64	–	dB
	Gain = +13dB	–	73	–	dB
MIC Power Characteristics:					
Output Voltage (No Load) (Note 10)		2.05	2.16	2.27	V
Output Power Supply Current				1	mA
IPGA Characteristics:					
Input Resistance (LIN, RIN, MICL, MICR pins)		6.3	9	15	kΩ
Step Size	+28dB ~ -8dB	0.1	0.5	1	dB
	-8dB ~ -16dB	0.1	1	2	dB
	-16dB ~ -32dB	0.1	2	4	dB
	-32dB ~ -40dB	-	2	-	dB
	-40dB ~ -52dB	-	4	-	dB
ADC Characteristics: (Note 11)					
Resolution				20	bits
Input Voltage (Note 12)		1.35	1.5	1.65	Vpp
S/(N+D) (-0.5dBFS Input)	IPGA = 0dB	74	84		dB
	IPGA= +28dB	–	70	–	dB
D-Range (-60dBFS Input, A-weighted)	IPGA = 0dB	82	89		dB
	IPGA= +28dB	–	79	–	dB
S/N (A-weighted)	IPGA = 0dB	82	89		dB
	IPGA= +28dB	–	79	–	dB
Interchannel Isolation (Note 13)	IPGA = 0dB	90	100		dB
	IPGA= +28dB	–	75	–	dB
Interchannel Gain Mismatch	IPGA = 0dB			0.5	dB
	IPGA= +28dB	–	0.5	–	dB

Parameter	min	typ	max	Units
Power Supplies				
Power Supply Voltage:				
Normal Operation (PDN="H") (Note 14)				
MVDD (Note 15)		3.4	5	mA
AVDD+DVDD		6	9	mA
Power-Down Mode (PDN="L") (Note 16)				
MVDD + AVDD + DVDD		10	100	μA

Note 6. PREL and PRER pins
Note 7. PRENL and PRENR pins. Gain of Pre-Amp is +33dB. Input resistance of Pre-Amp is changed by gain.
Gain = +13dB: 1.9kΩ(typ), Gain = +18dB: 1.1kΩ(typ), Gain = +28dB: 340Ω(typ)
Note 8. A maximum output voltage is the value which fills "THD+N ≤ 0.1%". It is almost in proportion to MVDD voltage.
-1.5dBV = 2.38Vpp = (MVDD x 0.88)Vpp (typ)
Note 9. PSR is applied to MVDD with 1kHz, 50mVpp.
Note 10. Output voltage is proportional to MVDD voltage and it is typically (MVDD x 0.8) V.
Note 11. ADC is input from MICL/MICR or LIN/RIN and it measures included in IPGA. Internal HPF cancels the offset of IPGA and ADC.
Note 12. Analog input voltage (Full-scale voltage: IPGA = 0dB) is proportional to AVDD voltage.
IPGA = ADC = (0.6 x AVDD) Vpp (typ)
Note 13. This value is interchannel isolation between LIN and RIN or between MICL and MICR.
Note 14. All blocks in the AK5356 are powered-up. (PMMIC=PMADC= "1")
Note 15. MPWR pin supplies 0mA.
Note 16. In case of power-down mode, all digital input pins including clocks pins (MCLK, BCLK and LRCK) are held at DVDD or DVSS. PDN pin is held at DVSS.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=2.0 ~ 3.3V, DVDD=1.8 ~ 3.3V, MVDD=2.4~ 3.3V, fs=44.1kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (LPF):						
Passband (Note 17)	±0.1dB	PB	0		17.4	kHz
	-1.0dB			20.0		kHz
	-3.0dB			21.1		kHz
Stopband (Note 17)		SB	27.0			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 18)		GD		17.0		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 17)	-3dB	FR		3.4		Hz
	-0.5dB			10		Hz
	-0.1dB			22		Hz

Note 17. The passband and stopband frequencies scale with fs (sampling frequency).
For example, PB=0.454 x fs (@ -1.0dB).

Note 18. The calculated delay time caused by digital filtering. This time from the input of an analog signal to setting the 20bit data of both channels to the output register of the ADC and includes the group delay of the HPF.

DC CHARACTERISTICS

(Ta=25°C; AVDD=2.0 ~ 3.3V, DVDD=1.8 ~ 3.3V, MVDD=2.4~ 3.3V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	75%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	25%DVDD	V
High-Level Output Voltage Iout = -80μA	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage Iout = 80μA	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=2.0 ~ 3.3V, DVDD=1.8 ~ 3.3V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing (MCLK)					
256fs: Frequency	fCLK	2.048	11.2896	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs: Frequency	fCLK	3.072	16.9344	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
LRCK Timing					
Frequency	fs	8	44.1	50	kHz
Duty Cycle	Duty	45		55	%
Serial Interface Timing					
BCLK Period	tBLK	312.5			ns
BCLK Pulse Width Low	tBLKL	130			ns
Pulse Width High	tBLKH	130			ns
BCLK "↓" to LRCK edge	tBLR	-tBLKH+50		tBLKL-50	ns
LRCK to SDTO (MSB) (Note 19)	tDLR			80	ns
BCLK "↓" to SDTO	tDSS			80	ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Power-down & Reset Timing					
PDN Pulse Width	tPW	150			ns
PDN"↑" to SDTO Delay (Note 20)	tPWV		4128		1/fs

Note 19. Except for I^2S mode.
Note 20. This is the number of LRCK rising after PDN pin is pulled high.

■ Timing Diagram

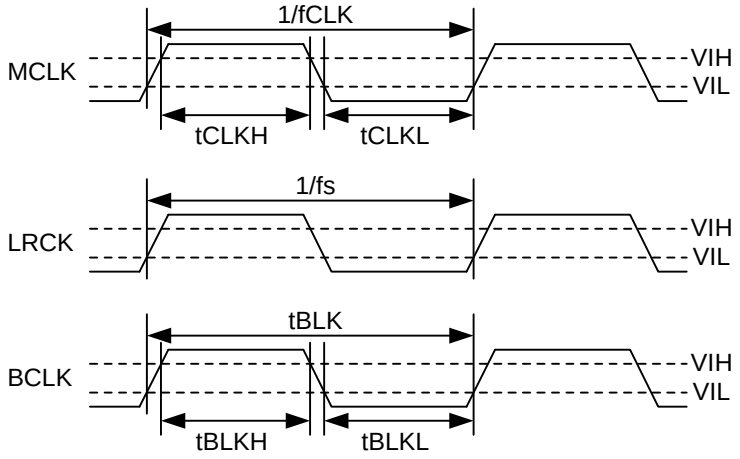


Figure 2. Clock Timing

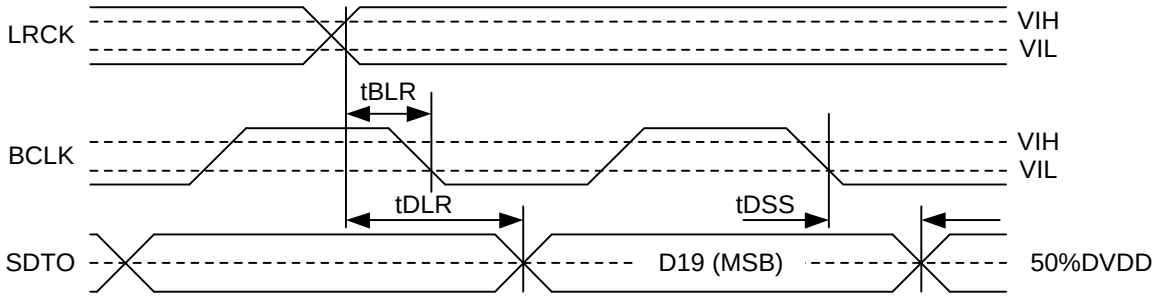


Figure 3. Audio Data Output Timing (Audio I/F = No.0)

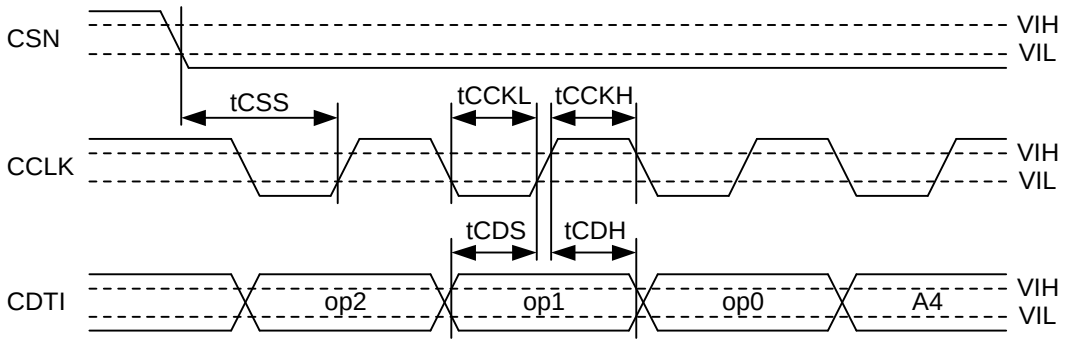


Figure 4. WRITE Command Input Timing

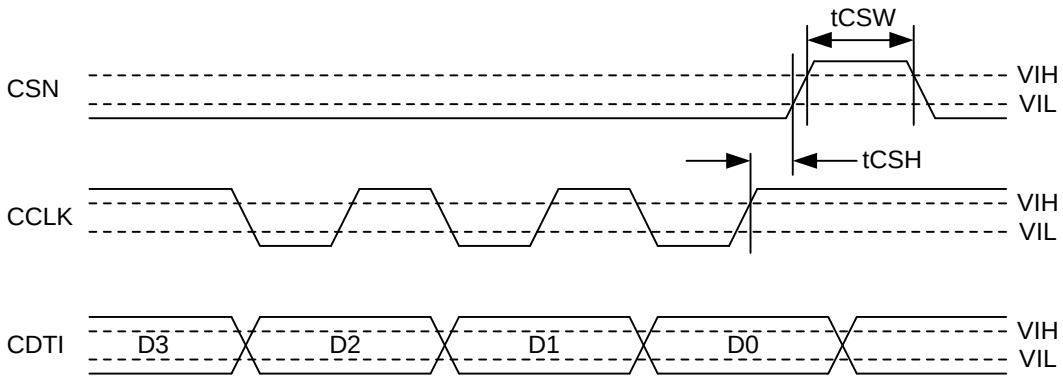


Figure 5. WRITE Data Input Timing

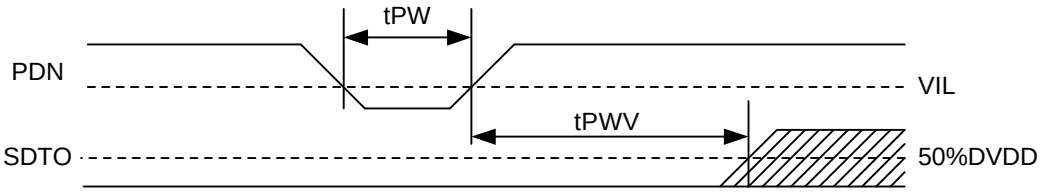


Figure 6. Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The clocks required to operate are MCLK (256fs/384fs), LRCK (fs) and BCLK (32fs, 40fs~). The master clock (MCLK) should be synchronized with LRCK. The phase between these clocks does not matter. The Frequency of MCLK can be input at 256fs or 384fs. When the 384fs is input, the internal master clock is divided into 2/3 automatically. *fs is sampling frequency.

All external clocks (MCLK, BCLK and LRCK) should always be present whenever the ADC is in operation. If these clocks are not provided, the AK5356 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK5356 should be placed in power-down mode.

■ Audio Data I/F Format

The SDTO, BCLK and LRCK pins are connected to an external controller. The audio data format has two modes, MSB-first and 2's compliment. The data format is set using the DIF bit. SDTO is latched by a falling edge of BCLK.

No.	DIF bit	SDTO (ADC)	LRCK	BCLK	
0	0	16bit MSB justified	Lch: "H", Rch: "L"	= 32fs	Default
		20bit MSB justified	Lch: "H", Rch: "L"	≥ 40fs	
1	1	16bit I^2S compatible	Lch: "L", Rch: "H"	= 32fs	
		20bit I^2S compatible	Lch: "L", Rch: "H"	≥ 40fs	

Table 1. Audio Data Format

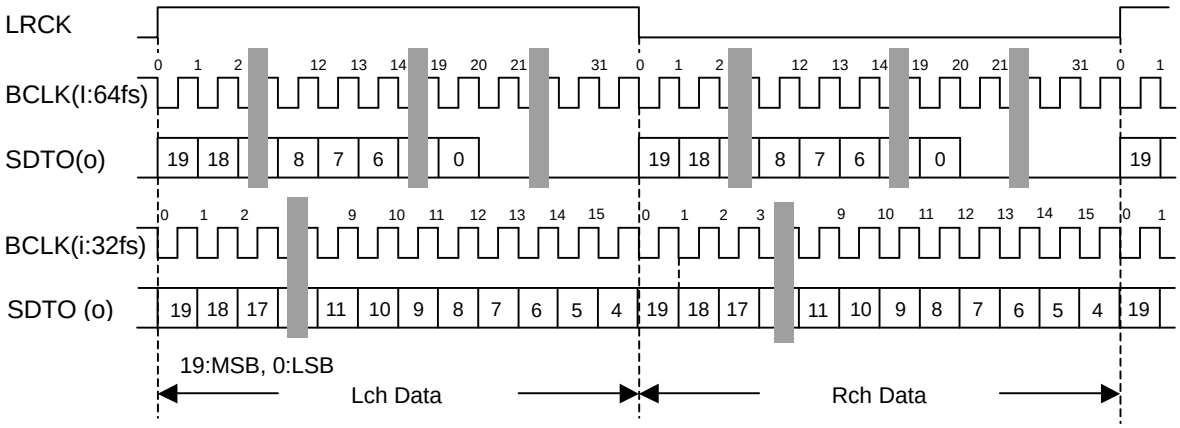


Figure 7. Audio Data Timing (No.0)

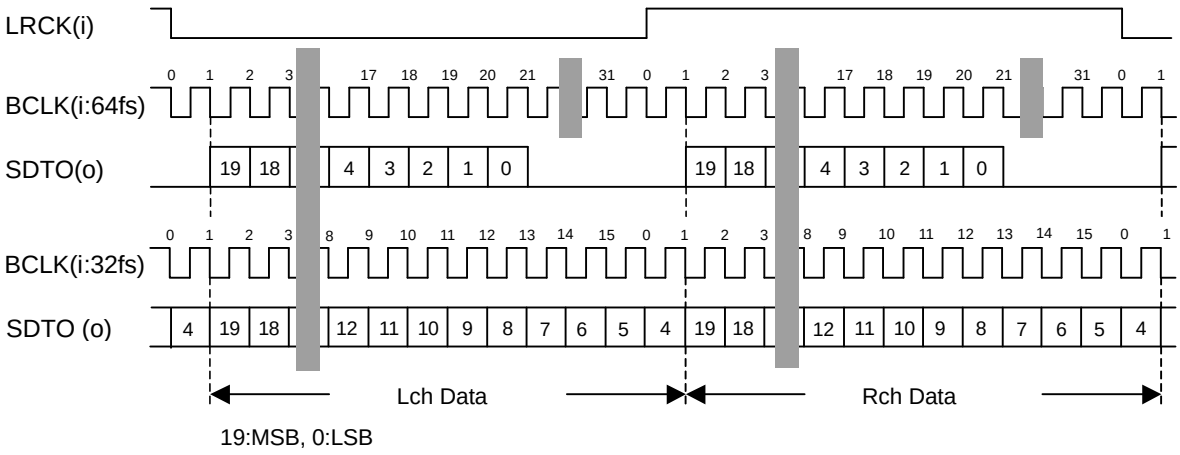


Figure 8. Audio Data Timing (No.1)

■ Digital High Pass Filter

The AK5356 has a Digital High Pass Filter (HPF) to cancel DC-offset in both the IPGA and ADC. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz. This cut-off frequency scales with the sampling frequency (fs). And the HPF can select ON/OFF by HPF bit.

■ MIC Block

1. Pre-Amp

The Pre-Amp is non-inverting amplifier and internally biased to MVCM voltage with 100kΩ (typ.). Gain of the Pre-Amp can select +13dB, +18dB, +28dB or +33dB by PREG1-0 bits.

Pre-Amp gain value of L/R channels change by zero crossing detection or timeout independently. Timeout cycle is fixed to 2048/fs (=46.8ms @ fs = 44.1kHz). Zero crossing detection is done by IPGA block. When PMADC bit is “0”, gain of Pre-Amp changes immediately.

An external capacitor is needed to cancel DC gain. The cut-off frequency is determined by an internal resistor (Ri) and an external capacitor (C1).

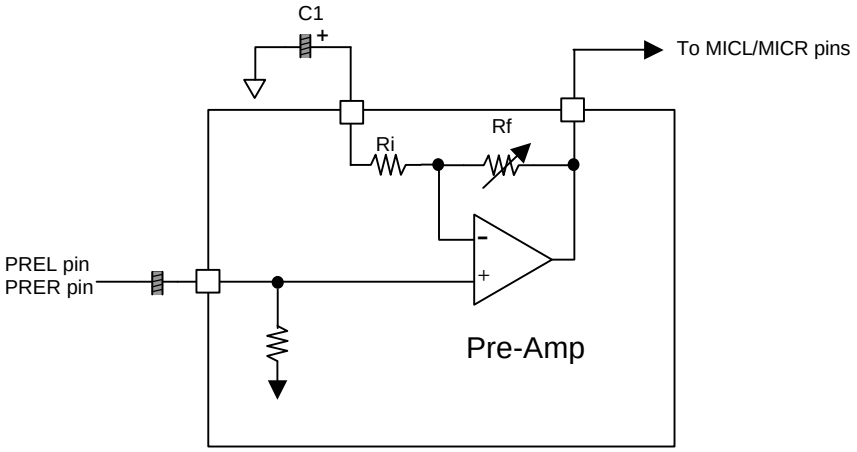


Figure 9. Pre-Amp

2. Power Supply for MIC

The power supply for microphone device is supplied from MPWR pin. The output voltage is typically 2.16V(= 0.8 x MVDD at MVDD=2.7V). MPWR pin can supply the current up to 1mA. When PMMIC bit is “0”, the output current is not supplied.

■ System Reset

The AK5356 is placed in the power-down mode by bringing PDN pin "L". The control registers are also reset at the same time. This reset should always be done after power-up. An analog initialization cycle starts after exiting the power-down mode. The output data SDTO becomes available after 4128 cycles of LRCK clocks. During initialization, the ADC digital data outputs of both channels are forced to a 2's complement "0". The ADC outputs settle to the data corresponding to the input signal at the end of initialization (Settling time equals the group delay time approximately.).

As a normal initialization cycle may not be executed, nothing writes at address 01H during initialization cycle after exiting power-down by PDN pin.

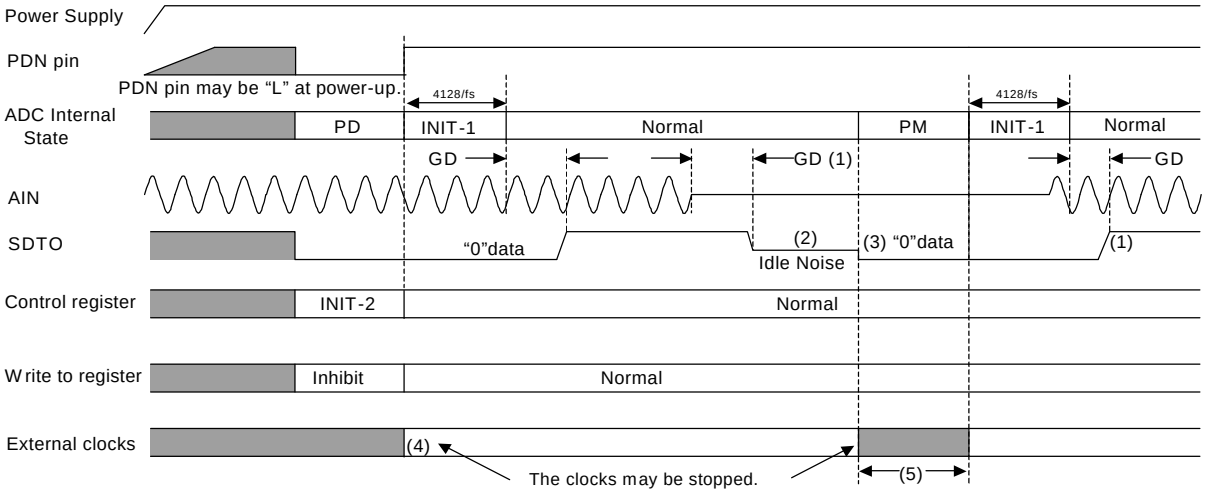


Figure 10. Power-Up / Power-Down Timing Example

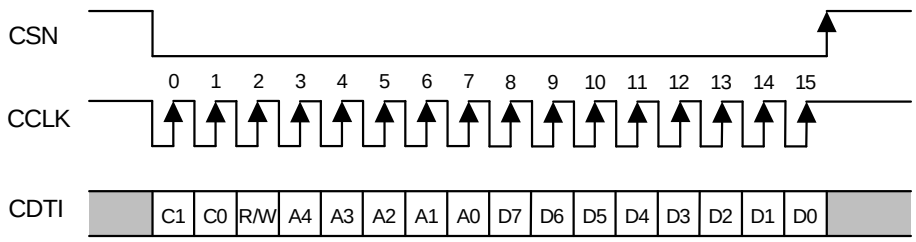
- PD: Power-down state. ADC is output "0".
- PM: Power-down state by Power Management bit. ADC is output "0".
- INIT-1: Initialization cycle of ADC
- INIT-2: Initializing all control registers.
- Inhibit: Inhibits writing to all control registers.

Note: See "Register Definitions" about the condition of each register.

(1). Digital output corresponding to the analog input is delayed by the Group Delay amount (GD). Output signal gradually comes to settle to input signal during a group delay.
(2). If the analog signal does not be input, digital outputs have the offset to op-amp of input and some offset error of a internal.
(3). ADC output data is "0" at power-down.
(4). When the external clocks (MCLK, BCLK and LRCK) are stopped, the AK5356 should be placed in the power-down state.
(5). When external clocks are not supplied, inhibits writing to all control registes.

■ Timing of Control Register

The internal registers are written by the 3-wire μP interface pins: CSN, CCLK, CDTI. These data are included by Chip Address (2bit, The AK5356 is fixed to "10".), Read/Write (1bit), Address (MSB-first, 5bit) and Control data (MSB-first, 8bit). A side of transmitted data is output to each bit by "↓" of CCLK, a side of receiving data is input by "↑" of CCLK. Writing of data becomes effective by "↑" of CSN. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized at PDN pin = "L".



C1-C0: Chip Address (Fixed to "10")
R/W: Read/Write (Fixed to "1"; Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 11. Control Data Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Select	0	PREG1	PREG0	HPF	RIN	MICR	LIN	MICL
01H	Power Management Control	0	0	0	0	0	0	PMADC	PMMIC
02H	Mode Control	MONO1	MONO0	ZTM1	ZTM0	0	0	DIF	0
03H	IPGA Control	ZEIP	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0

All registers are reset at PDN = "L", then inhibits writing to all registers.

For address from 04H to 1FH, data must not be written.
Unused bits must contain a "0" value.

■ Register Definition

Input Select

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Input Select	0	PREG1	PREG0	HPF	RIN	MICR	LIN	MICL
Default		0	1	0	0	0	1	0	1

PREG1-0: Select gain of Pre-Amp
00: +13dB
01: +18dB
10: +28dB (Default)
11: +33dB

Pre-Amp gain value of L/R channels change by zero crossing detection or timeout independently. Timeout cycle is fixed to 2048/fs (=46.8ms @ fs = 44.1kHz). Zero crossing detection is done by IPGA block. When PMADC bit is "0", gain of Pre-Amp changes immediately.

HPF: Select ON/OFF of the digital HPF (0: ON, 1: OFF)

RIN: Select ON/OFF of Rch LINE input (0: OFF, 1: ON)
MICR: Select ON/OFF of Rch MIC input (0: OFF, 1: ON)
LIN: Select ON/OFF of Lch LINE input (0: OFF, 1: ON)
MICL: Select ON/OFF of Lch MIC input (0: OFF, 1: ON)

Power Management Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management Control	0	0	0	0	0	0	PMADC	PMMIC
Default		0	0	0	0	0	0	1	1

PMADC: Power Management of IPGA and ADC
0: Power OFF
1: Power ON (Default)

PMMIC: Power Management of MIC Block (Pre-Amp, MIC Power and MVCM)
0: Power OFF
1: Power ON (Default)

When PDN pin goes "L", all circuit in the AK5356 can be powered-down in no relation to PMADC and PMMIC bits. When PMADC and PMMIC bits go "0", all circuit in the AK5356 can be also powered-down. However, the contents of control registers are held.

Except the case of PMADC=PMMIC= "0" or PDN pin = "L", MCLK, BCLK and LRCK should not be stopped.

Mode Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Mode Control	MONO1	MONO0	ZTM1	ZTM0	0	0	DIF	0
Default		0	0	1	1	0	0	0	0

MONO1-0: Monaural Mixing
00: Stereo (Default)
01: (L+R)/2
10: LL
11: RR

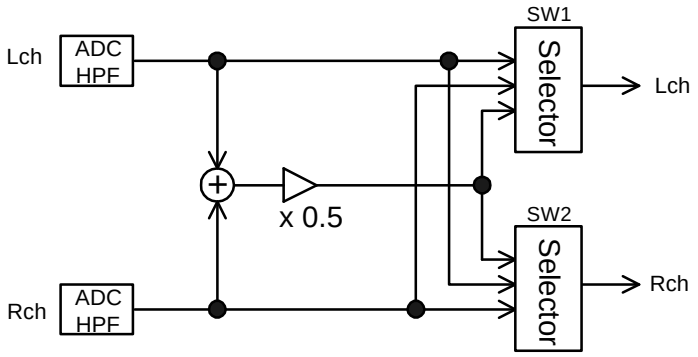


Figure 12. Monaural mixing block

Mode	SW1	SW2	MONO1	MONO0
Stereo Recording	Lch	Rch	0	0
Monaural Recording Stereo Input	(L+R)/2	(L+R)/2	0	1
Monaural Recording Lch Input	Lch	Lch	1	0
Monaural Recording Rch Input	Rch	Rch	1	1

Table 2. Monaural Mode Setting

ZTM1-0: Setting of Zero Crossing Timeout for IPGA
00: 256/fs
01: 512/fs
10: 1024/fs
11: 2048/fs (Default)

DIF: Select Digital Interface Format

No.	DIF bit	SDTO (ADC)	LRCK	BCLK	
0	0	16bit MSB justified	Lch: “H”, Rch: “L”	= 32fs	Default
		20bit MSB justified	Lch: “H”, Rch: “L”	≥ 40fs	
1	1	16bit I^2S Compatible	Lch: “L”, Rch: “H”	= 32fs	
		20bit I^2S Compatible	Lch: “L”, Rch: “H”	≥ 40fs	

Table 3. Audio Data Format

Input Analog PGA Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Input Analog PGA Control	ZEIP	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
Default		0	28H						

ZEIP: Select IPGA zero crossing operation
0: Disable (Default)
1: Enable
Writing to IPGA value at ZEIP = "1", IPGA value of L/R channels changes by zero crossing detection or timeout independently.
In the timeout cycle, it is possible to set in ZTM1-0 bit. When ZTM1-0 is "11", timeout cycle is 2048/fs = 46.4ms (@fs=44.kHz). When ZEIP is "0", IPGA changes immediately.

IPGA6-0: Input Analog PGA, 97 levels; 00H=MUTE
ON/OFF of zero crossing detection can be controlled by ZEIP bit.

DATA	GAIN(dB)	Step	Level
60H	+28.0	0.5dB	73
5FH	+27.5		
5EH	+27.0		
•	•		
28H	+0.0		
27H	-0.5		
•	•		
19H	-7.5		
18H	-8.0		
17H	-9.0	1dB	8
16H	-10.0		
•	•		
11H	-15.0		
10H	-16.0		
0FH	-18.0	2dB	12
0EH	-20.0		
•	•		
05H	-38.0		
04H	-40.0		
03H	-44.0	4dB	3
02H	-48.0		
01H	-52.0		
00H	MUTE		1

Table 4. Input Gain Setting

[Writing to IPGA register at ZEIP = "1" continuously]

When writing control register continuously, the change of IPGA should be written after zero crossing timeout. If IPGA is changed by writing to control register before zero crossing detection, IPGA value of L/R channels may not give a difference level.

SYSTEM DESIGN

Figure 13 shows the system connection diagram. An evaluation board [AK5356] is available which demonstrates the application circuit, optimum layout, power supply arrangement and measurement results.

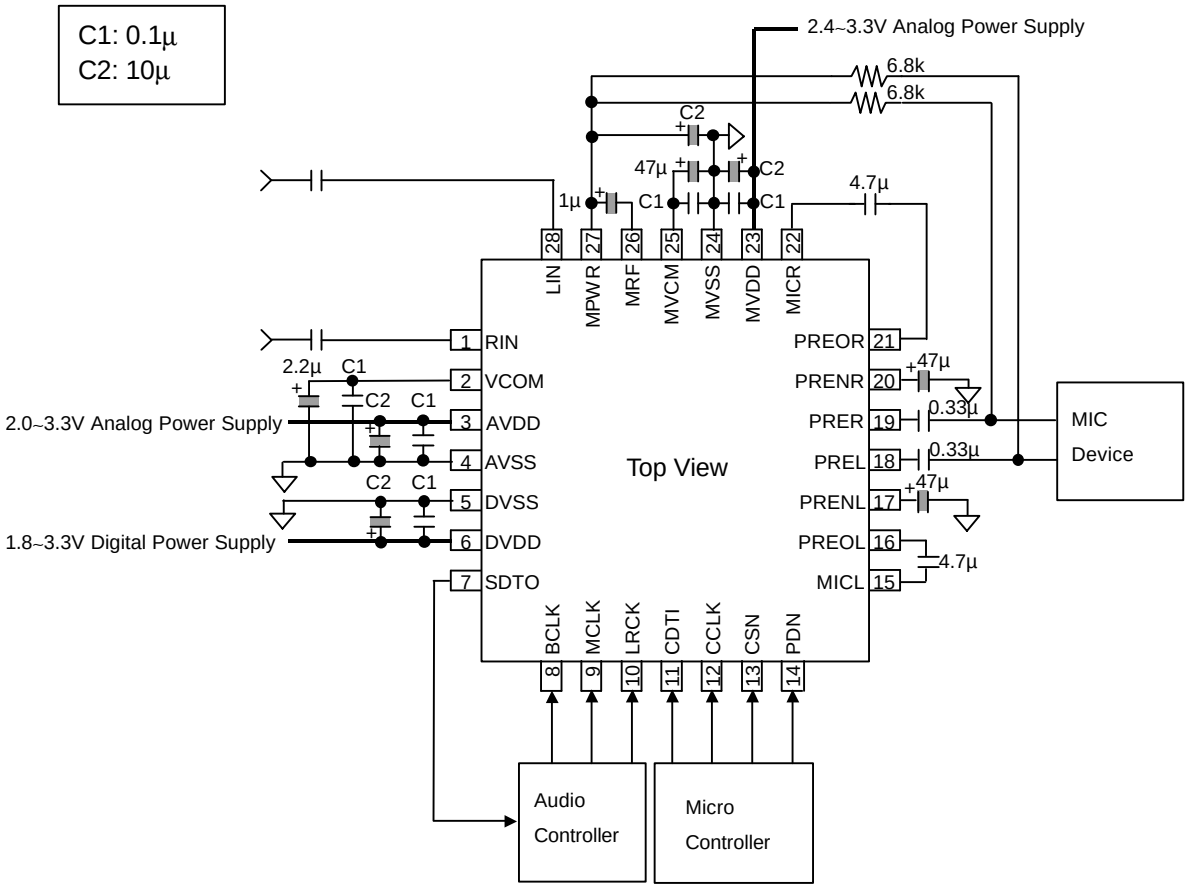
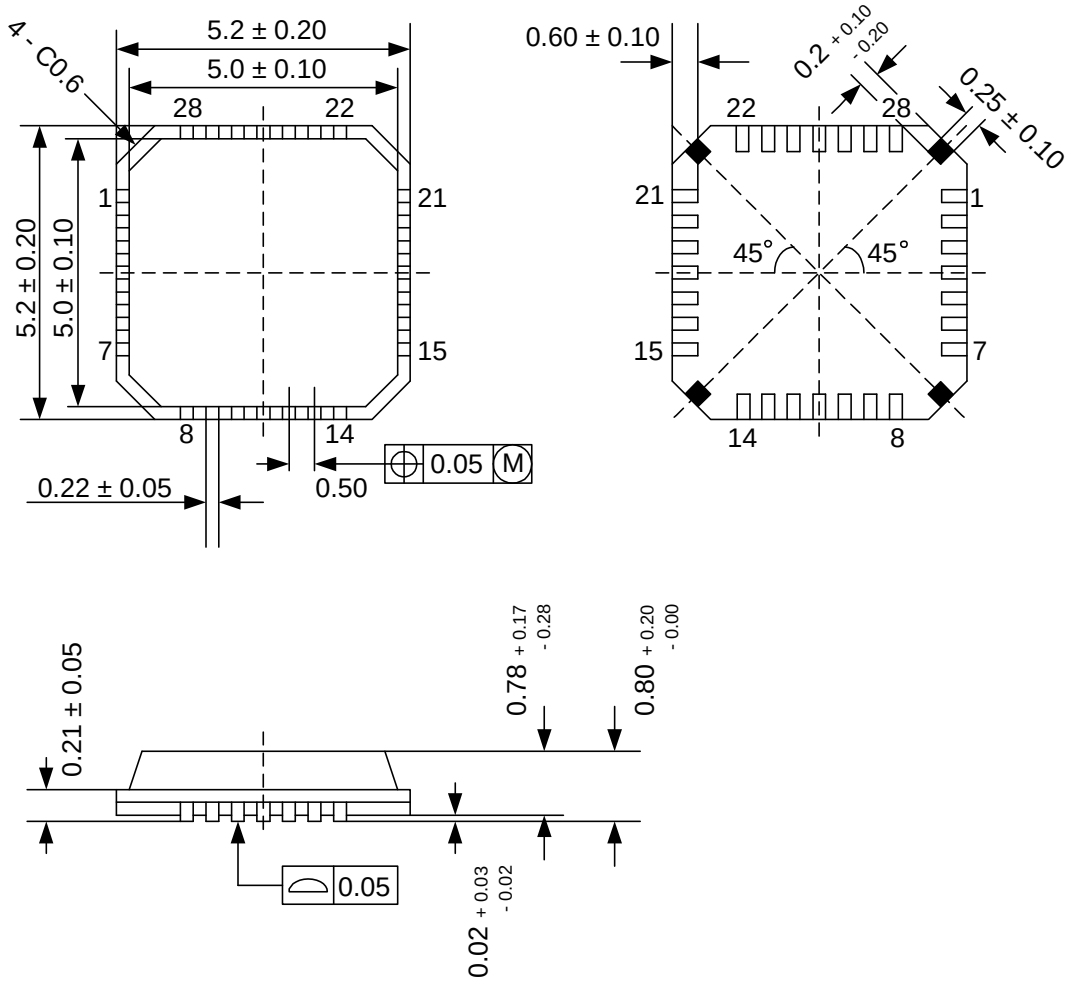


Figure 13. System Connection Diagram Example

NOTE: Electrolytic capacitor value of VCOM depends on low frequency noise of supply voltage.

PACKAGE

● 28pin QFN (Unit: mm)

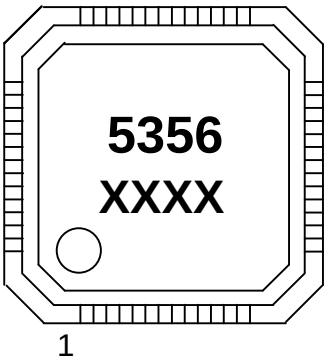


Note) The part of black at four corners on reverse side must not be soldered and must be open.

■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate (Pb free)

MARKING



XXXX : Date code identifier (4 digits)

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