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#### **Contact information:**

Headquarters: ams AG Tobelbaderstrasse 30 8141 Unterpremstaetten, Austria Tel: +43 (0) 3136 500 0 e-Mail: ams\_sales@ams.com

Please visit our website at www.ams.com

# AS3911

# AS3911 general purpose demo Hardware description



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Application engineer: Thomas Luecker Marketing Manager: Mark Dickson

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# 2 Introduction

This application note describes the AS3911 general purpose Demo board and its usage. The general purpose board is made for a flexible use, hence the digital part can be separated from the analogue part. This enables fast software development since the analogue part can be used out of the box.

The analog section has several jumpers to allow a custom antenna and capacitive electrodes to be used.



# 3 Hardware

#### 3.1 Block diagram

The board compromise of a Micro controller with USB support, a LDO to supply the micro controller and the HF reader IC AS3911.





#### 3.2 EMC and Power supply concept

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For rejection of EMC due the rectangular carrier field generation, ferrite beads are placed close to the supply with additional capacitors next to the connector.



Since the specification of USB-supply voltage can have worst case 4.5 Volt, the supply Voltage of the device might vary. AS3911 has an internal regulator that measure the voltage and adjust the internal regulator such that the voltage on the output driver (for antenna) is 0.3Volt below the supply voltage. This adjustment assure that the digital noise on the supply of the antenna driver can be rejected and the Voltage for the antenna driver can be maximized. Hence, for evaluation purpose, we have implemented a jumper P5 which can be used to provide an external voltage supply to the reader IC.

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#### 3.3 Digital section (micro controller)



- The used micro controller is a PIC24 FJGB002 with internal USB.
- Three pins (Pin 1,2 and 3 of the micro controller) are being used for selection of different Hardware versions of boards.
- Four diodes (D5-D8) display the various conditions of the board.
- The connector P2 can be used as a alternative connction to an external micro controller or to connect to a new developed analoge sytem of AS3911. The selection can be done by un mount the coupling resistors (R13-17).

#### 3.3.1 Programming header P1

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P1 is the programming header for the microchip controller. The pin order on the header P1 is exactly the same as being used on the microchip tool chain, hence no special adapter is needed.





#### 3.4 Analog section

Following is the schematic of the analog section incl. AS3911 and its external components





This setup is made to demonstrate almost all the capabilities of AS3911. The salient features are:

- Differential antenna
- Capacitive wakeup (possibility to attach external electrodes)
- Antenna tuning trimming capacitors
- 27MHz Crystal
- supply noise rejection
- High sensitivity
- Low impedance driver stage

#### 3.4.1 Power concept

AS3911 has internal LDO that needs to be decoupled with capacitors of 2.2 microF and 10 nF. These pins are

AGD (analogue ground) VSP\_D (to supply the logic of AS3911) VSP\_A (to supply the analogue part of AS3911) VSP\_RF (to supply the driver stage of AS3911)

AS3911 contains internal level shifter that enables to connect to micro controller with different VDD than AS3911. Pin 1 shall be connected to the same Voltage as the supply of the micro controller.

GND as well as the supply line are being connected with a ferrite bead to reject the EMC disturbance caused by the HF driver.

#### 3.4.2 Antenna stage

The Antenna stage consists of a two stage Filter network and a matching. The two stage filter shall reject higher harmonics of the 13,56 MHz carrier. Since inductors are non-ideal components and the self-resonant frequency of the second coil is around 400 MHz, we propose to use a two staged filter.

The first stage has a corner frequency above 200 MHz and will reduce the harmonics at the higher frequencies.

The second stage has a corner frequency below 10 MHz and will reject frequencies in the lower frequency band.

The matching network follows the filter and adapts the power from the driver to the antenna.

The tuning consists of external capacitors and chip internal switches. In case the switches are open, the antenna Voltage is directly applied to the input pin of the chip.

Since the expected Voltage of the Antenna can be high, additional capacitors for voltage limitation can be applied. The AS3911 can accept voltages up to 30V on its antenna tuning pins.

The input pins are being connected by a capacitive divider. The voltage on that pins shall be less than 3.3 Volt.



#### 3.4.3 Capacitive wakeup

The capacitive wakeup consists of two pins that are each connected to an electrode and are protected against ESD with a gas discharge element.

Since that pins can also be used as test outputs, an additional UFL connector is mounted.

# 4 Measurement

#### 4.1 Current consumption

The measurement is being done across the AS3911 supply jumper P5.

AS3911 working condition	Current consumption in
	mA
After startup	7,58
en=1, rx_en=0, tx_en=0	
en=1, rx_en=1, tx_en=0	14,97
en=1, rx_en=1, tx_en=1	150
en=0, rx_en=0, tx_en=0, wu=1	0.002

#### 4.2 Antenna stage

Used equipment: Network Analyzer HP 8753C Network analyser Parameter test set 85047A Test set

#### 4.3 Measurement of the antenna Parameters

The parameters of the antenna are done in following sequence 1: Start with the measurement of the serial Inductance and the serial resistor at a frequency that is far off the self-resonance of the antenna. The chosen frequency is 1 MHz

@ 1 MHz we get:  $L_{PC} = 940 \text{ nH}$   $R_{DC} = 470 \text{ mOhm}$ 

2. Measurement of the self-resonance (The point in which the impedance will be reel, all reactance's will be zero.

=>  $f_{res} \sim 59 \text{ MHz}$   $R_{P,CAR} = 5000 \text{ Ohm}$ 

Using the inductance value that are being measured at 1 MHz, the resonance capacitor can be calculated with the formula

$$C = \frac{1}{\left(2*\Pi*fres\right)^2*L_{PC}} = \frac{1}{\left(2*\Pi*59MHz\right)^2*940nH} = 7,74\,pF$$

The value of the parallel resistor has to be converted from the self-resonance for the working frequency. The main reason for that conversion is the skin effect of the antenna, thus a correction factor can be given by:

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$$K = \sqrt{\frac{fres}{ftune}} = \sqrt{\frac{59}{13,56}} = 2,085$$

Which will end up in Rp2 at  $fc = K^*R_{DC}$ 

Finally  $R_{PC2} = K \cdot R_{DC} \approx 10.4 \text{ k}\Omega$ 

All components of the antenna are now known and a replacement for the antenna circuit can be drawn.

The serial resistor of the coil can be converted with the approximation formula of the Q-factor

$$Q = \frac{\omega L}{Rs} \approx \frac{Rp}{\omega L} \Longrightarrow Rp = \frac{(\omega L)^2}{Rs} = 14kOhm$$

The complete resistor will thus be a parallel schematic of the resistor due to DC component and the self-resonance component

$$Rpc = \frac{Rp1 * Rp2}{Rp1 + Rp2} \approx 6,02kOhm$$

All components of the antenna are known and a model of the antenna can be given:



The values for the wanted resonance circuit are therefore:

RPC =6,02 kOhm

CPC= 7,74 pF

LPC= 940 nH

#### 4.4 Determination of the Antenna resistor

The Antenna Q Factor can then be calculated as

$$Q = \frac{R_{PC}}{(\omega L)} = \frac{R_P}{(\omega L)} = \frac{6,02kOhm}{2*\Pi*13,56MHz*940nH} = 75$$

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Since the antenna works like a filter around it resonance frequency and the subcarrier is 848kHz apart from the carrier, the bandwidth and thus the Q factor need to be adapted. The Bandwidth is defined based on the sub carrier frequency.

$$Q = \frac{\Delta fres}{fres} = \frac{848kHz}{13,56MHz} \approx 13$$

Since AS3911 can work due its excellent sensitivity in high Q environment, the Q factor can be increased to values above 13 and for that board Q is set to 20.

And the parallel target resistor can then be calculate to

$$R_T = Q * (\omega L)$$

$$R_T = 20*(2*13MHz*940nH) = 1601Ohm$$

Taking the parasitic resistor RPC from the antenna into account, the physical assembled resistor can be calculated to

$$R_P = \frac{R_{PC}R_T}{R_{PC} - R_T} = \frac{6020*1601}{6020-1601} = 2181\Omega$$

The next available physical value is 2200 Ohm.

#### 4.5 Matching of the driver

The matching is done from the driver resistor towards the antenna resistor.

The driver resistor can be assumed with 2 Ohm.

Since the antenna is being used differential, only half of the antenna shall be considered for the matching.

Matching resistor on antenna side: RP=1090 Ohm Antenna coil LP=470nH



Using the program smith.exe from Bern University of applied science, following matching with physical available values is found.

	ae	austria <b>micro</b> systems
	Schematic	
Data Dainte	220.0 nH	ε. ξ
DP-Nr. 1 (2.000 + j0.000)0hm	330.0 pF	
DF-Nr. 2 [2.000 + ]18./44]0hm DP-Nr. 3 [2.709 - j21.772]0hm DP-Nr. 4 [2.709 - j57.339]0hm DP-Nr. 5 [14.176 + i130.539]0hm	470.0 mH 88.9 pF	
DP-Nr. 6 (1.22e+003 + j0.000)Ohm		L

2 Ohms are being matched to 1220 Ohm.



According to the smith chart, the parallel capacitor shall be 89 pF. This capacitor is being composed out of the parasitic capacitance of the antenna, the parasitic capacitance of the tracks / voltage divider of the input and the tuning capacitor.

Capacitor	Value	Note
	pF	
Parasitic antenna capacitor	15,4	Measured value of 7,7 pF
		needs to be multiplied by two
		due to the differential stage
Parasitic of the capacitive	Assumed to be18	Capacitor divider (10 pF)
divider and tuning inputs		plus 2 pF parasitic on each
		tuning inputs (4x2 pF)
Tuning capacitor	56	Half of the maximum tuning
		capacitor bank
Result	88	

#### 4.6 Verification of the Q factor in the time domain

The resonance circuit envelope can be calculated with an exponential function Falling edge:

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$$U_{f} = e^{\frac{-t}{\tau}} = e^{-t\frac{2\pi\Pi f_{c}}{Q}}$$
  
Rising edge:  
$$Ur = 1 - e^{\frac{-t}{\tau}} = 1 - e^{-t\frac{2\pi\Pi f_{c}}{Q}}$$

Thus if the time constant (37% of the maximum amplitude) is known, the Q factor is calculated to:

 $Q_{B} = \tau * 2 * \Pi * f_{c}$ 

# Version Name Name

#### 4.7 Measurement with Standard assembly of 2200 Ohm.

With TF=310 ns With TR=205 ns

QR=26 QF=17

#### 4.8 Layout recommendations

AS3911 is a high integrated device that allow easy layout. There are only a few layout rules to consider.

Use a solid ground plan under the chip and use thermal via under the chip to dissipate the heat of and enable a low ohmic connection of the exposed pad to the ground plane.

Take care that the decoupling capacitors of the LDO are close to the chip. Use thick wires for the decoupling tracks and place the 10nF capacitor closest to the chip.

Use a symmetric layout for the antenna stage

Do not cross the digital lines with the analogue lines.

Take care on the signals VSN\_RF, VSP\_RF and the two output pins RFO1 and RFO2. These pins build up the internal driver stage. Tracks on those four pins shall be short and ground connections must be solid.



#### 4.9 PCB stack

The PCB stack is made of a two layer PCB with 1.6 mm core material and 35micro (43 micro final ) copper.





#### 4.11 Gerber Bottom

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#### 4.12 Assembly Top





#### 4.13 Bill of Material

Part Info	Reference	Footprint	Producer	Distributor	Distributor Number	count
Integrated Circuits (IC)						
AS3911	AS1	QFN32	austriamicrosystems			1
AS1360	U2	SOT23	austriamicrosystems			1
PIC27FJ64GB002	U3	QFN28_6x6	Microchip	Digikey	PIC24FJ64GA002T- I/MLTR-ND	1
SMD resistor						
10k	R1, R2, R4, R5, R7, R18, R20, R100	R0402	Yageo	Digikey	311-10KGRTR-ND	8
0R	R6,R29	R0402	Yageo	Digikey	311-0.0JRTR-ND	2
220R	R8, R9, R10, R11, R12, R13, R14, R15, R16, R17	R0402	Panasonic-ECG	Digikey	P220GTR-ND	10
470R	R19, R23, R24, R25, R26	R0402	Stackpole Electronics	Digikey	RMCF0402JT470RTR-ND	5
27R	R21, R22	R0402	Yageo	Digikey	311-27JRTR-ND	2
330R	R27	R0402	Yageo	Digikey	311-330JRTR-ND	1
2k2	R28	R0402	Yageo	Digikey	311-2.2KJRTR-ND	1
SMD capacitors						
10u	C1,C4,C10	C0805	TDK Corporation	Digikey	445-1371-2-ND	3
1u	C5,C6	C0603	Taiyo Yuden	Digikey	587-2834-2-ND	2
10n	C7, C15, C18, C24, C29, C30	C0402	Yageo	Digikey	311-1042-2-ND	6
100n	C8, C9	C0402	AVX Corporation	Digikey	478-1239-2-ND	2
18p	C11, C12, C13, C16	C0402	TDK Corporation	Digikey	445-1238-2-ND	4
2u2	C14, C17, C21, C32, C33	C0603	TDK Corporation	Digikey	587-2983-2-ND	5
6p8	C20, C34	C0402	TDK Corporation	Digikey	445-4887-2-ND	2
12p	C23, C35	C0402	Yageo	Digikey	311-1016-2-ND	2
100p	C25	C0402	Yageo	Digikey	311-1024-2-ND	1
27p	C27, C36	C0402	Yageo	Digikey	311-1019-2-ND	2
56p	C31, C37	C0402	Yageo	Digikey	311-1022-2-ND	2
47p	C38, C43	C0402	Yageo	Digikey	311-1021-2-ND	2
470p	C44, C47	C0402	Yageo	Digikey	311-1028-2-ND	2
330p	C45, C46	C0402	Yageo	Digikey	311-1027-2-ND	2
120p	C48, C49	C0603	TDK Corporation	Digikey	445-1248-2-ND	2
6p8	C50	C0603	TDK Corporation	Digikey	445-5039-2-ND	1
100p	C51, C54	C0603	TDK Corporation	Digikey	445-1281-2-ND	2
10p	C52, C53	C0603	Kemet	Digikey	399-1049-2-ND	2
SMD inductors						
10n	L4,L5	L0603	TDK Corporation	Digikey	445-1492-2-ND	2
220n	L7,L8	L0805	Murata	Digikey	490-5669-2-ND	2
Ferritbead	L1, L2, L3, L6, L9	L0805	Taiyo Yuden	Digikey	587-1911-2-ND	5
SMD diodes				<u> </u>		
24V	D1, D2, D4	D0603_SUP		Farnell	1470613	3
Zener	D3	SOD323F (SC-90)	Comchip Technology	Digikey	641-1068-2-ND	1

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SMD LED						
LED_LUMEX	D5,D6,D7,D8	Led_0402_L umex	Kingbright Corp	Digikey	754-1104-2-ND	4
Oscillator						
27.12MHz	Q1	Crystal FA- 20H 40.0000MF1 5Z-AC3	Murata	Digikey	490-5581-2-ND	1
Mechanical components						
USB_MINI_B	U1	SOCKET_S MD_USB_M INI	Hirose Electric	Digikey	H2959TR-ND	1
Not Used						
10u	C2,C3	C0603	TDK Corporation	Digikey	445-4112-2-ND	2
8MHz	Y1	Crystal FA- 20H 40.0000MF1 5Z-AC3				1
Header 8H	P1, P2	HDR1X8				2
U FL Socket - Surface Mount	P3, P4					2
Header 2	P5	HDR1X2				1
MHDR1X2	P6, P7	HDR1X2				2
Header 3	P8	HDR1X3		<u> </u>		1
Plug	T1	TESTPOINT				1
Plug	T2, T3, T4, T5	PIN1				4
dnp	C19, C22, C26, C28, C39, C40, C41, C42	C0402				8
dnp	R3	R0402				1
CSA20-141N DNP	U4, U5	6-0805_M				2
L	9					
Tolerance if not othe	er specified		$\mathbf{O}$			
Capacitor NP0/COG	2%					
Capacitor X7R:	10%		1			
Capacitor Y5V:	+80	% -20%				
Tantalum	209/					

	(		
Tolerance if not othe	r specified		
Capacitor NP0/COG		2%	
Capacitor X7R:		10%	
Capacitor Y5V:		+80% -20%	
Tantalum		20%	
Resistor		5%	
Inductivity		5%	

#### 5 Version History

Version Originator Change log	
1.00 tlu Initial Version	



For further information please contact

The Wireless Business Line Schloss Premstaetten A-8141 Unterpremstaetten AUSTRIA Tel: +43-(0)3136-500-5473 FAX: +43-(0)3136-500-4141 wireless@austriamicrosystems.com

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