

# DIFFERENTIAL-TO-LVDS BUFFER/DIVIDER W/INTERNAL TERMINATION

**ICS889872**

## General Description



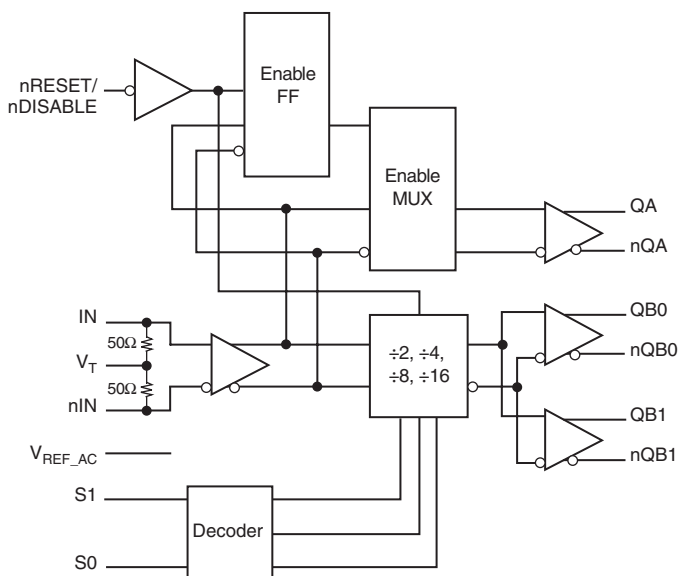
The ICS889872 is a high speed Differential-to-LVDS Buffer/Divider w/Internal Termination and is a member of the HiPerClockSTM family of high performance clock solutions from IDT. The ICS889872 has a selectable  $\div 2$ ,  $\div 4$ ,  $\div 8$ ,  $\div 16$  output

dividers. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

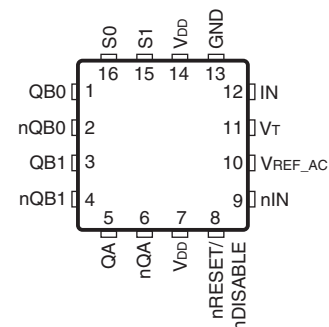
## Features

- Three LVDS outputs
- Frequency divide select options:  $\div 4$ ,  $\div 6$ : >2GHz,  $\div 8$ ,  $\div 16$ : >1.6GHz
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: >2GHz
- Cycle-to-cycle jitter: 1ps (typical)
- Total jitter: 10ps (typical)
- Output skew: 7ps (typical), QA/nQA outputs
- Part-to-part skew: 250ps (typical)
- Propagation Delay: 750ps (typical), QA/nQA outputs
- Full 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Block Diagram



## Pin Assignment



**ICS889872**  
**16-Lead VFQFN**  
**3mm x 3mm x 0.95mm package body**  
**K Package**  
**Top View**

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	QB0, nQB0	Output		Differential output pair. Divide by 2, 4, 8, 16. Unused outputs must be terminated with 100W across the pin (QB0/nQB0). LVDS interface levels.
3, 4	QB1, nQB1	Output		Differential output pair. Divide by 2, 4, 8, 16. Unused outputs must be terminated with 100W across the pin (QB1/nQB1). LVDS interface levels.
5, 6	QA, nQA	Output		Differential undivided output pair. LVDS interface levels.
7, 14	V <sub>DD</sub>	Power		Power supply pins.
8	nRESET/ nDISABLE	Input	Pullup	Output reset and enable/disable pin. When LOW, resets the divider select, and align Bank A and Bank B edges. In addition, when LOW, Bank A and Bank B will be disabled. Input threshold is V <sub>DD</sub> /2V. Includes a 37kΩ pullup resistor. LVTTTL / LVCMOS interface levels.
9	nIN	Input		Inverting differential LVPECL clock input. RT = 50Ω termination to V <sub>T</sub> .
10	V <sub>REF_AC</sub>	Output		Reference voltage for AC-coupled applications. Equal to V <sub>DD</sub> – 1.4V (approx.). Maximum sink/source current is 0.5mA.
11	V <sub>T</sub>	Input		Termination input. Leave pin floating.
12	IN	Input		Non-inverting LVPECL differential clock input. RT = 50Ω termination to V <sub>T</sub> .
13	GND	Power		Power supply ground.
15, 16	S1, S0	Input	Pullup	Select pins. Logic HIGH if left unconnected (÷16 mode). S0 = LSB. Input threshold is V <sub>DD</sub> /2. 37kΩ pullup resistor. LVCMOS/LVTTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R <sub>PULLUP</sub>	Input Pullup Resistor			37		kΩ

## Function Tables

Table 3A. Control Input Function Table

Input	Outputs	
nRESET	QA, QBx	nQA, nQBx
0	Disabled; LOW	Disabled; HIGH
1	Enabled	Enabled

NOTE: After nRESET switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1*.

Figure 1. nRESET Timing Diagram

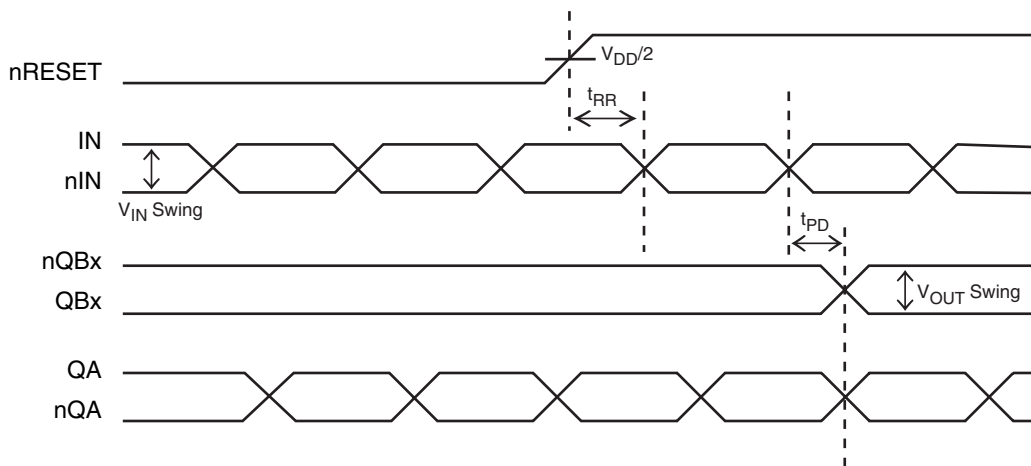


Table 3B. Truth Table

Inputs			Outputs	
nRESET/nDISABLE	S1	S0	Bank A	Bank B
1	0	0	Input Clock	Input Clock $\div 2$
1	0	1	Input Clock	Input Clock $\div 4$
1	1	0	Input Clock	Input Clock $\div 8$
1	1	1	Input Clock	Input Clock $\div 16$
0	X	X	QA = LOW, nQA = HIGH; NOTE 1	QBx = LOW, nQBx = HIGH; NOTE 2

NOTE 1: On the next negative transition of the input signal.

NOTE 2: Asynchronous reset/disable function. Absolute Maximum Ratings

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	10mA 15mA
Input Current, $I_N$ , $nIN$	$\pm 50mA$
$V_T$ Current, $I_{VT}$	$\pm 100mA$
Input Sink/Source, $I_{REF\_AC}$	$\pm 0.5mA$
Operating Temperature Range, $T_A$	-40°C to +85°C
Package Thermal Impedance, $\theta_{JA}$ , (Junction-to-Ambient)	51.5°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current			80		mA

Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		0		0.8	V
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	$V_{DD} = 2.625V, V_{IN} = 0V$	-150			$\mu A$

**Table 4C. Differential DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{IN}$	Differential Input Resistance (IN, nIN)			100		$\Omega$
$V_{IH}$	Input High Voltage (IN, nIN)		1.2		$V_{DD}$	V
$V_{IL}$	Input Low Voltage (IN, nIN)		0		$V_{DD} - 0.15$	V
$V_{IN}$	Input Voltage Swing		0.15		2.8	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing		0.3			V
$I_{IN}$	Input Current (IN, nIN)				45	mA
$V_{REF\_AC}$	Bias Voltage			$V_{DD} - 1.35$		V

**Table 4D. LVDS DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OUT}$	Output Voltage Swing			350		mV
$V_{OH}$	Output High Voltage			1.475		V
$V_{OL}$	Output Low Voltage		0.925			V
$V_{CCM}$	Output Common Mode Voltage			1.35		V
$\Delta V_{OCM}$	Change in Common Mode Voltage				50	mV

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	$\div 2, \div 4$		>2		GHz
	Input Frequency	$\div 8, \div 16$		>1.6		GHz
$t_{PD}$	Propagation Delay; NOTE 1, 2	IN-to-Q	Input Swing: <400mV	750		ps
			Input Swing: $\geq 400mV$	750		ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3, 4	QB0-to-QB1		7		ps
		QA-to-QB		60		ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 4, 5			250		ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 2, 6			1		ps
$f_{jit(j)}$	Total Jitter; NOTE 2			10		ps
$t_{RR}$	Reset Recovery Time; NOTE 2		600			ps
$t_R / t_F$	Output Rise/Fall Time; NOTE 2			150		ps

All parameters characterized at  $\leq 1GHz$  unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Specs are design targets.

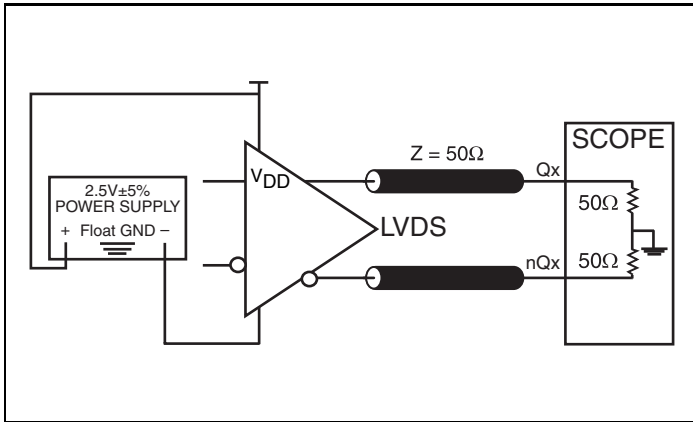
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

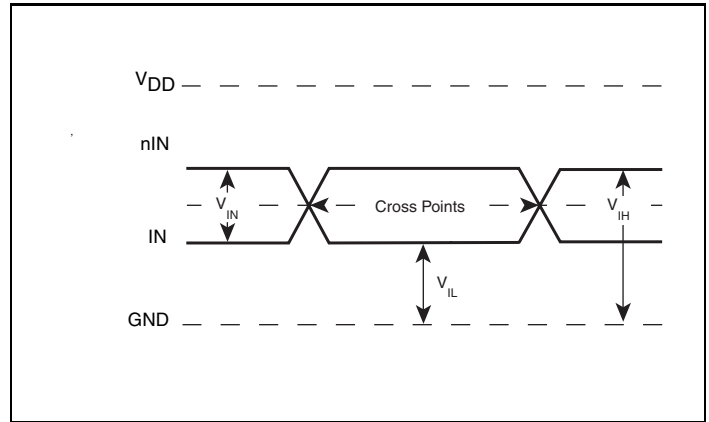
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 6: The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

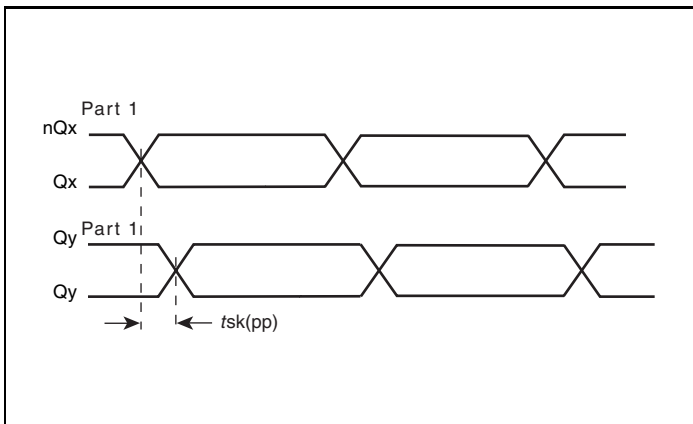
### Parameter Measurement Information



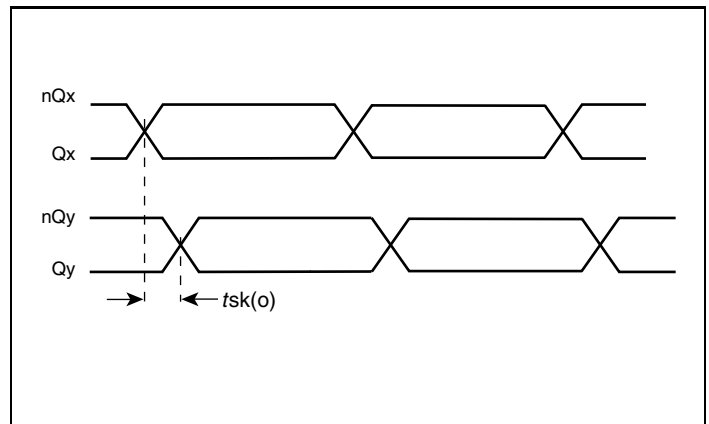
LVDS Output Load AC Test Circuit



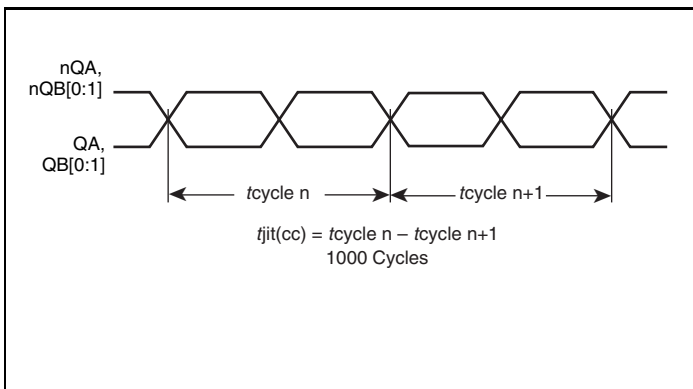
Differential Input Level



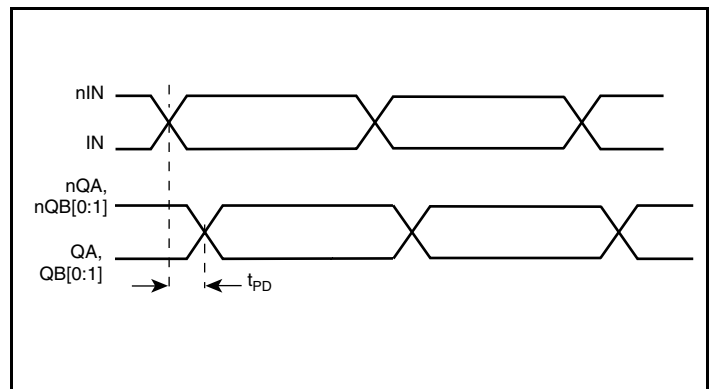
Part-to-Part Skew



Output Skew

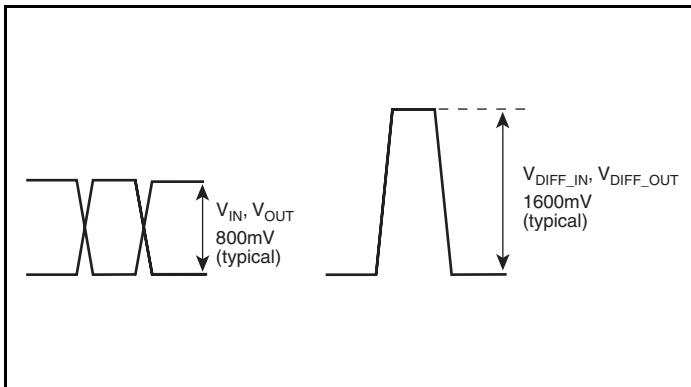


Cycle-to-Cycle Jitter

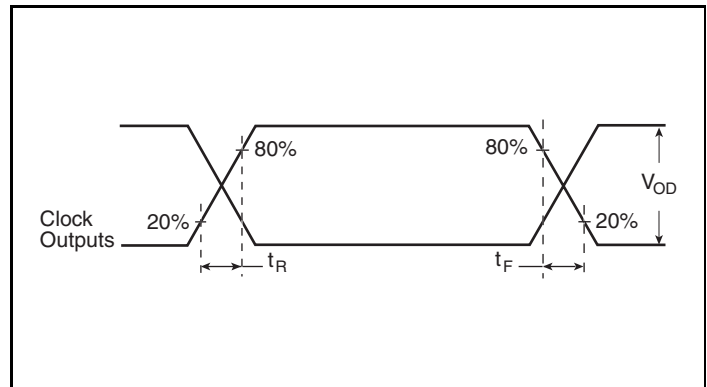


Propagation Delay

## Parameter Measurement Information, continued



Single-Ended & Differential Input Voltage Swing



Output Rise/Fall Time

## Application Information

### Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

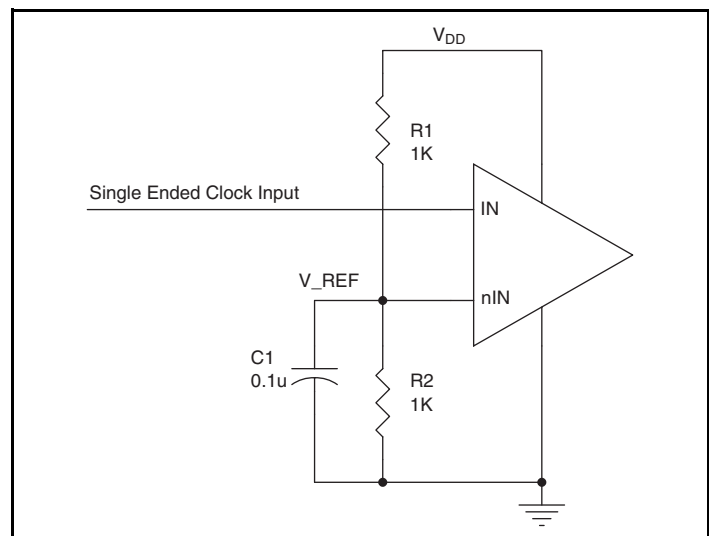
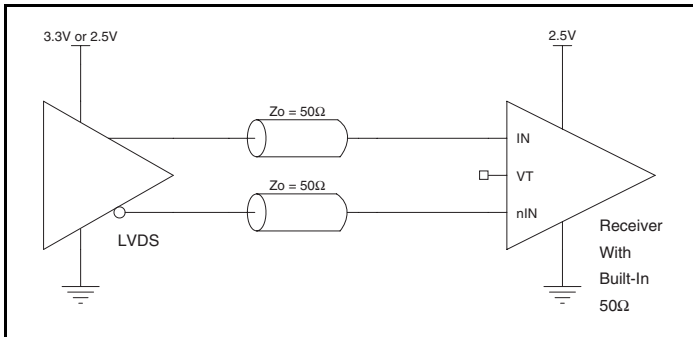


Figure 2. Single-Ended Signal Driving Differential Input

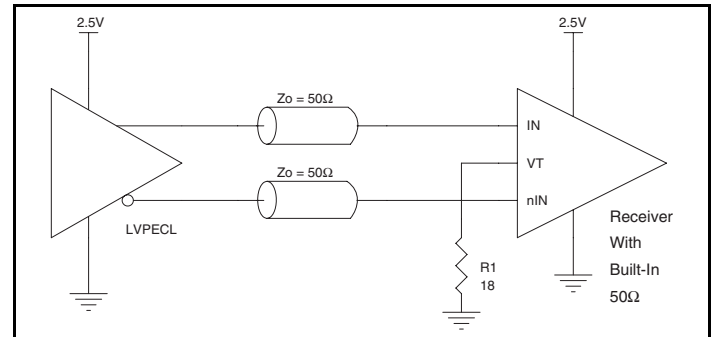
## Differential Input with Built-in 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types.

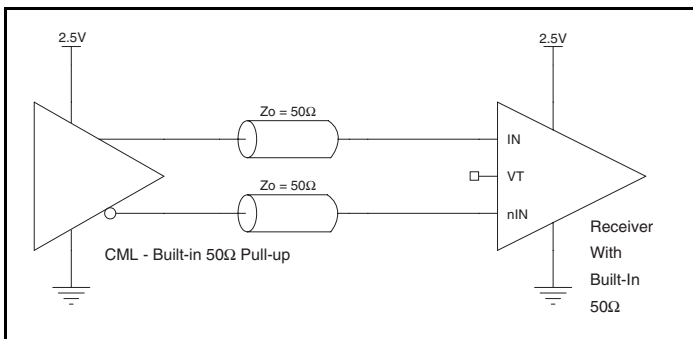
The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



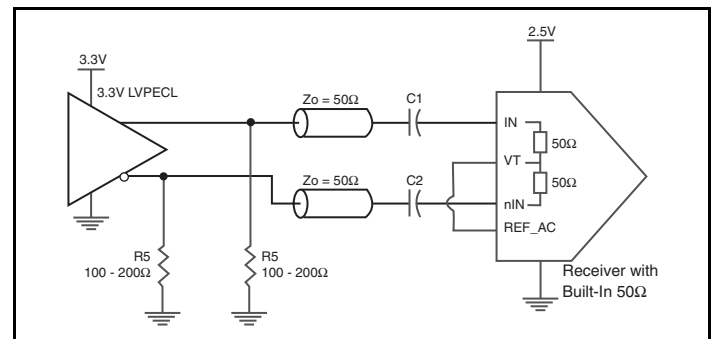
**Figure 3A. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver**



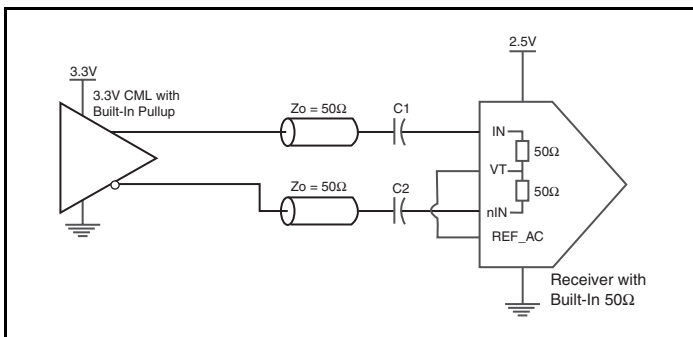
**Figure 3B. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver**



**Figure 3C. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup**



**Figure 3D. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver**



**Figure 3E. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by a 3.3V CML Driver with Built-In Pullup**



## Recommendations for Unused Input Pins

### Inputs:

#### LVC MOS Select Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

### Outputs:

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, we recommend that there is no trace attached.

## EPAD Thermal Release Path

The EPAD provides heat transfer from the device to the P.C. board. The exposed metal pad on the PCB is connected to the ground plane through thermal vias. To guarantee the device's electrical and thermal performance, EPAD must be soldered to the exposed

metal pad on the PCB, as shown in Figure 4. For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

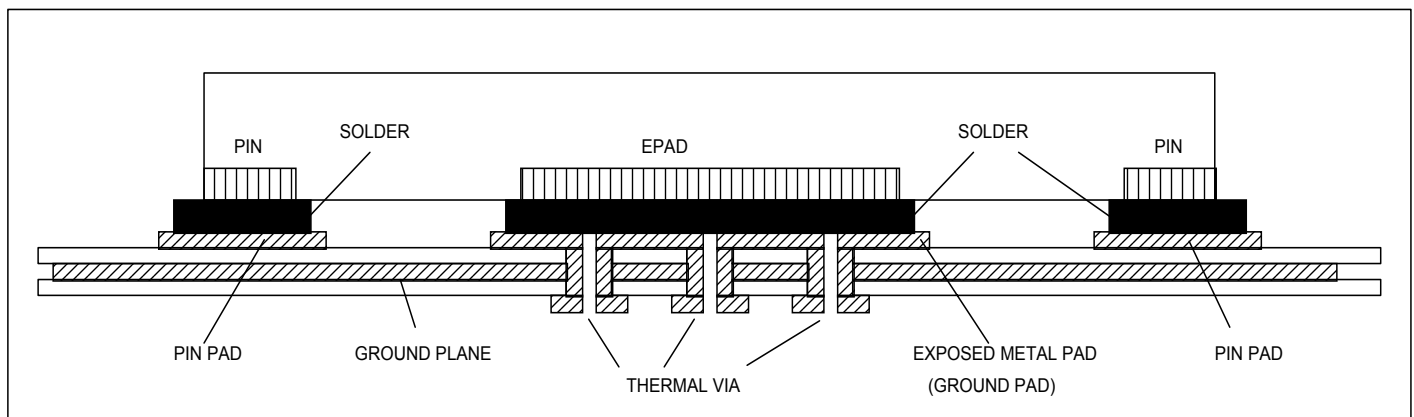


Figure 4. P.C. Board for Exposed Pad Thermal Release Path Example

## 2.5V LVDS Driver Termination

Figure 5 shows a typical termination for LVDS driver in characteristic impedance of  $100\Omega$  differential ( $50\Omega$  single)

transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

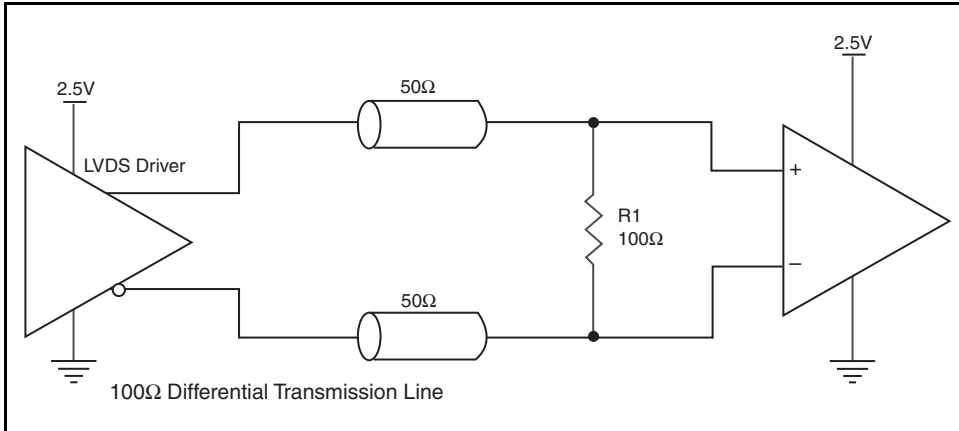


Figure 5. Typical LVDS Driver Termination

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS889872. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS889872 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 2.5V + 5\% = 2.625V$ , which gives worst case results.

- $Power_{MAX} = V_{DD\_MAX} * I_{DD\_MAX} = 2.625V * 80mA = 210mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.210W * 51.5^\circ C/W = 95.8^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 16 Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity			
Linear Feet per Minute	0		
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W		

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead VFQFN

$\theta_{JA}$ by Velocity		
Linear Feet per Minute	0	
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W	

## Transistor Count

The transistor count for ICS889872 is: 323

Pin compatible with SY89872U

## Package Outline and Package Dimensions

### Package Outline - K Suffix for 16 Lead VFQFN

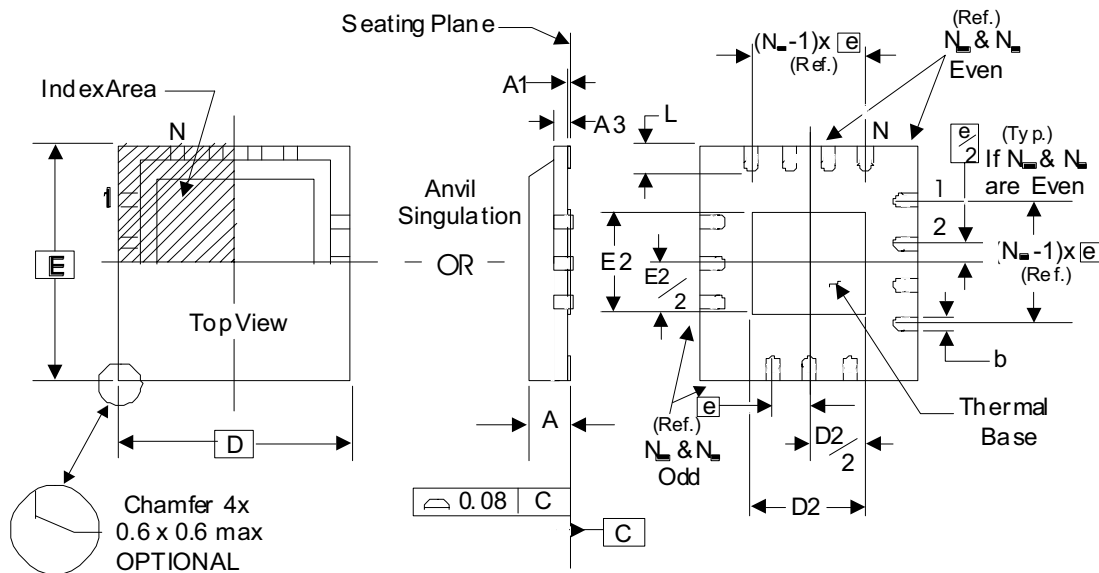


Table 8. Package Dimensions

JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	16	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
$N_D$ & $N_E$	4	
D & E	3.00 Basic	
D2 & E2	1.00	1.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS889872AK	872A	16 Lead VFQFN	Tube	-40°C to 85°C
ICS889872AKT	872A	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
ICS889872AKLF	TBD	"Lead-Free" 16 Lead VFQFN	Tube	-40°C to 85°C
ICS889872AKLFT	TBD	"Lead-Free" 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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