General Description

The ADT7310 is system specific power supply IC that is suitable for color CCD camera.
Other features include over-current protection, thermal shutdown. It reduces design complexity and external component count.

Package outline of the ADT7310

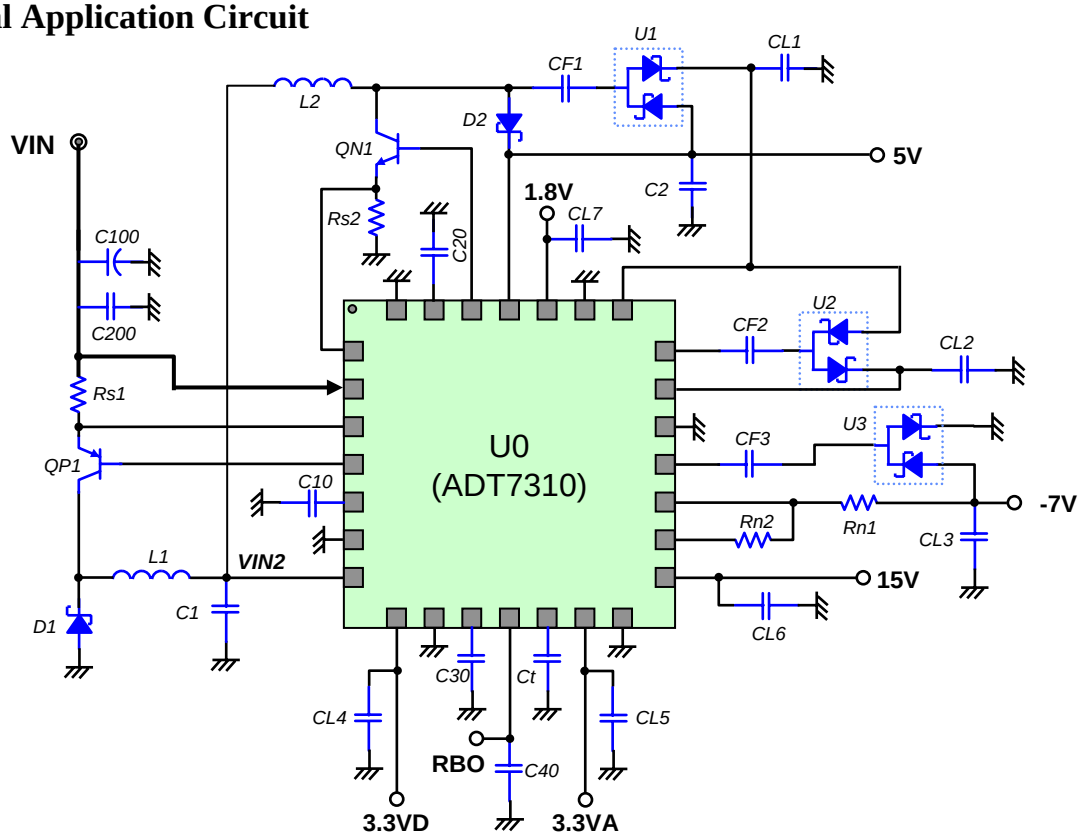
Features

- Input voltage range : 4.75V to 18V
- Multiple output voltage channel available
  - 2 channel 3.3V outputs , 200mA / 60mA max.
  - 1.8V output , 40mA max.
  - 5V boost converter output , 100mA max.
  - 15V output , 10mA max.
  - Externally adjustable negative voltage output (-7V typical)
- Power-on-reset output & power sequence
- Protection : thermal shutdown , over-current protection
- Small size(5x5 mm^2 body) and thermally enhanced 28 Pin MLF Package

Applications

- Color CCD camera
- CCTV camera
- distributed power system
  (3.3V / 1.8V / 5V / 15V / -7V)

Typical Application Circuit



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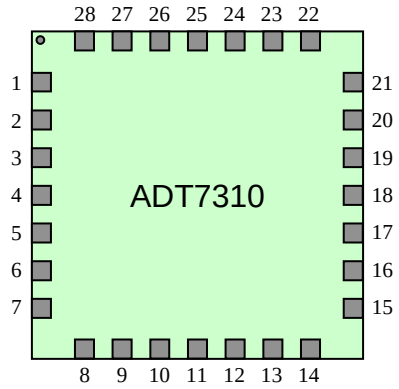
Part List

Component	Type	Value (Model)	Manufacturer
U0	IC	ADT7310	ADTech
U1, 2, 3	IC	BAT54SWT1	ON Semiconductor
QP1	Chip transistor	2SB1424	ROHM
QN1	Chip transistor	MMBT4401LT1	ON Semiconductor
D1, D2	Chip SBD	RSX101M-30	ROHM
L1	Chip inductor	47uH / 590mA (SLF6028T-470MR59)	TDK
L2	Chip inductor	47uH / 590mA (SLF6028T-470MR59)	TDK
C1 , 2	MLCC	10uF / 10V / X5R	Murata
C100	Tantalum capacitor	10uF / 25V (T91C106K025AT)	KEMET
C200	MLCC	0.1uF / 25V	-
CF1 , 2 , 3	MLCC	1uF / 25V / X5R	Murata
CL1 , 2 , 3	MLCC	2.2uF / 25V / X5R	Murata
C10	MLCC	1nF	-
C20	MLCC	22nF	-
C30	MLCC	22nF	-
Ct	MLCC	18pF	-
CL4, 5, 7	MLCC	2.2uF / 25V / X5R	Murata
CL6	MLCC	4.7uF / 25V / X5R	Murata
C40	MLCC	10nF	-
Rs1 , 2	Chip resistor	0.1Ω / 1%	-
Rn1	Chip resistor	45.3kΩ / 1%	-
Rn2	Chip resistor	12.1kΩ / 1%	-

※ SBD (Schottky Barrier Diode)

Pin Configuration



Pin Description

I : Input , O : Output , IO : Input/Output , P : Power , G : Ground , A : Analog , D : Digital

Pin No.	Name	I/O	Type	Description
1	RS2	I	A	Current sensing and voltage feed-forward for boost converter
2	VIN1	-	P	Main power input
3	RS1	I	A	Current sensing and voltage feed-forward for buck converter
4	PWM	O	D	PWM output for buck converter
5	CC1	O	A	Capacitor terminal for phase compensation of buck converter
6	GND2	-	G	Ground
7	VIN2	-	P	Second power input
8	VO1	O	A	3.3V output for digital part
9	GND3	-	G	Ground
10	DLY	O	A	Delay time control for RBO signal
11	RBO	O	D	Power on reset output
12	CT	O	A	Capacitor terminal for tuning oscillation frequency
13	VO2	O	A	3.3V output for analog part
14	GND4	-	G	Ground
15	VHO	O	A	15V output for CCD positive voltage
16	VREG	O	A	Internal reference voltage output
17	VNO1	I	A	Feedback voltage input for VNO (-7V typical)
18	DRV3	O	D	Driving signal output of charge pump inverter
19	GND5	-	G	Ground
20	VIN5	-	P	Power input for 15V output
21	DRV2	O	D	Driving signal output of charge pump doubler
22	VIN4	-	P	Power input for charge pump block
23	GND6	-	G	Ground
24	VLO	O	A	1.8V output
25	VIN3	-	P	Feedback voltage input for boost converter
26	DRV1	O	D	PWM output for boost converter
27	CC2	O	A	Capacitor terminal for phase compensation of boost converter
28	GND1	-	G	Ground

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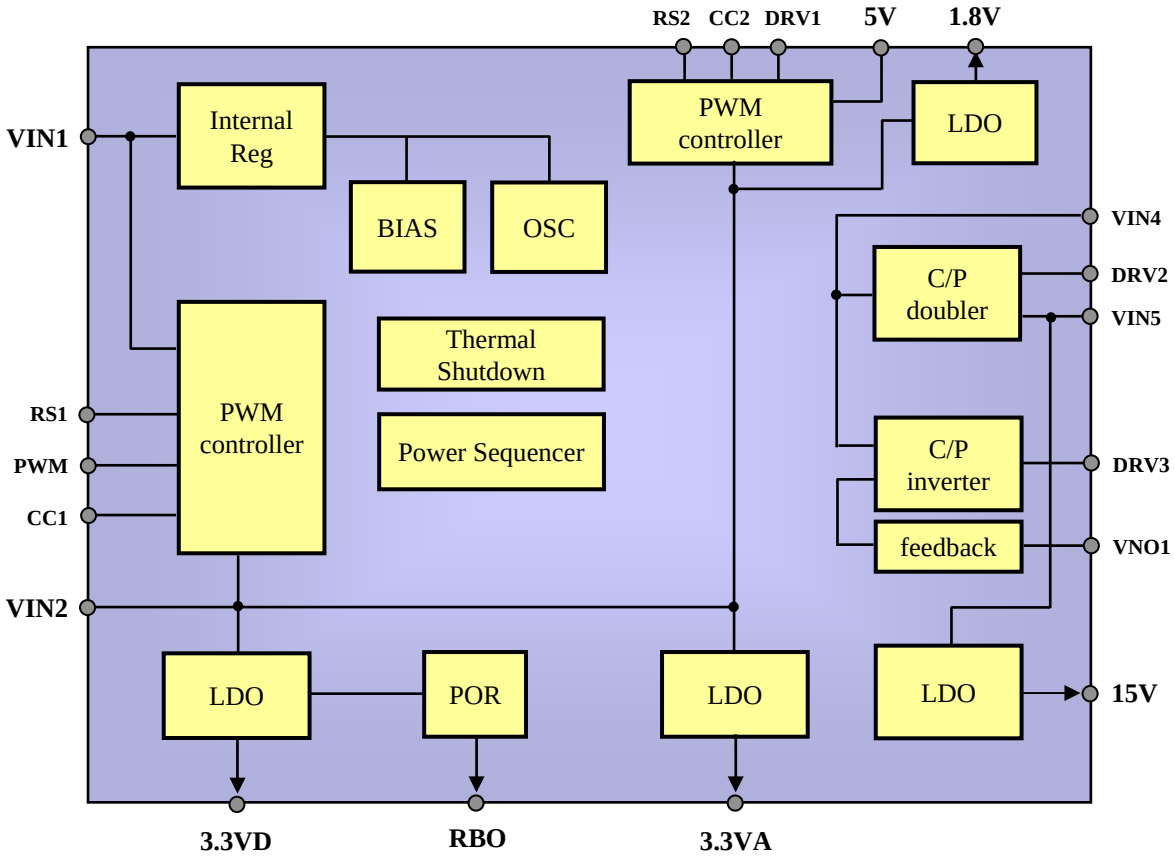
Functional Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{IN}	-	-	20	V
Power dissipation (Ta=70℃) *1	P_{Dmax}	-	-	2.2	W
Storage temperature	T_{STG}	-65	-	+150	℃
Junction temperature	T_{Jmax}	-	-	+150	℃
Thermal resistance	Θ_{JA}	-	35	-	℃/W

*1 derate 35℃/W above +70℃.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{IN}	4.75	12	18	V
Operating temperature	T_{OPR}	-20	-	+85	℃
Junction temperature	T_J	-	-	+125	℃
Max. power dissipation (Ta=70℃)*1	P_D	-	-	1.5	W

*1 This spec. indicates that junction temperature of the device is under 125℃. In specific applications, this is recommended under this power dissipation specification.

Electrical Characteristics (Ta = 25℃ , V_{IN} = 12V , unless otherwise noted.)

Parameter		Condition	Min	Typ	Max	Unit	Note
Basic Function							
Operating supply voltage		-	4.75	12	18	V	
ICC with no load		V_{IN}=12V, w/o loading	5.0	8.0	11.0	mA	
Power on reset	Tdelay	V_{IN}=12V , C30 =22nF	-	8.5	-	ms	
	VOH	-	3.0	3.3	3.6	V	
Over-temperature protection	On	Junction temperature at OT enable	-	140	-	℃	
	Off	Junction temperature at OT release	-	110	-	℃	
Efficiency		V_{IN}=12V , max. load current	-	58	-	%	
Switching frequency		Continuous mode , Ct=13pF	400	500	600	kHz	*Note1*
		Continuous mode , Ct=18pF	300	400	500	kHz	*Note2*
Buck Converter (+3.7V output)							
Output voltage (VIN2)		V_{IN}=12V	3.5	3.7	3.9	V	

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Electrical Characteristics (continued)

Parameter	Condition	Min.	Typ.	Max.	Unit	Note
+3.3VD output						
Output voltage	V_{IN}=12V , I_O=180mA	3.0	3.3	3.6	V	
Output drive current	V_{IN}=12V	-	180	200	mA	
Current limit	V_{IN}=12V	-	480	-	mA	
Load regulation	I_O=0 to 200mA	-	90	200	mV	
Ripple rejection	I_O=200mA , freq=10kHz	-	40	-	dB	
+3.3VA output						
Output voltage	V_{IN}=12V , I_O=50mA	3.0	3.3	3.6	V	
Output drive current	V_{IN}=12V	-	50	60	mA	
Current limit	V_{IN}=12V	-	180	-	mA	
Load regulation	I_O=0 to 60mA	-	60	100	mV	
Ripple rejection	I_O=60mA , freq=10kHz	-	40	-	dB	
+1.8V output						
Output voltage	V_{IN}=12V , I_O=25mA	1.7	1.8	1.9	V	
Output drive current	V_{IN}=12V	-	25	40	mA	
Current limit	V_{IN}=12V	-	200	-	mA	
Load regulation	I_O=0 to 40mA	-	20	40	mV	
Ripple rejection	I_O=40mA , freq=10kHz	-	40	-	dB	
+15V output						
Output voltage	V_{IN}=12V , I_O=5mA	14.55	15.00	15.45	V	
Output drive current	V_{IN}=12V	-	5	10	mA	
Current limit	V_{IN}=12V	-	20	-	mA	
Load regulation	I_O=0 to 10mA	-	30	50	mV	
-7V output (Rn1=45.3kΩ , Rn2=12.1kΩ , unless otherwise noted.)						
Output voltage	V_{IN}=12V , Io=-2mA	-7.5	-7.0	-6.5	V	
Output drive current	Inflow current	-	2	5	mA	
Load regulation	Io=0 to -5mA	-	30	100	mV	
Boost Converter (+5V output)						
Output voltage (VIN3)	V_{IN}=12V , I_O=80mA	4.75	5.00	5.25	V	
Maximum output current	V_{IN}=12V	-	50	100	mA	

Note 1. This switching frequency is suitable to 5V VIN operating condition.
Note 2. This switching frequency is suitable to 12V VIN operating condition.

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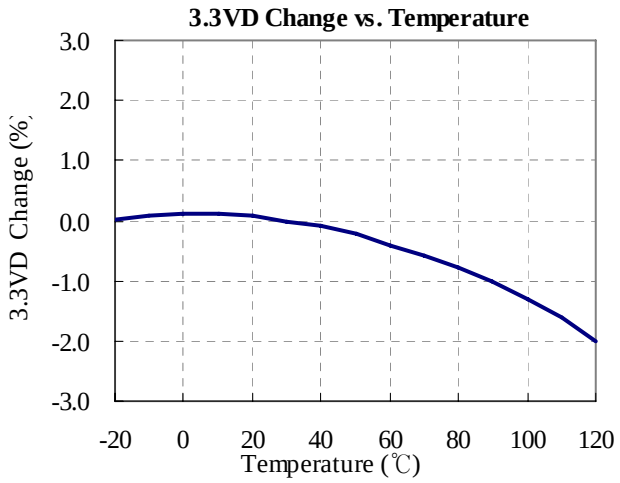
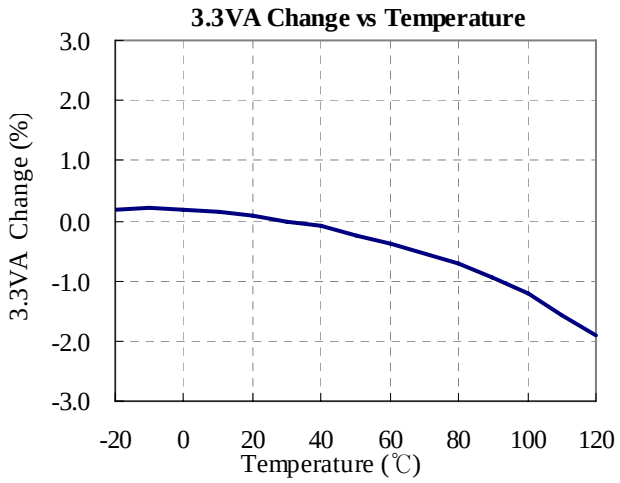
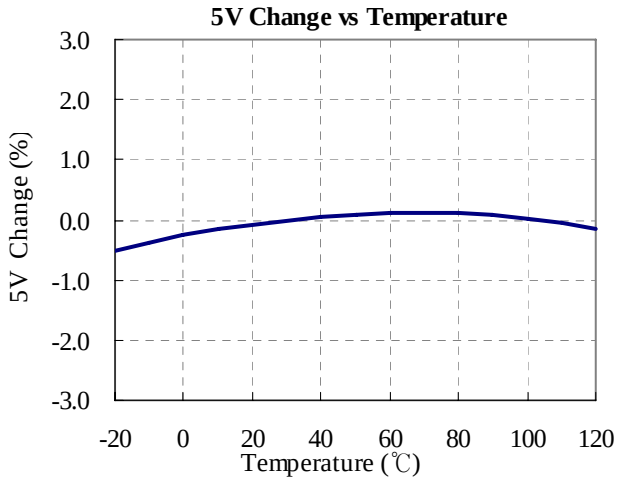
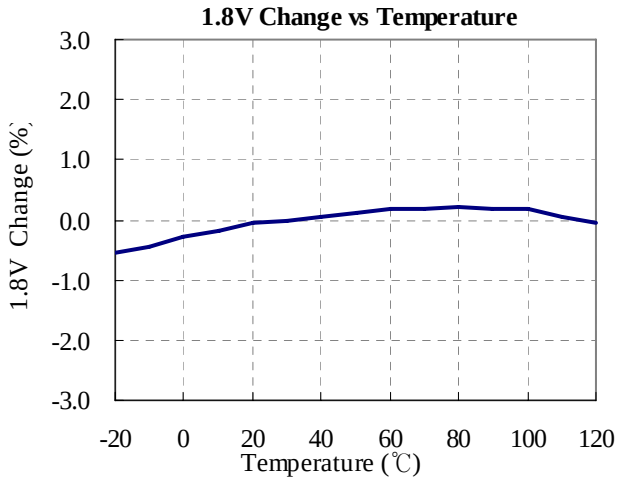
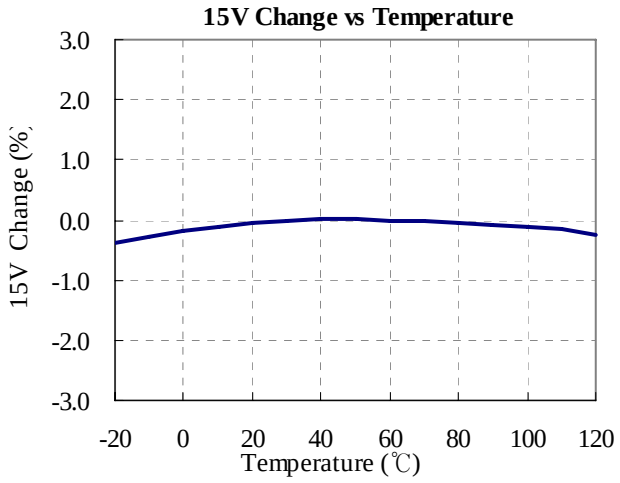
Typical Performance Characteristics

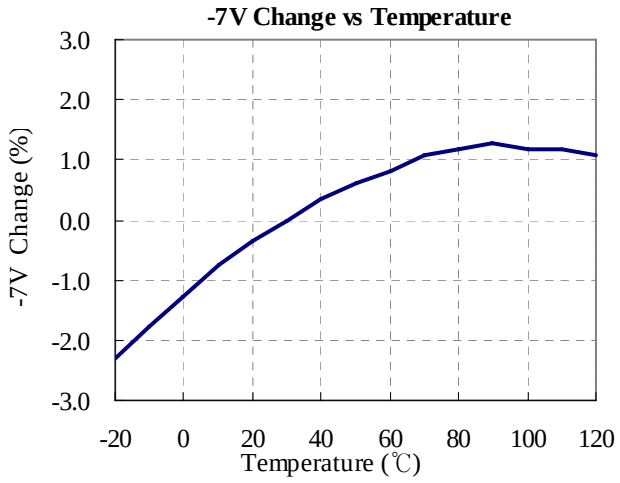












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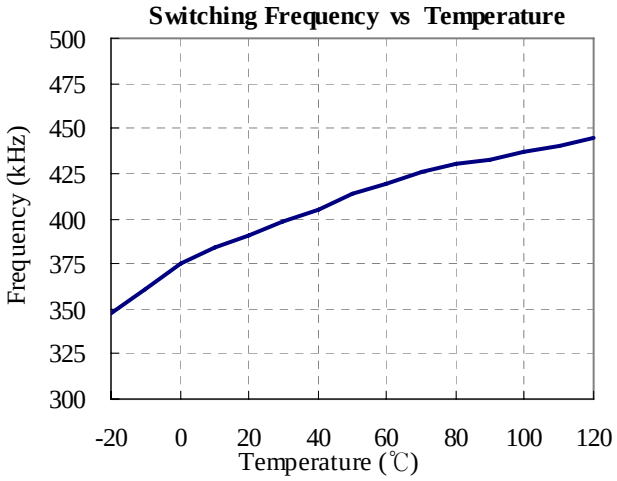
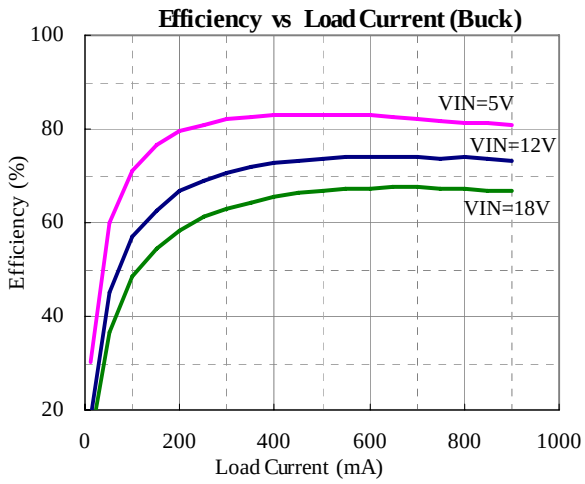
Typical Performance Characteristics





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Operation Description

DEVICE INFORMATION

The ADT7310 includes one step down DC-DC switching buck converter, one step up DC-DC switching boost converter, charge pump boost converter, charge pump inverting converter, and several LDOs.

Especially produced for powering CCD camera applications, this device provides various power channels for composing the CCD applied camera system. These channel are 3.3V, 5V, 15V , -7V and 1.8V. From these channel, it is possible to supply all the powers required for the application in one power supply device, ADT7310.

The ADT7310 is assembled with small size and thermally enhanced MLF (Micro Lead Frame) package.

With wide input operating voltage range and one stop power supply configuration, it is very easy to design new specific set.

BUCK CONVERTER

Buck converter generates internal supply voltage (approximately 3.7V). As required wide input supply range from 4.75V to 18V, intermediate power is needed. From this intermediate power all the channel outputs re-generated. Using a current mode architecture with asynchronous rectification, the buck converter have the ability to deliver sufficient current to the following power supply channels.

BOOST CONVERTER

5V output channel is generated by the boost converter. Operating with current mode step-up DC-DC converter, its input voltage is buck converter output voltage (3.7V typical). With this boost converter output, supplied the power at the following charge pump converters for generating +15V and -7V output. Also it is provided +5V output with 100mA load current independently. In case of upper 100mA load, must be considered the device's heat dissipation constraint.

CHARGE PUMP CONVERTER

By these converters the ADT7310 provides +15V and -7V channel outputs. For these two channel generation, it is used three charge pump converters, one with externally composed and others with integrated. In case of generating charge pump inverter the part of the inverter are placed at the outside of the device for its inherent limitation of negative voltage operation. -7V inverter is possible to change its output voltage by tuning the external resistors.

Note that external resistors for tuning negative voltage output required as accurate as possible. It is recommended 1% accuracy. Because -7V output is generated by two cascaded charge pump converter, this channel has operating voltage limitation. With the operation above -7.5V, it is saturated and its regulation performance degraded.

+15V channel is generated with two cascaded charge pump converters and one LDO. This channel output supplied current to CCD device. So, its channel output noise affects image to noise directly. This is why one LDO is added and therefore the ADT7310 provides clear +15V output to the system.

LDO

This device has four LDOs integrated (+3.3V 2 channel, +15V and +1.8V channel). Because the ADT7310 provided for using CCD camera application, the noise of each channel output must be minimized. Integration of LDOs trade off noiseless output and heat dissipation performance of the device. From these aspect, each channel load capability and input-output dropout conditions are designed. By these considerations this device provides optimum application function. Note that the heavy load current and high line voltage application will produce themal constraint.

POWER ON SEQUENCE

CCD camera application made by various devices requires many different supply voltages. Also with different operating rating between devices, it is seriously considered to power up sequence. Fortunately CCD camera application has only two critical power supplies, +15V and -7V for powering the CCD.

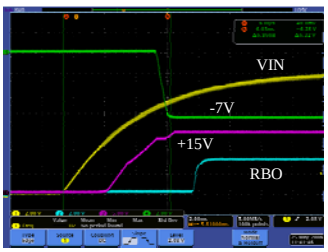
Power on sequence that the system needs is as follows :

i) the -7V must be supplied lastly.

ii) the +15V must be supplied before the -7V.

iii) other power supplies have no order.

Followed by the upper sequence, the ADT7310 operate successfully when it is powered up. Further the ADT7310 will monitor +3.3V channel voltage and generate RBO signal to reset the DSP device. This RBO signal also follows after the -7V channel settling.



** This specifications are subject to be changed without notice*

Application Hints

LDO CONSIDERATIONS

EXTERNAL CAPACITORS

The ADT7310's regulators requires external capacitors for regulator stability. These are specifically designed for CCTV camera applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

OUTPUT CAPACITOR

The LDO's are designed specifically to work with small ceramic output capacitors. And each LDO's has its own output capacitor ranges. Be sure to be connected proper output capacitor between the output pin and ground.
For using MLCC, output capacitor value is good to use more than that of the specified to 'Typical Application Circuit'.
And its required ESR range are between 10mΩ to 1Ω.

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the optimum range for stability.

The LDO's will remain stable and in regulation with no external load.

CAPACITOR CHARACTERISTICS

The LDO's are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47uF to 4.7uF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0uF ceramic capacitor is in the range of 20mΩ to 40mΩ.
The capacitor value can change greatly, depending on the operation conditions and capacitor type. So, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application.
The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Normally increasing the DC bias condition can result in the capacitance value falling below the minimum specified limit. It is therefore recommended that the capacitor manufacturer's specifications for the nominal value capacitor are consulted for all conditions.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55℃ to +125℃, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55℃ to +85℃. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25℃ to +85℃. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25℃.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47uF to 4.7uF range.
Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25℃ down to -40℃, so some guard band must be allowed.

BUCK CONSIDERATIONS

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different saturation current rating specs are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25℃ so rating at max ambient temperature of application should be requested from manufacturer.

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. A 47uH inductor with a saturation current rating of at least 590mA is recommended in this application. The inductor's resistance should be as low as possible for better efficiency. For CCTV camera application, radiated RF noise from inductor is critical for high definitive video image. In this application, a toroidal or shielded bobbin inductor should be used.

Application Hints (continued)

OUTPUT CAPACITOR SELECTION

Use a 10uF, 10V ceramic capacitor. Use X7R or X5R types, do not use Y5V.

The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as :

Voltage peak-to-peak ripple due to capacitance can be expressed as follows

$$V_{PP\text{-}C} = I_{RIPPLE} / (4 * f * C)$$

where I_{RIPPLE} : Average to peak inductor current

f : Minimum switching frequency

Voltage peak-to-peak ripple due to ESR can be expressed as follows

$$V_{PP\text{-}ESR} = (2 * I_{RIPPLE}) * R_{ESR}$$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared can be expressed as follows

$$V_{PP\text{-}RMS} = \sqrt{(V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2)}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the ESR of the output capacitor. The ESR is frequency dependent (as well as temperature dependent), make sure the value used for calculations is at the switching frequency of the part.

INPUT CAPACITOR SELECTION

The ADT7310 uses 10uF, 25V tantalum capacitor for input capacitor. Use a mix of input bypass capacitors to control the voltage overshoot. Use ceramic capacitor for the high frequency decoupling and tantalum capacitor to supply the required rms input current. Place the input capacitor as close as possible to the VIN pin of the device. The input filter capacitor supplies current to the PNP switching transistor of the converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. The input current ripple can be calculated as :

$$I_{RMS} = I_{OUTMAX} * \sqrt{1 - \frac{V_{OUT}}{V_{IN}} * \left(\frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12} \right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

where I_{OUTMAX} : maximum load current

L : min. inductor value including worst case tolerance

CHARGE PUMP CONSIDERATIONS

DOUBLER / INVERTER CAPACITOR SELECTION

The flying capacitor (CF*) transfers charge from the its input power supply to the output. A polarized capacitor (tantalum, aluminum electrolytic, etc.) must not be used here, as the capacitor will be reverse biased upon start-up of the ADT7310. The size of the flying capacitor and its ESR affect output current capability and ripple characteristic. In this applications, a 1uF, X7R or X5R type ceramic capacitor is recommended for the flying capacitor.

The load capacitor (CL1,2,3) of the charge pump plays an important part in determining the characteristics of the doubler output. The ESR of the output load capacitor affects charge pump output resistance, which plays a role in determining output current capability. Both output capacitance and ESR affect output voltage ripple. For these reasons, a low value ESR capacitor is recommended.

BOOST CONSIDERATIONS

INDUCTOR SELECTION

As previously mentioned from the inductor selection at the buck converter, inductor at the boost converter also needs to be considered two factors when choosing an inductor;
the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple.
By the property of cascading boost converter from buck converter, its inductor saturation current is lower than the that of the buck converter. In this application, the same 47uH adopted and is sufficient. Boost converter drives both its load current and the following charge pump converters for generating +15V and -7V. For proper operation at the power up time this inductor needs more saturation current than its total load current required.

OUTPUT CAPACITOR SELECTION

Use a 10uF, 10V ceramic capacitor. Use X7R or X5R types, do not use Y5V. (the same component as buck converter)

** This specifications are subject to be changed without notice*

Application Hints (continued)

The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple . These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions. Though the output ripple at the boost converter is not critical at the CCD camera application, care must be needed because its output ripple attacks other power supplies composed in the board to add ripple voltage noise and induce noise at the image. So, if produced output ripple don't affect to the image than it is recommended to choose one by considering component cost.

PCB design for optimized thermal performance

1. Overview

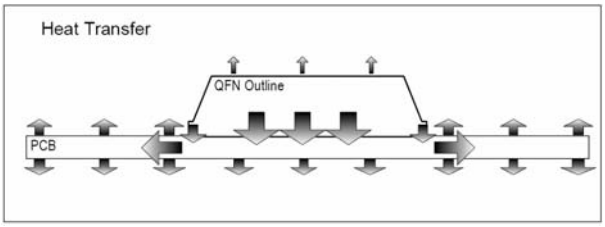
Temperature characteristic of the ADT7310 is dependant to power dissipation and heat away of the PCB pattern. Therefore, in design of the PCB pattern, Consideration of the heat away characteristic is important.

ADT7310 package is designed to provide enhanced thermal characteristics through the exposed PAD on the bottom surface of the package. Exposed PAD effectively decrease the thermal resistance, which in turn provides excellent heat dissipation from the die.
In order to take full advantage of exposed PAD, the PCB must have features to effectively conduct heat away from the package. This can be achieved by incorporating thermal PAD and thermal VIAs.

2. PCB Layout considerations

2.1 Heat transfer

For enhanced thermal performance, the exposed PAD on the package needs to be soldered to thermal PAD on the PCB. Furthermore, for proper heat conduction through the PCB, thermal VIAs need to be incorporated in the PCB in the thermal PAD region. The exposed PAD should be attached to the ground plane for proper thermal and electrical performance.
Figure 1 illustrates primary heat away through GND layer of the PCB. The presence of large metal planes in the PCB can heat away 90% of the generated heat in the ADT7310 (Reference 1)



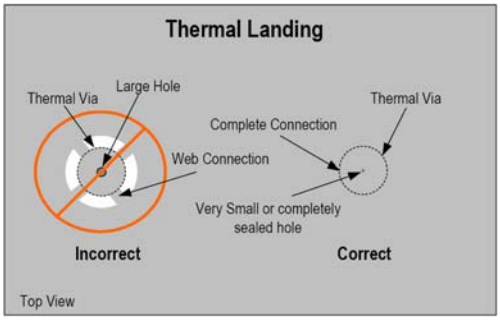
<Figure 1. Heat transfer>

2.2 Thermal PAD

To maximize thermal performance, the size of the thermal PAD should at least match the exposed PAD size. The size of the thermal PAD on the bottom PCB layer should be at least as large as the thermal PAD on the top PCB layer. It is recommended that the bottom thermal PAD be thermally connected to a GND layer (Reference 2)

2.3 Thermal VIAs

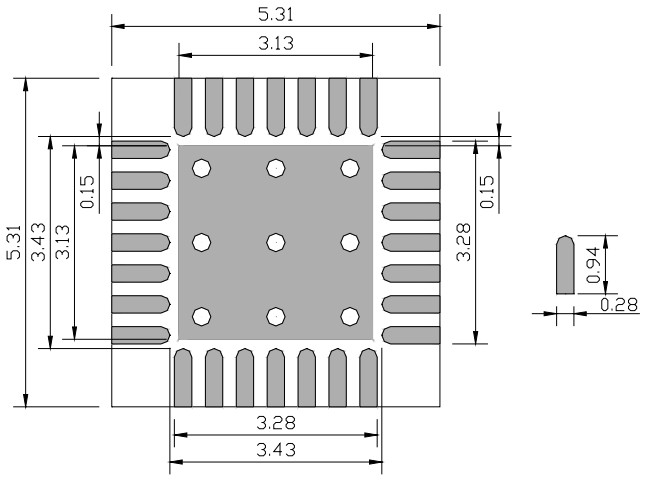
In order to effectively transfer heat from the top layer of the PCB to the bottom layers, thermal VIAs need to be incorporated into the thermal pad design. The number of thermal VIAs improve the package thermal performance. Generally, web-constructed VIA is often used in through-hole applications to facilitate the soldering of a pin to a large plane. It has a large thermal resistance to the surrounding layer. For this reason, do not use web-constructed VIA to the thermal PAD. It is recommended use completely connected VIA to the surrounding layer (Figure 2).
If the diameter of the VIAs is too large, solder will be pulled away from the exposed paddle (solder wicking) during the reflow process. This will decrease thermal characteristic of the VIA



<Figure 2. Thermal Landing and Thermal VIA>

3. Recommended PCB patterns

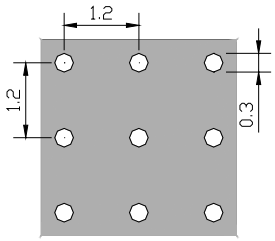
Figure 3 and 4 show adoptive PCB pattern of the ADT7310. Top and bottom of the thermal PAD patterns are the same and connected through the thermal VIAs. Also the bottom thermal PAD must be connected to adjacent ground plane. It is recommended that an array of thermal VIAs should be incorporated at 1.0 to 1.2mm pitch with VIA diameter of 0.3 to 0.33mm.



<Figure 3. PCB land pattern – Top Layer>

** This specifications are subject to be changed without notice*

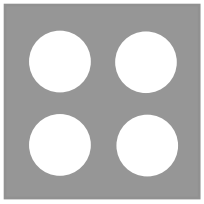
PCB design for optimized thermal performance



<Figure 4. PCB land pattern – Bottom Layer>

4. Stencil MASK

In order to effectively remove the heat from the package and to enhance electrical performance the exposed PAD needs to be soldered to the thermal PAD, preferably with minimum voids. If the solder paste coverage is too big, out gassing occurs during reflow process which may cause defects (splatter, solder balling). Therefore, It is recommended that smaller multiple openings in stencil should be used instead of one big opening for printing solder paste on the thermal PAD region (Figure 5). This will typically result in 50 to 80% solder paste coverage



1.0mm dia. Circles
@1.2mm Pitch

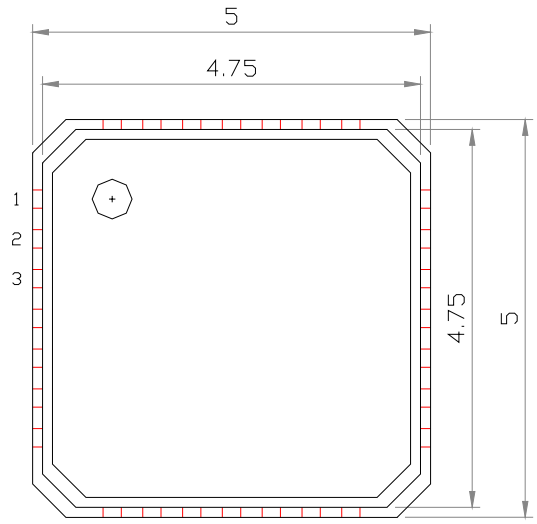
<Figure 5. Thermal PAD stencil MASK>

5. Reflow condition

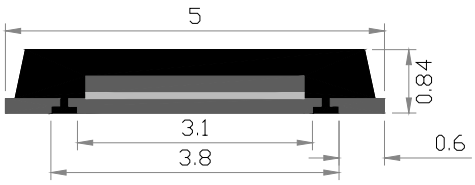
Reflow profile and peak temperature has a strong influence on void formation. Voids in the thermal PAD region reduce as the peak reflow temperature is 250~270℃. Solder extrusion from the bottom side of the PCB reduces as the reflow temperature is reduced.

Reference :
1. B.Guenin, “Packaging: Designing for Thermal Performance.” Electronics Cooling, May1997.
2. Application Note: “Application Notes for Surface Mount Assembly of Amkor’s Micro Lead Frame (MLF) Packages.” Amkor Technology, March2001

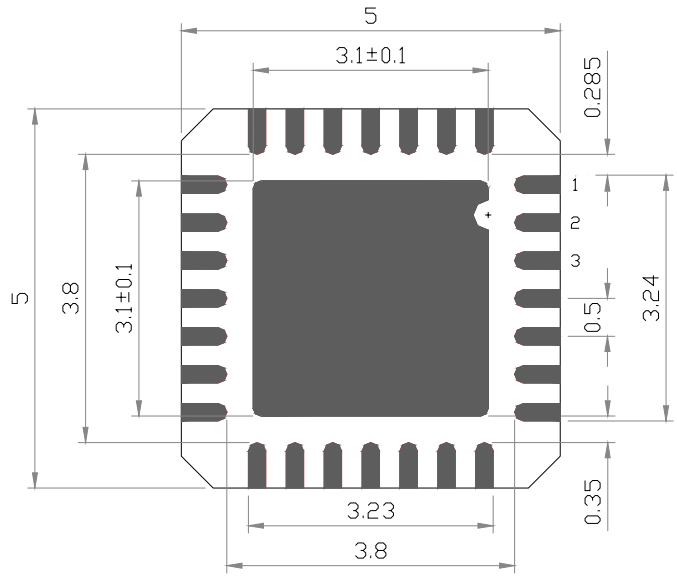
Package ; 28MLF, 5mm x 5mm body (units : mm)



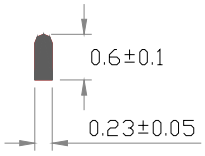
TOP VIEW



SIDE VIEW



BOTTOM VIEW



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