Future Technology Devices International Ltd

Datasheet

VDrive3 Vinculum-II Application Module

VDrive3 is a USB host/microcontroller application module with an enclosure. The default firmware of the VDrive3 supports UART/SPI communications with the embedded USB host controller and USB host port. This product provides an attractive solution for quick and easy integration of applications with a USB flash disk or other USB client devices.

1 Introduction

VDrive3 is designed to support quick and easy integration of a UART/SPI application with a USB client device. The VDrive3 comes in a neat enclosure displaying a bi-colour LED, making it suitable for incorporating into finished product designs. In addition, a product option, VDrive3-LD, is available that offers a lid to cover the USB port to provide protection in harsh environments.

The VDrive3 utilises FTDI's Vinculum-II (VNC2-48L1B) dual USB host controller IC. This IC is a microcontroller and USB host controller; it is reprogrammable using the UART interface or the Vinculum-II debugger module connecter. The default firmware is V2DAP; this firmware establishes the UART/SPI to USB host interface and can be modified or replaced with other firmware.

V2DAP is firmware that supports Vinculum-II to Vinculum backward compatibility*. The Vinculum-II IDE and FTDI's expanding range of drivers allow for additional design flexibility (including Android interfacing).

For details on the Vinculum-II collateral, please click http://www.ftdichip.com/Products/ICs/VNC2.htm

For details on FTDI Android support updates please click http://www.ftdichip.com/Android.htm.

1.1 Features

VDrive3 has the following features:

- Vinculum-II microcontroller/USB host controller IC.
- Product available as shown or with a lid covering the USB port.
- USB "A" type socket to connect to USB client devices.
- 2mm (0.08") pitch 8 pin header used for the UART/SPI interface.
- Connects directly and communicates with a FTDI TTL-232R-3V3-2mm USB-UART cable.
- Jumper selectable UART and SPI interfaces, both operating at 3.3V TTL/CMOS.
- Pre-programmed with V2DAP firmware
- Vinculum-II debugger module port under neat enclosure, for changing the firmware.
- UART programming mode control signals PROG# and RESET# are accessible via an internal header.
- The VDrive3 and all components used are Pb-free (RoHS compliant).

*See section 5

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2 Ordering Information

Module Code	Utilised IC Code	Description
VDRIVE3	VNC2-48L1B	USB host application module with enclosure.
VDRIVE3-LD	VNC2-48L1B	USB host application module with enclosure and protective lid over USB connector.

Table 2-1 – Ordering Information

3 VDrive3 Signals and Configurations

3.1 VDrive3 Pin-Out

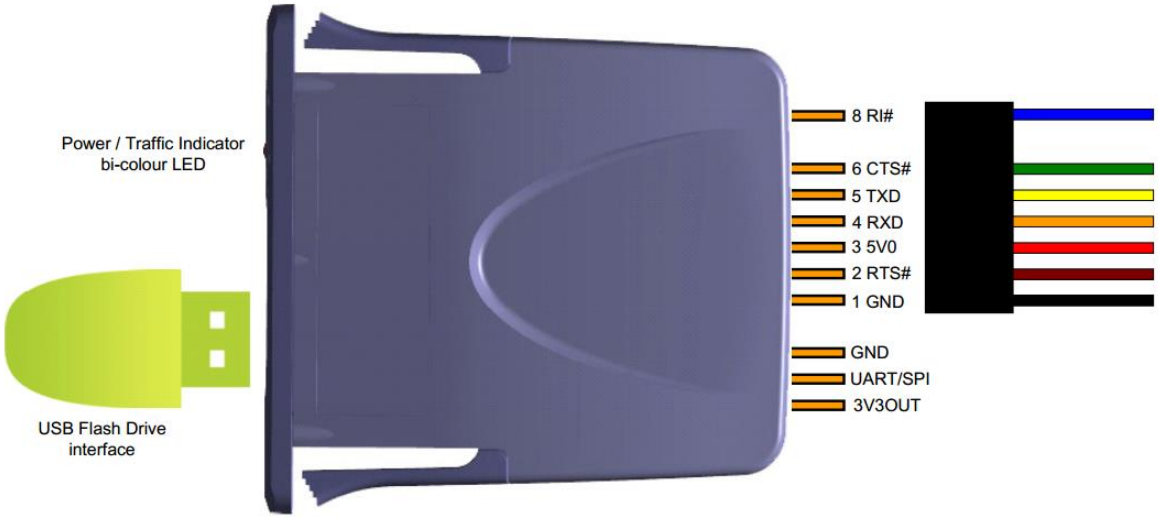

Figure 3.1 – VDrive3 Pin Out (in UART mode)

The pin-out of the VDrive3 is illustrated in Figure 4.1.

3.2 VDrive3 Jumper Configuration

The interface modes of the VDrive3 running on a V2DAP firmware is given in Table 3-1. The VDrive3 comes preloaded with the V2DAP firmware and the jumper on the UART/SPI pin is set to UART mode by default.

UART/SPI	Interface Mode
Pull-Up	UART
Pull-Down	SPI

Table 3-1 – VDrive3 Jumper Box

3.3 LED Functions

Operation	LED Behaviour
Power On	LED flashes Green/Red alternately for 2 seconds Repeated until monitor connects
USB Disk Initialisation	LED Red
USB Disk Ready	LED Green
USB Disk Removed	LED off
Disk is connected to USB Port	LED flashes Green
Nothing is connected to USB Port	LED off

Table 3-2 – VDrive3 LED Functions

3.4 Interface Description

Pin No.	Name	Type	Description
1	GND	PWR	Signal ground
2	RTS#	Output	Request To Send control output – Handshake signal
3	5V0	PWR	5V supply input
4	RXD	Input	Receive asynchronous data input
5	TXD	Output	Transmit asynchronous data output
6	CTS#	Input	Clear To Send control input - Handshake signal
7	NC	-	No Connect
8	RI#/WU	Input	Ring Indicator control input / Wake Up

Table 3-3 – 3.3V TTL/CMOS UART Interface Pin-Out

Pin No.	Name	Type	Description
5	SCLK	Input	SPI clock input. Maximum frequency: 24MHz – 3.3V TTL
4	MOSI	Input	SPI slave serial data input – 3.3V TTL
2	MISO	Output	SPI slave serial data output – 3.3V TTL
6	SS#	Input	SPI slave select input – 3.3V TTL

Table 3-4 – 3.3V TTL/CMOS SPI Interface Pin-Out

For further details see VNC2 datasheet.

4 VDrive2 and VDrive3 Comparison

The VDrive3 is a drop in replacement for the VDrive2 for the majority of VDrive2 applications. However, for a small number of applications that use SPI some changes to the application software may be required, this is due to a discrepancy in the SPI interface used in the Vinculum-I and Vinculum-II. For further details on these differences, please see AN_176 - Vinculum Comparison of VDAP and V2DAP.

Note: VDrive3's default firmware includes a reflash function, allowing the firmware to be updated from a flash drive. This reflash can be performed with the following steps:

1: Configure the VDrive3 into UART mode.

2: Open a communication terminal and connect to the VDrive3 via the UART interface.

3: Connect a USB flash disk with any firmware named "FTRFBV2.FTD".

4: Wait for the new firmware to be loaded.

Additional features of the VDrive3:

- Vinculum-II can be configured by a user defined firmware
- VDrive3 hardware has an SPI master interface available. (not enabled by default in V2DAP firmware)
- VDrive3's SPI interface can be clocked up to 48MHz
- VDrive3 is programmable using the debugger-module port and the UART interface port.
- VDrive3 can utilise many of the Vinculum-II's sample firmware available on the FTDI website.

5 VDrive3 Application Example

5.1 UART Interface to PIC Example

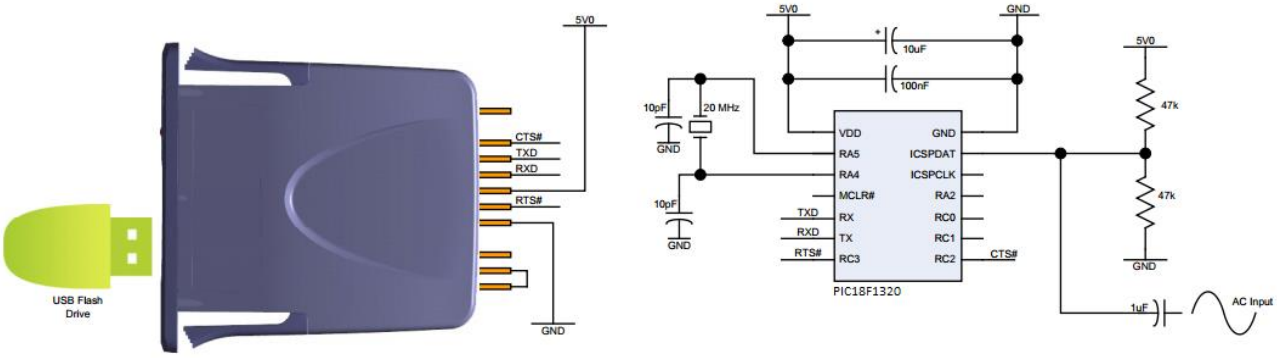

Figure 5.1 – VDrive3 UART example

The VDrive3 provides solutions for quick and easy integration of UART/SPI applications with USB slave devices. An application is illustrated in Figure 5.1, in this example the VDrive3 is connected to a microcontroller and peripheral components to form a flash disk based data logger. This application example also illustrates an analogue signal connected to the 10-bit analogue to digital input of a PIC18F1320, the analogue signal can be sourced from a wide variety of sensors.

The PIC code takes a pre-defined number of samples and then writes the corresponding ASCII values to a Comma Separated Value (CSV) file on the USB flash disk attached to the VDrive3 module. Vinculum-II's DOS like ASCII commands simplify the task of file handling. An extended ASCII command set is designed for use with a terminal whilst a shortened hexadecimal version is used with a microcontroller.

For details on this application please see "VNC1L-Data-Logging Example" on the following web page:
http://www.ftdichip.com/Support/SoftwareExamples/VinculumProjects.htm

6 VDrive3 Electrical Details

6.1 SPI Interface Timing

The following timing diagrams are for the VNC1L Legacy Interface mode of SPI slave.

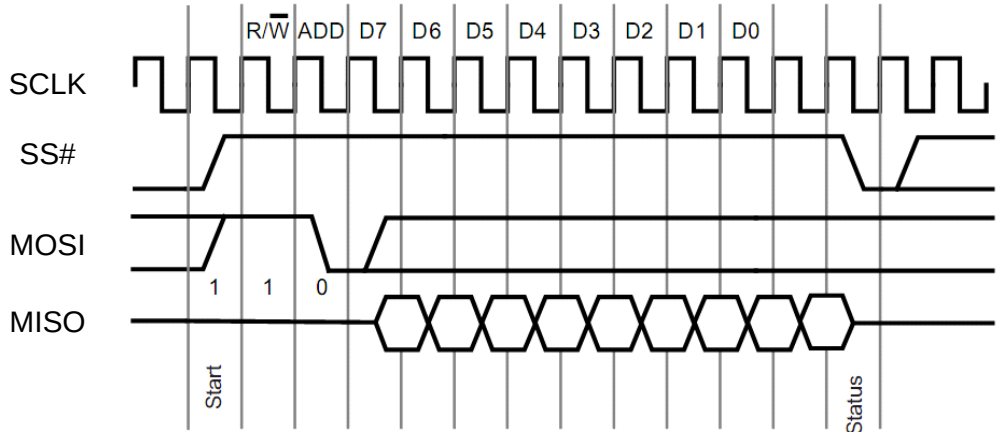

Figure 6.1 – VDrive2 SPI example

To start the data transfer process SS# needs to be set to high, and remain high for the entire read cycle. Once the read cycle is complete SS# needs to be set to low for at least one clock cycle to allow another data transfer cycle to occur.

The first bit of MOSI is the R/W bit, receiving a logic high for this bit allows data to be read from the VDrive3. The second bit is the address bit, ADD; this bit is used to select data read from the data register when set to logic high, and read from the status register when set to logic low. During an SPI Read cycle, a package of data is transmitted from the VDRIVE3 on the MISO line from the time of the first clock cycle after the SPI ADD bit, with the MSB transmitted first.

After the data has been transferred the status of MISO can be checked to determine if the data read is new data as indicated by a transmitted logic low. If old data is transmitted, as indicated by a transmitted logic high, the read cycle needs to be repeated to get new data.

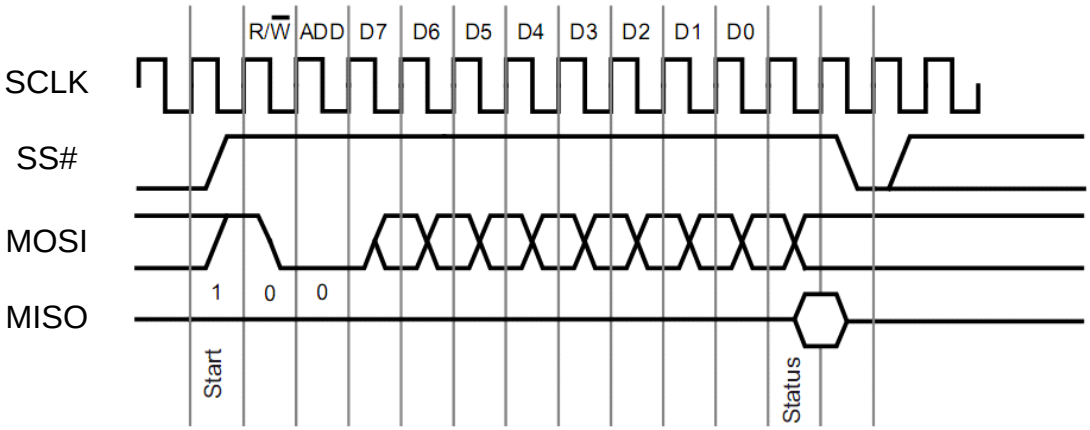

Figure 6.2 – VDrive3 SPI example

To start the data transfer process SS# needs to be set to high for the entire write cycle. Once the write cycle is complete SS# needs to be set low for at least one clock cycle to allow another data transfer cycle to occur.

The first bit of MOSI is the R/W bit, receiving a logic low for this bit allows data to be written to the VDrive3. The second bit is the address bit, ADD, this bit is used to select a data write to the data register when set to logic high, and to the status register when set to logic low. During an SPI Write cycle a package of data is transmitted to the VDRIVE3 on the MOSI line from the time of the first clock cycle after the SPI ADD bit, with the MSB transmitted first.

After the data has been transferred, the status of MISO can be checked to determine if the data written has been accepted. If a logic low is given for the status bit, it can be determined that the data write was successful. If a logic high is given for the status bit, the internal buffer of the device receiving data is full, and the same write cycle should be repeated.

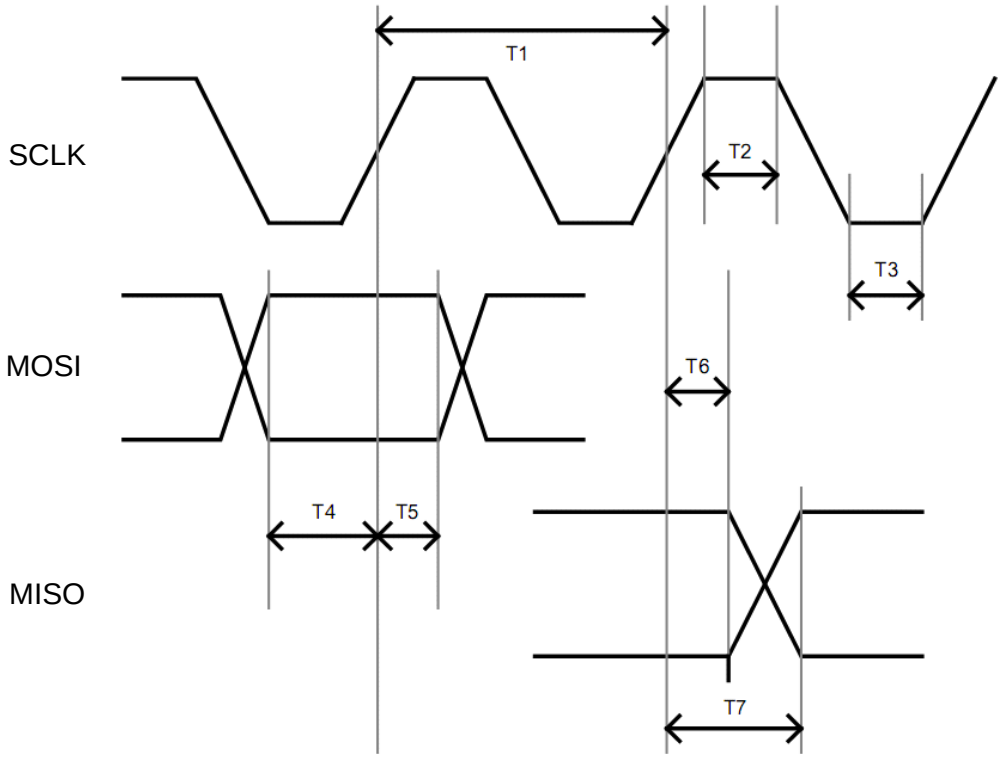

Figure 6.3 – VDrive3 SPI example

Time	Description	Min	Typical	Max	Unit
T1	SCLK Period	83	-	-	ns
T2	SCLK High	20	-	-	ns
T3	SCLK Low	20	-	-	ns
T4	Input Setup Time	10	-	-	ns
T5	Input Setup Time	10	-	-	ns
T6	Input Hold Time	2	-	-	ns
T7	Output Valid Time	-	-	20	ns

Table 6-1 – SPI Interface Pin-Out

7 VDrive3 Max-Ratings

The absolute maximum ratings for the VDrive3 devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-40°C to 85°C	Degrees C	
Ambient Operating Temperature (Power Applied)	-30°C to 85°C	Degrees C	
VCC Supply Voltage	-0.3 to +5.5	V	
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V	

Table 7.1 – Absolute Maximum Ratings

8 VDrive3 Mechanical Details

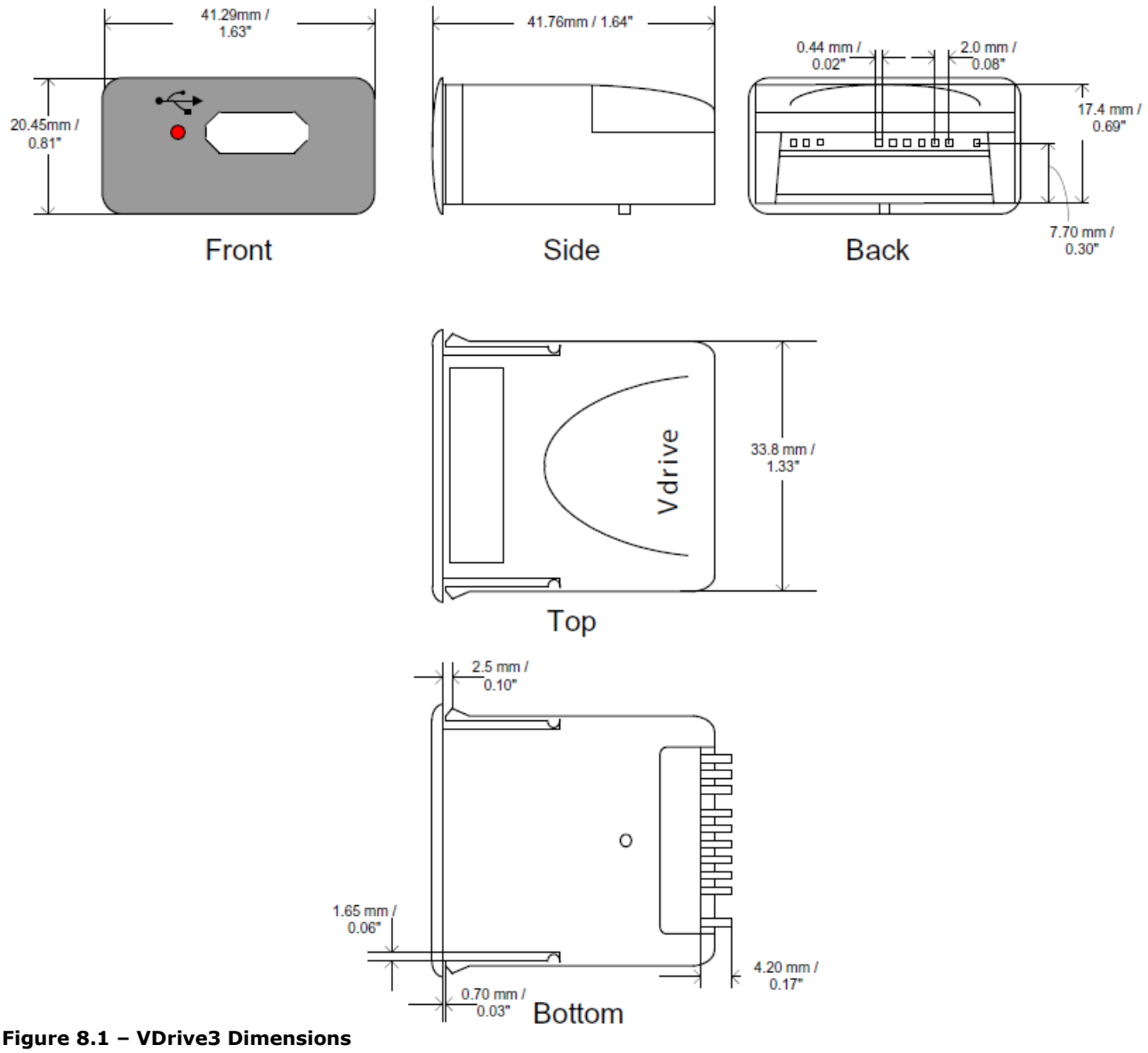

Figure 8.1 – VDrive3 Dimensions

Full detailed mechanical drawings for the VDrive3 enclosure are available on request from FTDI technical support.

9 VDrive3-LD Mechanical Details

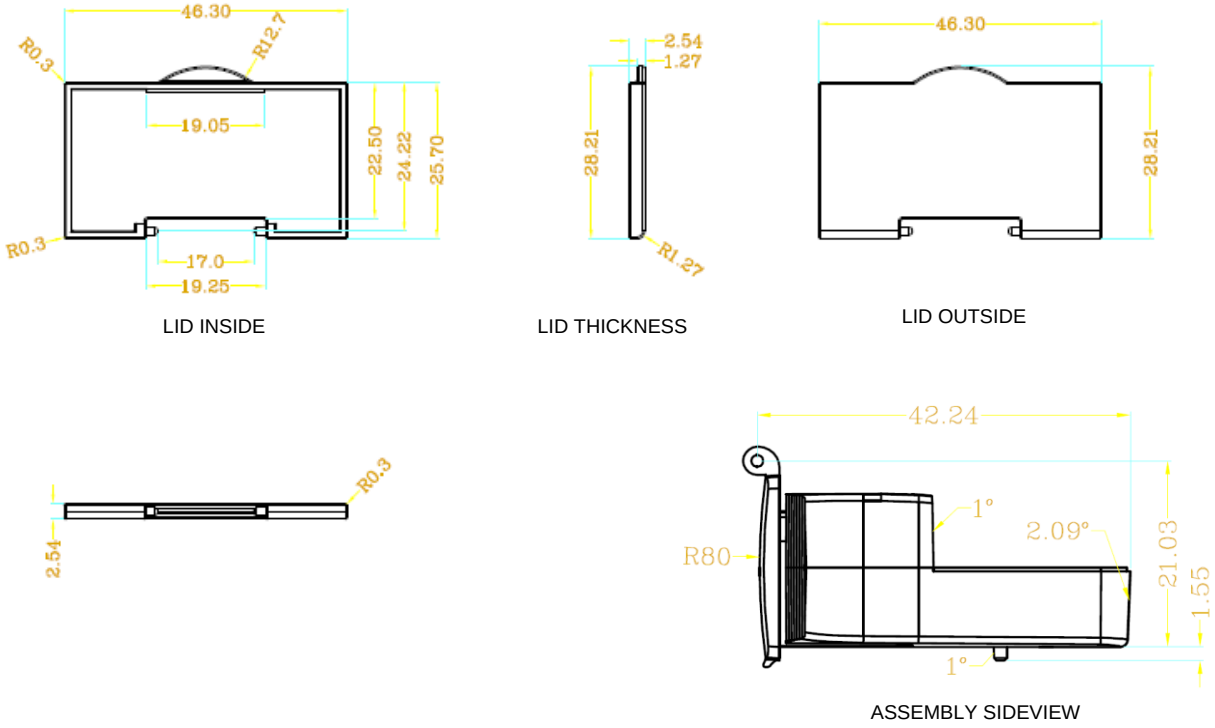

Figure 9.1 – VDrive3-LD Dimensions

Full detailed mechanical drawings for the VDrive3-LD enclosure are available on request from FTDI technical support.

10 VDrive3 Schematic

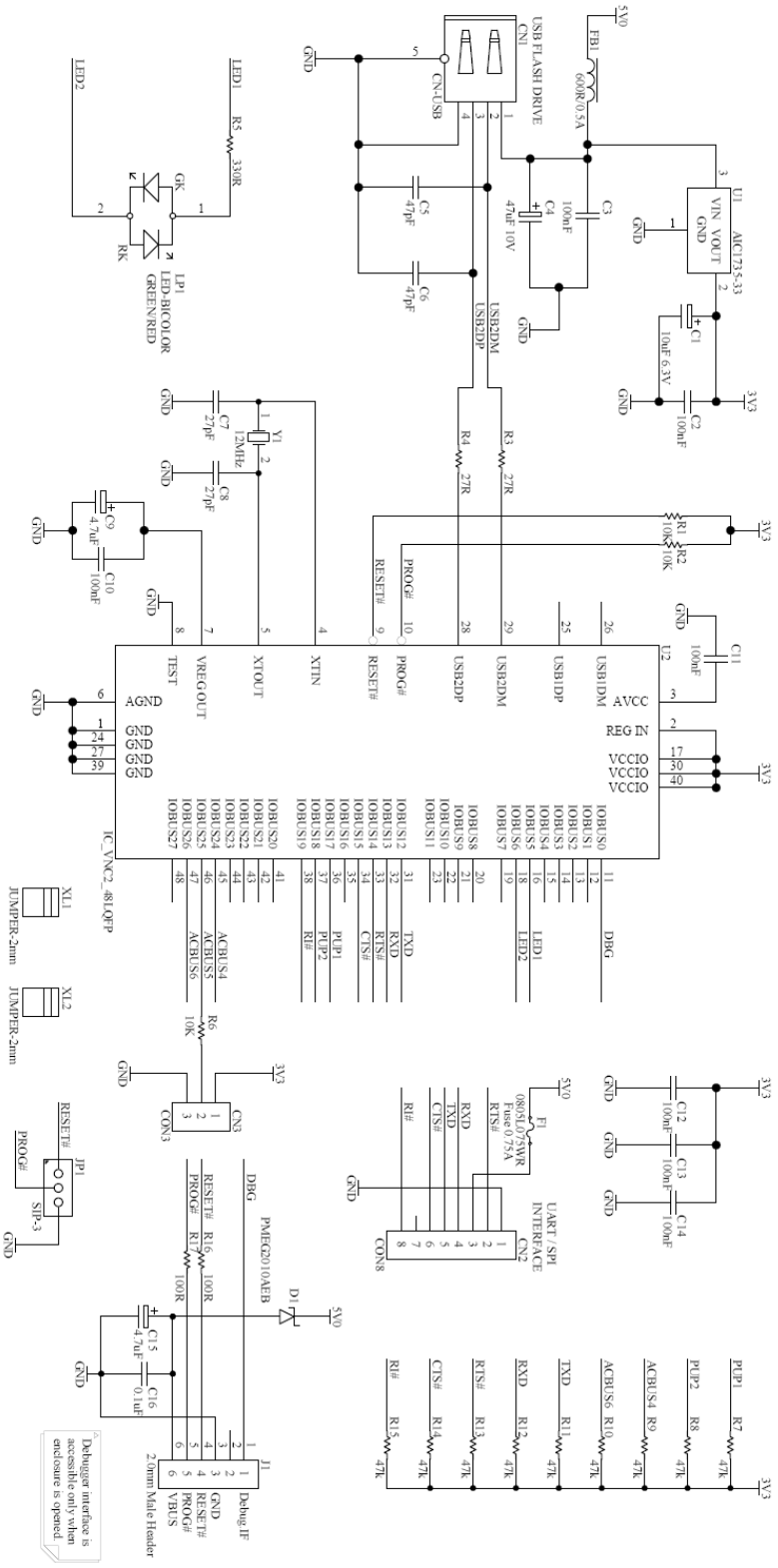

Figure 10.1 – Module Circuit Schematic

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

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Appendix B – Revision History

Document Title:	VDrive3
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Version 1.0	First issue	08/04/13
Version 1.1	Added new VDRIVE3-LD info	15/08/13
Version 1.2	Corrected dimension of case width	16/09/13

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