ANADIGICS

AWS5522

0.5 to 2.5 GHz SPDT Switch

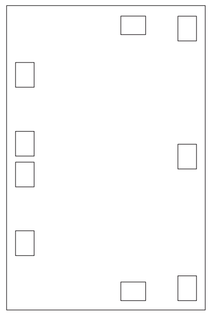
ADVANCED PRODUCT INFORMATION - Rev 0.1

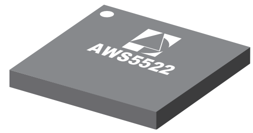
FEATURES

- Low Insertion Loss: 0.5 dB at 2 GHz
- High Isolation: > 25 dB
- Low Harmonic Levels: < -65 dBc
- Low Control Voltage Operation: to +2.5 V
- Low Profile Surface Mount Package

APPLICATIONS

- GSM Wireless Handsets and Front-end Modules
- CDMA Wireless Handsets and Front-end Modules





D1 Die	**S26 Package 12 Pin MLF 3mm x 3mm**

PRODUCT DESCRIPTION

The AWS5522 is a single pole, double throw (SPDT) RF switch developed to meet the stringent requirements of GSM and CDMA systems. Manufactured in ANADIGICS's state-of-the-art pHEMT process, the device uses patent-pending circuit topologies to provide the low insertion loss, high port-to-port isolation and high linearity needed to enhance the performance of wireless handset radios. The AWS5522 is offered both as an MMIC die and in a 12-lead 3mm x 3mm MLF package.

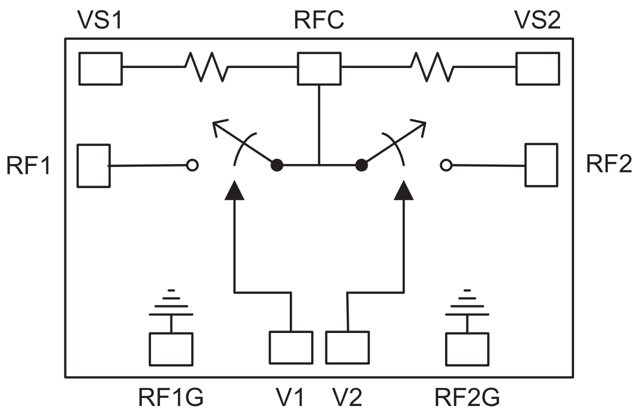
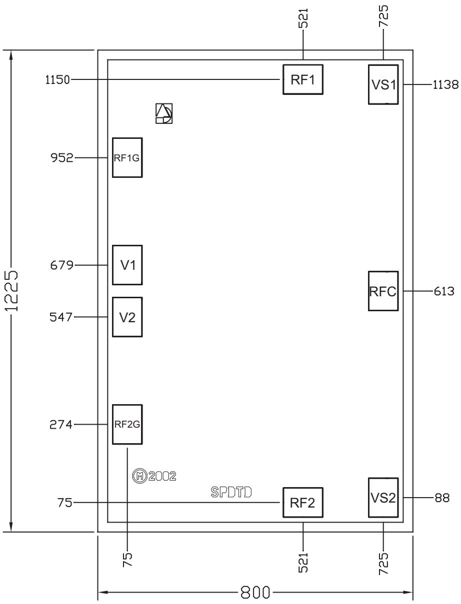


Figure 1: Block Diagram



Dimensions in µm.
Bond Pads: 100µm x75µm
Die Thickness: 178µm
No backside metal.

Figure 2 : Die Configuration

Table 1 : Pad Description

NAME	DESCRIPTION
VS1	Common port bias voltage (logic high)
RF1	RF port, path 1
RF1G	Ground
V1	Control voltage, RF path 1
V2	Control voltage, RF path 2
RF2G	Ground
RF2	RF port, path 2
VS2	Common port bias voltage (logic high)
RFC	RF common port

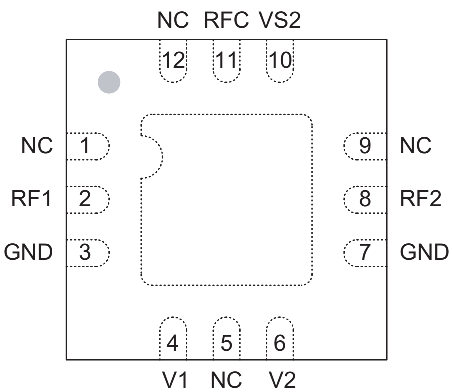


Figure 3: Packaged Device Pinout (X-ray Top View)

Table 2: Pin Description

PIN	NAME	DESCRIPTION
2	RF1	RF port, path 1
4	V1	Control voltage, RF path 1
6	V2	Control voltage, RF path 2
8	RF2	RF port, path 2
10	VS2	Common port bias Voltage (logic high)
11	RFC	RF common port
3, 7	GND	Ground
1, 5, 9, 12	NC	No connection

ELECTRICAL CHARACTERISTICS

Table 3: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT	COMMENTS
Common Port Bias Voltage (V_S)	-0.2	+8.0	V	at VS1 or VS2 (1)
Control Voltages (V_1, V_2)	-0.2	+8.0	V	
RF Input Power (P_{IN})	-	10	W	at RF1, RF2 and RFC
Storage Temperature (2)	-65	+150	°C	

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:
(1) The VS1 and VS2 ports may remain open-circuited without damage to the device.
(2) Storage Temperature limits apply to the die only after it has been removed from the ANADIGICS shipping material. (The limits apply at all times for the packaged device.)
3. The RF1, RF2 and RFC ports should be AC-coupled. No external DC bias should be applied.

Table 4: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
RF Frequency (f)	0.5	-	2.5	GHz	
Common Port Bias Voltage (V_S)		(1)			applied at either VS1 or VS2 port
Control Voltages (V_1, V_2)	0 +2.5	- -	+0.2 +3.5	V	RF path OFF state RF path ON state
Ambient Temperature (T_A)	-30	-	+85	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:
(1) For optimal linearity performance, the Common Port Bias Voltage (V_S) should be set to the same Control Voltage used to turn ON either of the individual RF paths. The VS1 and VS2 ports may remain open-circuited without damage to the device, but with some degradation in linearity.

Table 5: Electrical Specifications - Unpackaged Die
(T_A = +25 °C; RF ports terminated with 50 Ω; V_n = +2.7 V and is the Control Voltage for the ON path, RFC-RFn; V_x = 0 V and is the Control Voltage for the OFF path, RFC-RFx)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Insertion Loss 1 GHz 2 GHz	 - -	 0.4 0.5	 0.6 0.8	dB	RFC port to selected RFn port
Return Loss (1) 1 GHz 2 GHz	 - -	 -30 -32	 -20 -20	dB	RFC port and selected RFn port
Isolation 1 GHz 2 GHz	 25 25	 27 27	 - -	dB	RFC port to isolated RFx port
Input Third Order Intercept (2) 800 MHz Cellular Band 1900 MHz PCS Band	 - -	 +60 +59	 - -	dBm	RFC port to selected RFn port
2nd Harmonic Rejection (3) 1 GHz 2 GHz	 - -	 -79 -78	 -65 -65	dBc	P_{IN} = +34 dBm P_{IN} = +32 dBm
3rd Harmonic Rejection (3) 1 GHz 2 GHz	 - -	 -88 -81	 -65 -65	dBc	P_{IN} = +34 dBm P_{IN} = +32 dBm
Current Consumption	- -	- -	30 5	μA μA	each Vn port VS1 or VS2 port

Notes:
(1) The isolated RFx port has a return loss of approximately -3 dB.
(2) For the Cellular Band, two tones with P_{IN} = +22.5 dBm each, at 900.0 and 900.1 MHz. For the PCS Band, two tones with P_{IN} = +21 dBm each, at 1900.0 and 1900.1 MHz.
(3) $V_s = V_n$

Table 6: Switch Control Truth Table

CONTROL VOLTAGES		RF PATH SELECTION	
V_1	V_2	RFC - RF1	RFC - RF2
+2.5 to +3.5 V	0 to +0.2 V	ON	OFF
0 to +0.2 V	+2.5 to +3.5V	OFF	ON

Table 7: Electrical Specifications - Packaged Device
(T_A = +25 °C; RF ports terminated with 50 Ω; V_n = +2.7 V and is the Control Voltage for the ON path, RFC-RFn; V_x = 0 V and is the Control Voltage for the OFF path, RFC-RFx)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Insertion Loss 1 GHz 2 GHz	 - -	 0.4 0.5	 -0.6 -0.8	dB	RFC port to selected RFn port
Return Loss (1) 1 GHz 2 GHz	 - -	 -28 -33	 -20 -20	dB	RFC port and selected RFn port
Isolation 1 GHz 2 GHz	 25 25	 27 27	 - -	dB	RFC port to isolated RFx port
Input Third Order Intercept (2) 800 MHz Cellular Band 1900 MHz PCS Band	 - -	 +60 +59	 - -	dBm	RFC port to selected RFn port
2nd Harmonic Rejection (3) 1 GHz 2 GHz	 - -	 -75 -76	 -65 -65	dBc	P_{IN} = +34 dBm P_{IN} = +32 dBm
3rd Harmonic Rejection (3) 1 GHz 2 GHz	 - -	 -70 -74	 -65 -65	dBc	P_{IN} = +34 dBm P_{IN} = +32 dBm
Current Consumption	- -	- -	30 5	µA µA	each Vn port VS2 port

Notes:
(1) The isolated RFx port has a return loss of approximately -3 dB.
(2) For the Cellular Band, two tones with P_{IN} = +22.5 dBm each, at 900.0 and 900.1 MHz. For the PCS Band, two tones with P_{IN} = +21 dBm each, at 1900.0 and 1900.1 MHz.
(3) $V_s = V_n$

PERFORMANCE DATA

Figure 4: Insertion Loss vs. Frequency Unpackaged Die (ON path, V_n = +2.7 V, V_x = 0 V)

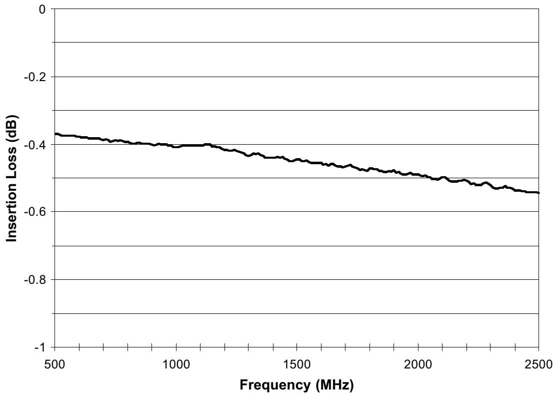


Figure 5: Insertion Loss vs. Frequency Packaged Device (ON path, V_n = +2.7 V, V_x = 0 V)

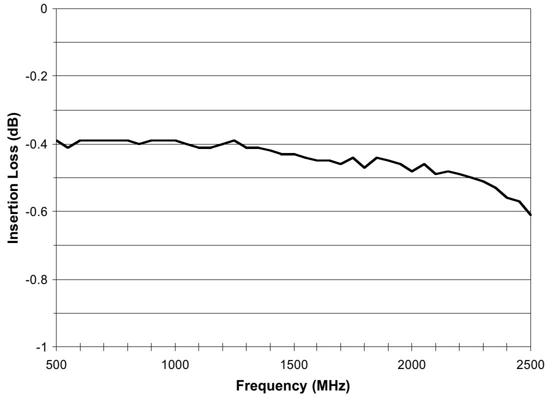


Figure 6: Return Loss vs. Frequency Upackaged Die (ON path, V_n = +2.7 V, V_x = 0 V)

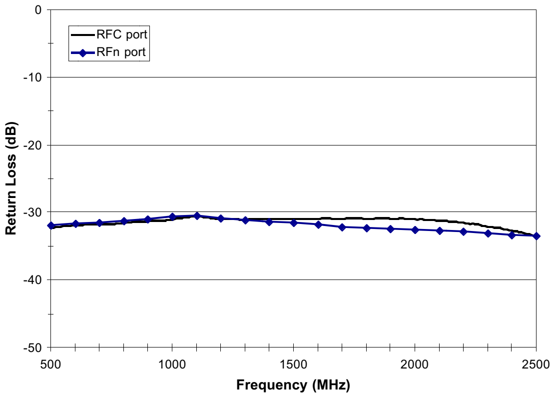


Figure 7: Return Loss vs. Frequency Packaged Device (ON path, V_n = +2.7 V, V_x = 0 V)

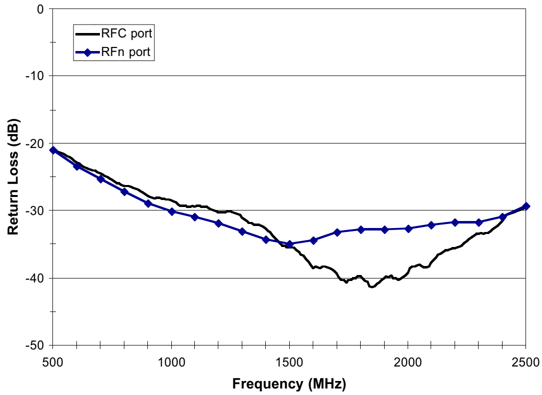


Figure 8: Isolation vs. Frequency Unpackaged Die (OFF path, V_n = +2.7 V, V_x = 0 V)

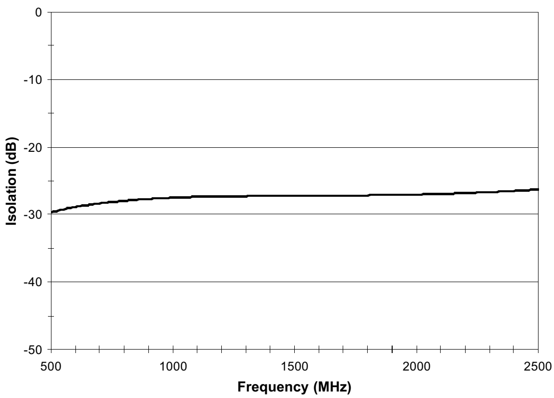


Figure 9: Isolation vs. Frequency Packaged Device (OFF path, V_n = +2.7 V, V_x = 0 V)

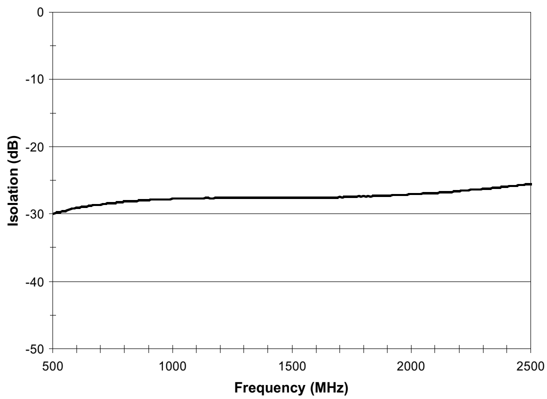


Figure 10: Harmonics of 1 GHz vs. Control Voltage Unpackaged Die (ON path, V_x = 0 V, f = 1 GHz, P_{IN} = +34 dBm)

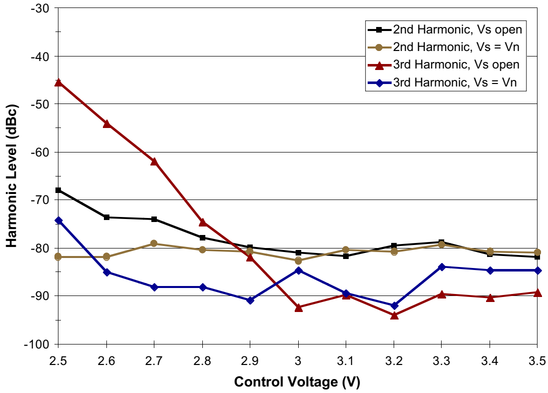


Figure 11: Harmonics of 1 GHz vs. Control Voltage Packaged Device (ON path, V_x = 0 V, f = 1 GHz, P_{IN} = +34 dBm)

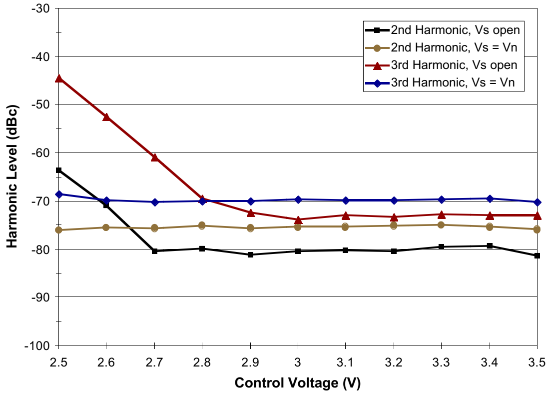


Figure 12: Harmonics of 2 GHz vs. Control Voltage Unpackaged Die (ON path, V_x = 0 V, f = 2 GHz, P_{IN} = +32 dBm)

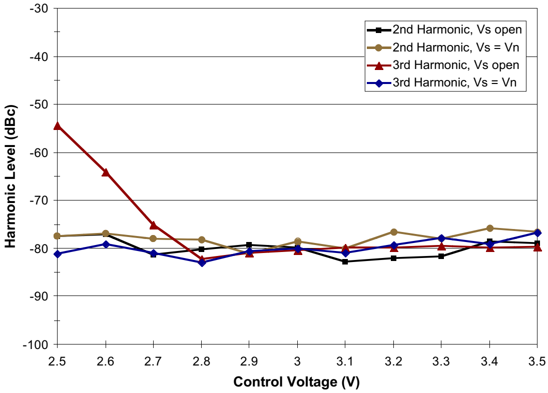
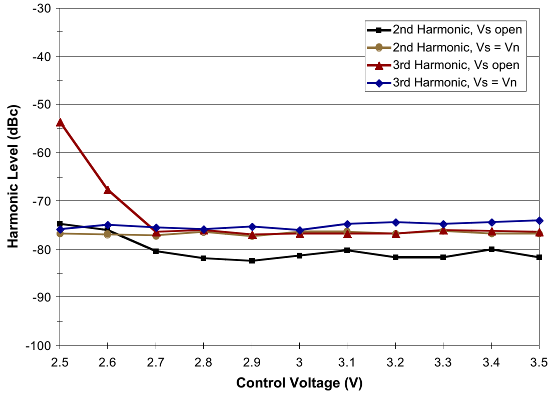


Figure 13: Harmonics of 2 GHz vs. Control Voltage Packaged Device (ON path, V_x = 0 V, f = 2 GHz, P_{IN} = +32 dBm)



APPLICATION INFORMATION

Unpackaged Die Applications

Bonding and circuit connections for the unpackaged AWS5522 die are shown in Figure 14, and application details are listed in the following notes:

1. Cb are DC blocking capacitors external to the device. A value of 100pF is sufficient for operation to 500MHz. The values may be tailored to provide specific electrical responses. The isolation of the switch provides enough decoupling of the RF1 and RF2 ports so that overall switch performance is not affected.

2. The VS1 and VS2 pins provides a fixed voltage potential to the common port of the switch. To get the best linear performance, either VS1 or VS2 should be tied to the logic high voltage potential (not the power supply). Only one of these pins need be attached, with the decision determined by external circuit layout. Current draw on this pin is less than 5µA.

3. The RF Ground bondwires should be kept as short as possible and bonded directly to a good RF ground for best broadband performance.

4. L_{ESD} provides a means to increase the ESD protection on a specific RF port, typically the port attached to the antenna. The ESD rating of the device is ±125V HBM overall. This rating is associated with the control pin to RF port path. RF port to RF port/RF Gnd has been determined to be >±500V HBM for this technology. By using L_{ESD} as an RF choke on a port, an ESD protection to ±8kV contact discharge can be achieved.

5. The die may be attached by either conductive or non-conductive epoxy formulated for attaching semiconductor parts. The back of the die is electrically isolated from the switch circuit and can be grounded or left isolated.

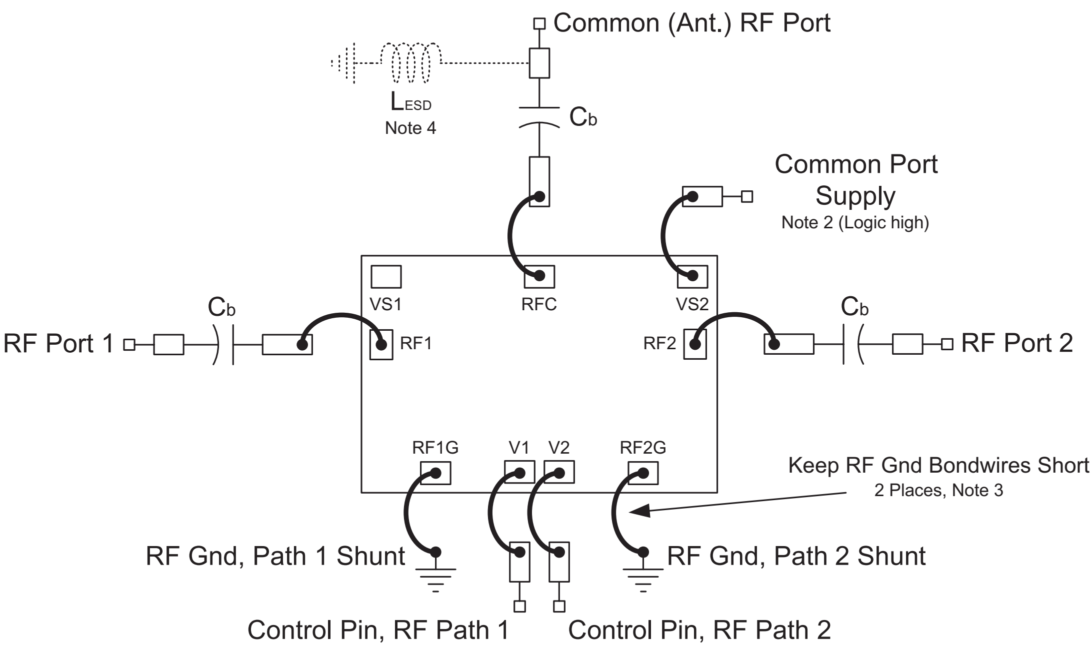


Figure 14: Unpackaged Die Application Schematic

Packaged Device Applications

External component requirements for the packaged AWS5522 device are shown in Figure 15, and application details are listed in the following notes:

1. Cb are DC blocking capacitors external to the device. A value of 100pF is sufficient for operation to 500MHz. The values may be tailored to provide specific electrical responses. The isolation of the switch provides enough decoupling of the RF1 and RF2 ports so that overall switch performance is not affected.

2. The VS2 pin provides a fixed voltage potential to the common port of the switch. To get the best linear performance, VS2 should be tied to the logic high voltage potential (not the power supply). Current draw on this pin is less than 5μA.

3. The RF Ground connections should be kept as short as possible and tied directly to a good RF ground for best broadband performance.

4. L_{ESD} provides a means to increase the ESD protection on a specific RF port, typically the port attached to the antenna. The ESD rating of the device is ±125V HBM overall. This rating is associated with the control pin to RF port path. RF port to RF port/RF Gnd has been determined to be >±500V HBM for this technology. By using L_{ESD} as an RF choke on a port, an ESD protection to ±8kV contact discharge can be achieved.

5. The large pad on the bottom of the package should be soldered to ground to assure proper performance of the device.

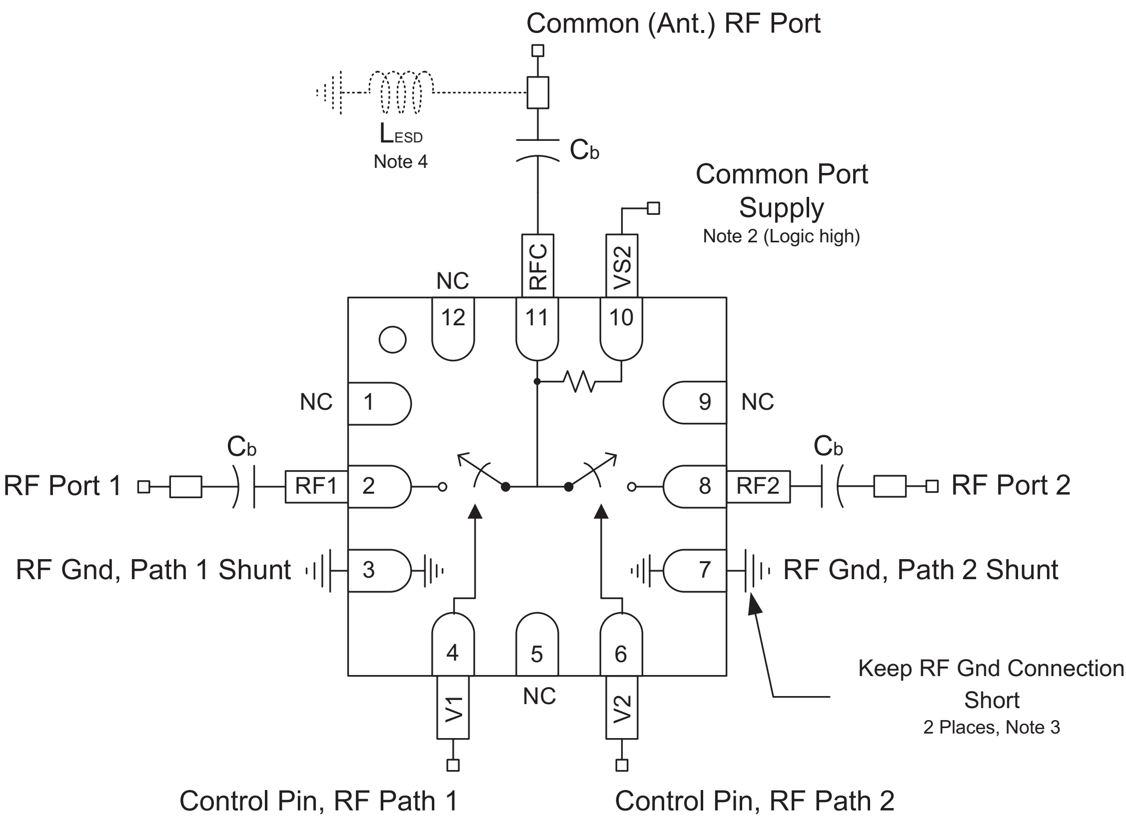
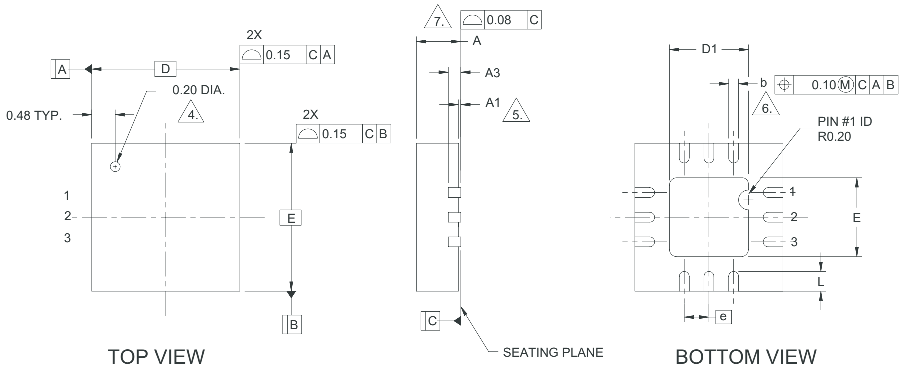


Figure 15: Packaged Device Application Schematic

PACKAGE OUTLINE



SYMBOL	DIMENSIONS-MM MIN.	NOM.	MAX.	NOTE	SYMBOL	DIMENSIONS-INCHES MIN.	NOM.	MAX.	NOTE
A	0.80	0.85	1.00		A	0.031	0.033	0.039	
A1	0.00	0.01	0.05		A1	0.000	0.0003	0.001	
A3		0.20 REF.			A3		0.008		
b	0.18	0.23	0.30		b	0.007	0.009	0.011	
D		3.00 BSC			D		0.118 BSC		
D1	1.45	1.60	1.75		D1	0.057	0.063	0.069	
E		3.00 BSC			E		0.118 BSC		
E1	1.45	1.60	1.75		E1	0.057	0.063	0.069	
e		0.50 BSC			e		0.019 BSC		
L	0.35	0.40	0.55		L	0.014	0.016	0.022	

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. APPLIED ONLY FOR TERMINALS
6. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING EXPOSED PART FROM MEASURING.
8. REFERENCE JEDEC OUTLINE MO-220.

Figure 16: S26 Package Outline - 12 Pin 3mm x 3mm MLF

NOTES

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWS5522D1	-30 °C to +85 °C	Die	(contact ANADIGICS for details)
AWS5522S26	-30 °C to +85 °C	12 Pin 3mm x 3mm MLF	Tape & Reel

ANADIGICS, Inc.
141 Mount Bethel Road
Warren, New Jersey 07059, U.S.A.
Tel: +1 (908) 668-5000
Fax: +1 (908) 668-5132

URL: http://www.anadigics.com
E-mail: Mktg@anadigics.com