AK4533 Audio Codec with Touch Screen Controller

Featues

[ADC]

- **1ch mono16-bit ADC (For Microphone)**
- **1st MIC Amplifier: 20dB Fixed Gain**
- **2nd Amplifier: from -8dB to +27.5dB (0.5dB step)**
- **AGC function**
- **Analog Performance:**
  - **S/N: 82dBA @ fs=44.1kHz, MIC_GAIN=20dB(AGC=off, 0dB)**

[Sampling Frequency]
Audio : from 8kHz to 44.1kHz

[DAC]

- **2ch(stereo) DAC**
- **Single End output**
- **Digital Attenuator**
- **Analog Performance**
  - **S/N: 88dBA@fs= 44.1kHz**

[Touch Screen/Battery Check]

- **SAR type A/D Converter: 12bit(10bit accuracy)**
  - **S/H circuit**
  - **4-1 Multiplex (2ch :Touch Screen, 2ch : Check for the battery)**

- **Low Power Current: 20mA**

- **Low Voltage Operation**
  - **Analog, Digital: 3.0V**

- **Small Package: 48pin LQFP**

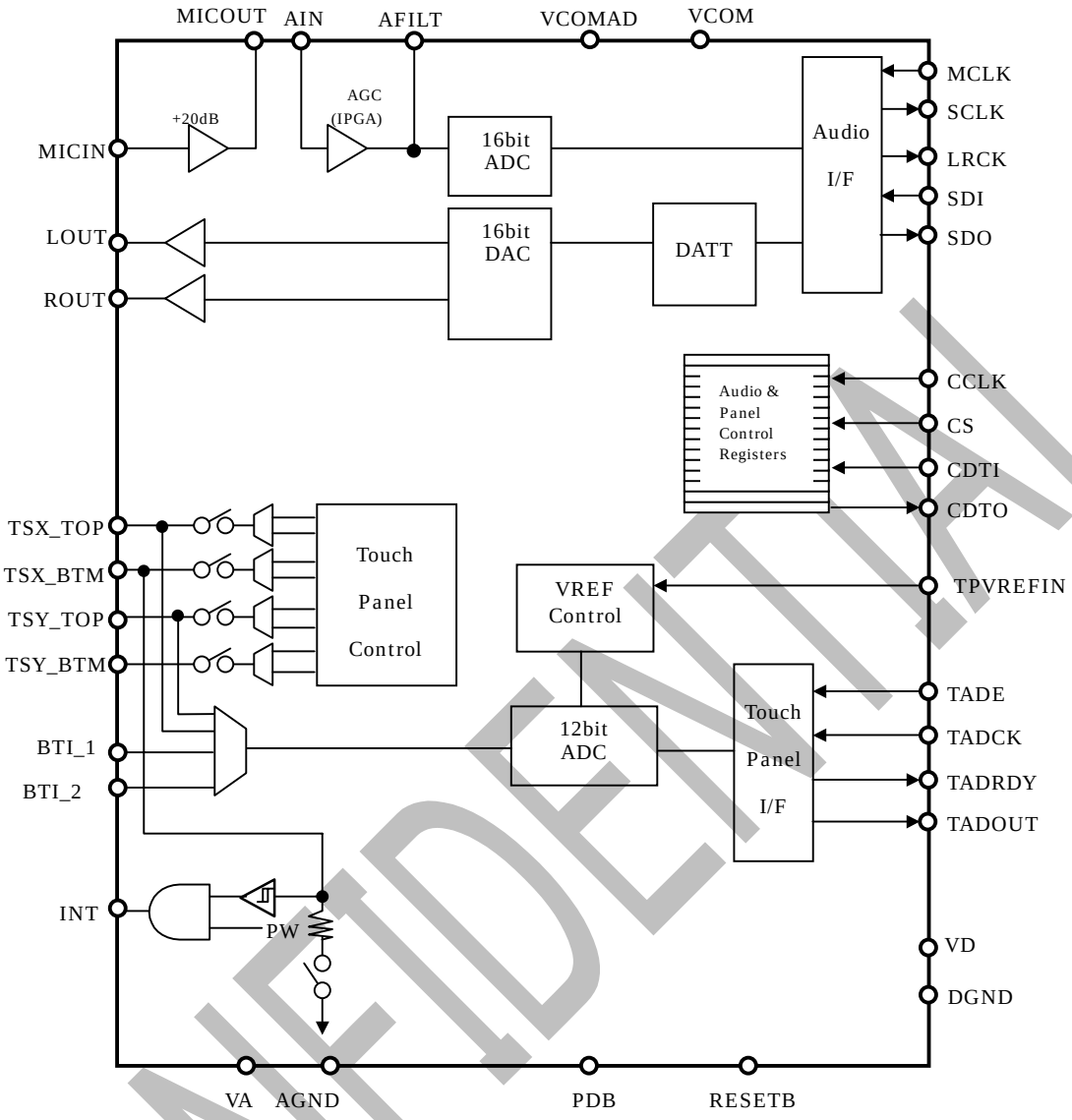
[General Description]

The AK4533 is audio codec with touch screen controller. The AK4533 incorporates several functions into one-chip; the position detection of the touch screen, the measurement of battery voltage, the record of the voice, and the playback of audio data.

The AK4533 has monaural A/D converter with AGC, and stereo D/A converter with digital attenuator. As codec can operate from 8kHz to 44.1kHz, the AK4533 can playback the sound like MP3 with high quality. On-chip digital attenuator with 1.5dB step can control DAC volume without the increase of CPU load. As AGC with 0.5dB step automatically controls voice input level to the appropriate level, the voice can be recorded clearly. As the AK4533 also has on-chip 20dB fixed gain preamplifier in addition to AGC, no other external preamplifier for microphone is required.

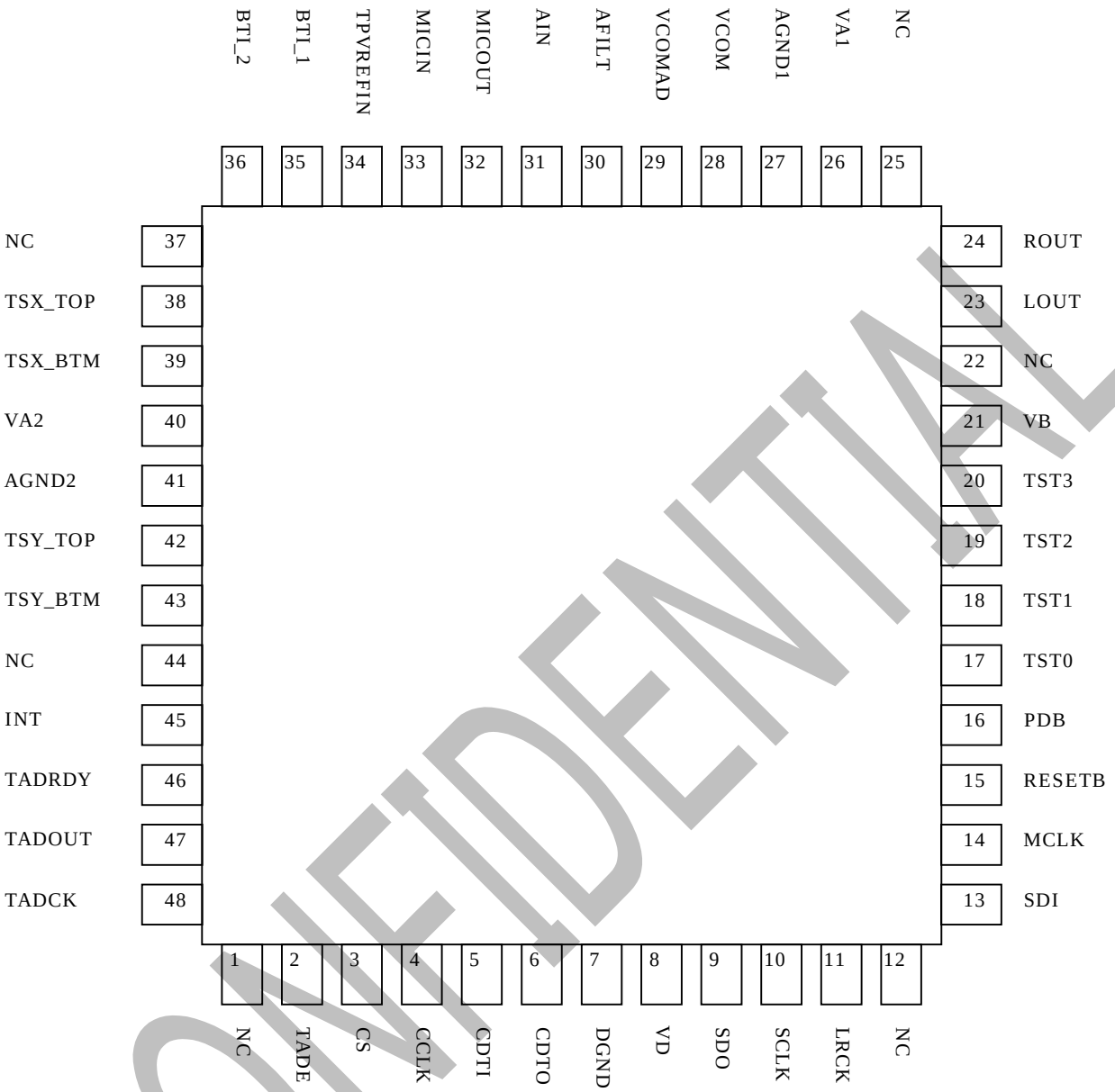
The AK4533 controls the voltages which are supplied to two pairs of electrode of touch screen. As the AK4533 also has 12bit/100kHz sampling SAR type A/D converter, it is possible to detect the pressed location by two A/D conversions. 12 bit digital code is output through serial interface. The AK4533 also has 2 analog channels as the input of Touch Screen A/D converter. The main purpose is for the measurement of the battery voltage.

As the AK4533 is small package, and can operate from 2.7V with low power consumption, it is suitable for mobile products, especially PDA.



BLOCK DIAGRAM

■Pin Configuration



PIN/FUNCTION

No.	Signal Name	I/O	Description
Power Supply			
7	DGND	-	Digital Ground
8	VD	-	Digital Power Supply : +3V
21	VB	-	Power Supply(Bulk) : +3V
26	VA1	-	Analog Power Supply : +3V
27	AGND1	-	Analog Ground
40	VA2	-	Analog Power Supply : +3V
41	AGND2	-	Analog Ground
Reset/Power Down			
15	RESETB	I	Reset Pin The device is powered down except for VCOM when this pin is “L”. All registers are cleared and are set to default values.
16	PDB	I	Power down Pin All blocks including VCOM are powered down when this pin is set to “L”.
Audio CODEC			
9	SDO	O	Audio ADC Serial Data Output
10	SCLK	O	Audio data Serial Output/Input Clock : 32fs The device outputs ADC data through SDO pin at the falling edge of SCLK clock. The device latches DAC (input) data through SDI pin at the rising edge of SCLK clock.
11	LRCK	O	Left/Right channel Select Clock, 1fs H: Left channel, L: Right channel When both of ADC block and DAC block go into power-down mode, this pin outputs “L”. Either of block is active, the device outputs LRCK clock.
13	SDI	I	Audio DAC Serial Data Input
14	MCLK	I	Master Clock Input 256fs or 512fs, which is selected by MSEL bit in the Control Register, master clock is input to this pin.
23	LOUT	O	DAC Left Channel Analog Output Note) Load resistance must be greater than 10KΩ. Load capacitance must be less than 50pF.
24	ROUT	O	DAC Right channel Analog Output Note) Load resistance must be greater than 10KΩ. Load capacitance must be less than 50pF.
28	VCOM	O	Analog Common Voltage Output Reference voltage of all analog circuit block (VA/2) Connect 4.7uF and 0.1uF capacitors
29	VCOMAD	O	Analog Common Voltage Output for ADC Reference voltage of ADC block Connect 4.7uF and 0.1uF capacitors
30	AFILT	I	Anti aliasing Filter for A/D Input Connect 1nF capacitor.
31	AIN	I	Analog Input Input inverting analog signal which is output from MICOUT pin 1uF capacitor is connected between MICOUT pin and AIN pin.
32	MICOUT	O	Microphone Analog Output Output inverting analog signal with 20dB gain of MICIN signal.
33	MICIN	I	Microphone Analog Input Input analog signal from microphone

No.	Signal Name	I/O	Description
Audio & Touch Panel Control I/F			
3	CS	I	Control Data Chip Select When read/write Touch Screen/Audio Control Data, set CS pin to “H”. Read/Write operation requires 16 CCLK cycles. CS pin must be set to “L” once per one Read/Write operation.
4	CCLK	I	Audio/Touch Screen Data Control Clock Input Clock signal used for Touch Screen/Audio control I/F.
5	CDTI	I	Touch Screen/Audio Control Data Input Control data is input to CDTI pin. The device latches data at the rising edge of CCLK.
6	CDTO	O	Touch Screen/Audio Control Data Output Control data is output through CDTO pin. The device outputs data at the falling edge of CCLK.
Touch Screen & watch Power-supply			
34	TPVREFIN	I	Touch Screen Reference Voltage Input The TPVREFIN voltage is referenced as full scale of Touch Screen A/D converter(TSADC) This pin should be connected to 4.7uF and 0.1uF capacitors. Note that maximum voltage is VA.
35	BTI_1	I	Battery level check Input_1 Note that maximum voltage is VA.
36	BTI_2	I	Battery level check Input_2 Note that maximum voltage is VA.
38	TSX_TOP	I/O	Touch Screen X_ TOP plate Voltage supply ■Measurement of the position on X axis: This pin supplies the voltage to the top side of the touch screen(normal mode -> VA, reverse mode -> AGND) ■ Measurement of the position on Y axis: The Input to Touch Screen A/D converter(TSADC) ■Powerdown Mode : OPEN ■Pen Waiting Mode: OPEN
39	TSX_BTM	I/O	Touch Screen X_ BOTTOM plate Voltage supply ■Measurement of the position on X axis: This pin supplies the voltage to the bottom side of the touch screen(normal mode -> AGND, reverse mode -> VA) ■ Measurement of the position on Y axis: OPEN ■Powerdown Mode : OPEN ■ Pen Waiting Mode: This pin is connected to AGND through the resister.
42	TSY_TOP	I/O	Touch Screen Y_ TOP plate Voltage supply ■Measurement of the position on Y axis: This pin supplies the voltage to the top side of the touch screen(normal mode -> VA, reverse mode -> AGND) ■ Measurement of the position on X axis: The Input to Touch Screen A/D converter(TSADC) ■Powerdown Mode : OPEN ■Pen Waiting Mode: OPEN
43	TSY_BTM	I/O	Touch Screen Y_ BOTTOM plate Voltage supply ■Measurement of the position on Y axis: This pin supplies the voltage to the bottom side of the touch screen(normal mode -> AGND, reverse mode -> VA) ■ Measurement of the position on X axis: OPEN ■Powerdown Mode : OPEN ■ Pen Waiting Mode: Supplies VA.

No.	Signal Name	I/O	Description
2	TADE	I	Touch Panel A/D Data Chip Enable Pin This pin enables the output of Touch Screen A/D converter when it goes to "H". ADC starts tracking at the rising edge. A/D Conversion and the output require 16 TADCK clock cycles. This pin should be set to "L" once per one A/D conversion.
45	INT	O	Interrupt This pin is "H" ONLY when the touch screen is pressed. In other cases, the pin is "L".
46	TADRDY	O	Touch Screen A/D data Output Ready When Touch Screen A/D converter is ready to output data, TADRDY pin goes to "H". This pin goes back to "L" after 12 bit data is output.
47	TADOUT	O	Touch Screen A/D Data Output MSB of A/D data is output at the rising edge of TADRDY is "H". Other bits of data are output at the falling edge of TADCK clock
48	TADCK	I	Touch Panel ADC Clock This clock is used for A/D conversion and for the output of data One A/D conversion needs 16 TADCK clock cycle.
Miscellaneous			
17	TST0	-	Test pin 0 Should be Connected to DGND.
18	TST1	-	Test pin 1 Should be Connected to DGND.
19	TST2	-	Test pin 2 Should be Connected to DGND.
20	TST3	-	Test pin 3 Should be Connected to DGND.
1	NC	-	Non Connection
12	NC	-	Non Connection
22	NC	-	Non Connection
25	NC	-	Non Connection
37	NC	-	Non Connection
44	NC	-	Non Connection

ABSOLUTE MAXIMUM RATINGS

AGND, DGND=0V

Parameter	Symbol	Min	max	Units
Power Supplies				
Analog	VA	-0.3	6.0	V
Digital	VD	-0.3	6.0(VA+0.3)	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Analog Input Voltage Note2)	VINA	-0.3	6.0(VA+0.3)	V
Digital Input Voltage Note2)	VIND	-0.3	6.0(VA+0.3)	V
Touch Panel Drive Current	IOUTDRV		50	mA
Ambient Temperature	Ta	-10	70	°C

All voltages with respect to ground.

RECOMMENDED OPERATING CONDITIONS

AGND, DGND=0V

Parameter	Symbol	min	typ	max	Units
Power Supplies					
Analog	VA	2.7	3.0	3.63	V
Digital	VD	2.7	3.0	VA	V

All voltages with respect to ground.

ANALOG CHARACTERISTICS

Ta=25°C, AVdd=DVdd=3.0V, signal=1kHz, Sampling Frequency : Fs=44.1kHz Measurement frequency=20 ~ 20kHz unless otherwise specified

Parameter	min	typ	Max	Units
Mono(1ch) ADC				
Resolution			16	Bits
S/N (A weighting) @ MIC gain=20dB, IPGA=0dB		82		dBA
S/(N+D) @ MIC gain=20dB, IPGA=0dB, Ain= - 1dBFS		77		dB
Input voltage Range @ MIC gain=20dB, IPGA=0dB		0.06*VA		Vp-p
MIC Amplifier				
Input Impedance		30		kΩ
Gain(Fixed)		20		dB
AGC(IPGA)				
Step Size		0.5		dB
Gain Control Range	-8		27.5	dB
Stereo(2ch)DAC:				
Resolution			16	Bits
S/N (A weighting) @fs=44.1kHz, Fin=1kHz, noise band=20kHz, 256fs_mode (Reference) @fs=8kHz, fin=1kHz, noise band=20kHz, 512fs_mode		 88 84		 dBA dBA
S/(N+D) @fs=44.1kHz, Fin=1kHz, noise band=20kHz, 256fs_mode		84		dB
Output Voltage		0.6*VA		Vp-p
Voltage Reference (Audio)				
VCOM,VCOMAD		0.5*VA		V
ADC for Touch Panel				
Resolution			12	Bits
Integral Linearity Error @100kHz @ External Rin=500Ω, FS=3V(TP mode)		1.5		LSB
Differential Linearity Error @100kHz @ External Rin=500Ω, FS=3V(TP mode)		1		LSB
Touch Panel Driver (ADC mode) ON- Resistance (Top side) @VA=3V, RL=300Ω ON- Resistance (Bottom side) @VA=3V, RL=300Ω (Reference) Drive Current @VA=3V, RL=300Ω		 10 10 10		 Ω Ω mA
Touch Panel Driver (Pen waiting State) Pull down Resistance for TSX_Bottom		 20		 kΩ
TPVREFIN (VRIN)	2.5		VA	V
Power Supply Current (VA+VD)				
Total Power ON (exclude TP_Drive current) Audio ADC + GAMP +IPGA (exclude VCOM) Audio DAC (2channel) (exclude VCOM) Touch Panel ADC (exclude TP_Drive current, VCOM) VCOM (RESTB=L) Touch Panel Driver Current @VA=3V, RL=300Ω		20 9 9 1.2 0.37 10		mA mA mA mA mA mA
Full Power Down (PDB=L)		3		uA

FILTER CHARACTERISTICS

Ta=25°C,AVdd=DVdd=3.0V, Signal=1kHz, fs=44.1kHz

Parameter	Symbol	min	Typ	max	Units
ADC Digital Filter (LPF)					
Pass band ±0.2dB	PB	0		17.64	kHz
Stop band	SB	26.46		2795.94	kHz
Stop band Attenuation	SA	70			dB
Absolute Delay (Note 1)			16.1		1/fs
ADC Digital Filter (HPF)					
Frequency Response	FR				
-3dB			6.89		Hz
-0.5dB			19.3		Hz
-0.1dB			45.0		Hz
DAC Digital Filter					
Pass band ±0.2dB	PB	0		17.64	kHz
Stop band	SB	26.46		326.34	kHz
Stop band Attenuation	SA	70			dB
Absolute Delay (No te 1)			14.8		1/fs
DAC Digital Filter + Analog Filter					
Frequency Response 0 ~ 17.64kHz	FR		±1.0		dB

Note 1: Absolute delay time caused by digital filter only (not including analog delta sigma, digital delta sigma, and analog post filter.)
ADC DF: to the LRCK rising edge before data is output.
DAC DF: from the next LRCK rising edge after both channel data is set.

DC CHARACTERISTICS (Logic I/O)

Ta=25°C,VA=VD=3.0V

Parameter	Symbol	min	Typ	max	Units
“H” level input voltage	VIH	0.7xVD	-		V
“L” level input voltage	VIL		-	0.3xVD	V
“H” level output voltage (@ Iout = -400uA)	VOH	VD-0.4	-		V
“L” level output voltage (@ Iout= 400uA)	VOL	-	-	0.4	V

SWITCHING CHARACHTERISTICS

Ta= -10°C ~ 70°C, AVdd=DVdd=2.7V ~ 3.63V, CL=20pF

Parameter	Symbol	min	Typ	max	Units
Audio					
Master Clock Timing					
MCLK_SEL="L" (512fs mode)	fMCLK	4.096		11.2896	MHz
MCLK_SEL="H" (256fs mode)	fMCLK	5.6448		11.2896	MHz
Pulse Width duty	duty_MCLK	40	50	60	%
LRCK Frequency	fs				
MCLK_SEL="L" (fMCLK/512)		8		22.05	kHz
MCLK_SEL="H" (fMCLK/256)		22.05		44.1	kHz
LRCK duty	duty_LRCK	-	50	-	%
Serial Interface Timing					
SCLK Frequency	fSCLK	-	32	-	fs
SCLK duty	duty_SCLK	40	50	60	%
SDI Hold Time after "SCLK rising"	tSD_H	100	-	-	ns
SDI Setup Time for "SCLK rising"	tSD_S	100			ns
SDO(MSB) delay from "LRCK rising"	tLR_SDO			150	ns
SDO delay from "SCLK falling"	tSC_SDO			150	ns
LRCK change to "SCLK falling"	tLR_SCF	-40		40	ns
Control Interface Timing					
CCLK Period	tCCK	500		2000	ns
CCLK Pulse Width Low	tCCKL	200		-	ns
CCLK Pulse Width High	tCCKH	200			ns
CDTI Hold Time after "CCLK rising"	tCDH	100			ns
CDTI Setup Time for "CCLK rising"	tCDS	100			ns
CS Low Level Time (for next command)	tCSW	200			ns
"CS rising" to "CCLK rising" time	tCSS	200			ns
"CCLK falling" to "CS falling" time	tCSH	0(TBD)			ns
CDTO delay from "CCLK falling"	tDCD	0		100	ns
16CCLK ↓ to CDTO ="L"	tCCL			100	ns
Touch Panel (A/D Converter)					
Conversion Rate				125	kHz
TADCK					
frequency	fTADCK	0.1		2	MHz
duty	duty_TADCK	45	50	55	%
TADE					
"H" Level Period		16			cycle
Setup Time for "TADCLK rising"	tTADES	225			ns
Hold Time after "TADCLK rising"	tTADEH	225			ns
"L" Level Time for next Conversion	tTADE_LW	200			ns
Tracking Time	tTRK	1.5			us
TADOUT delay time from TADCLK ↓	tTADD			150	ns
TADRDY					
"H" Level Period		-	12	-	cycle
TADCK ↓ to TADRDY change	tRDYD			50	ns
Others					
PDB Low Pulse Width	tPDB	200			ns
RESETB Low Pulse Width	tRESETB	200			ns
Input signal Rise/fall time (VIL to VIH) (CS,CCLK,TADE,TADCK, MCLK)				15	ns

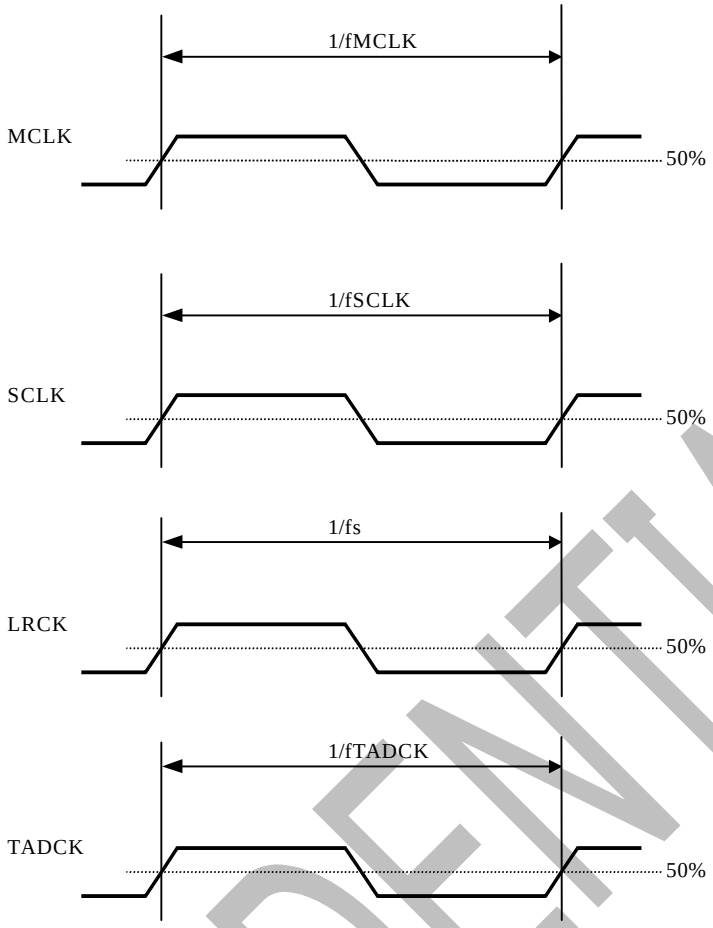


Figure 1. Clock Timing

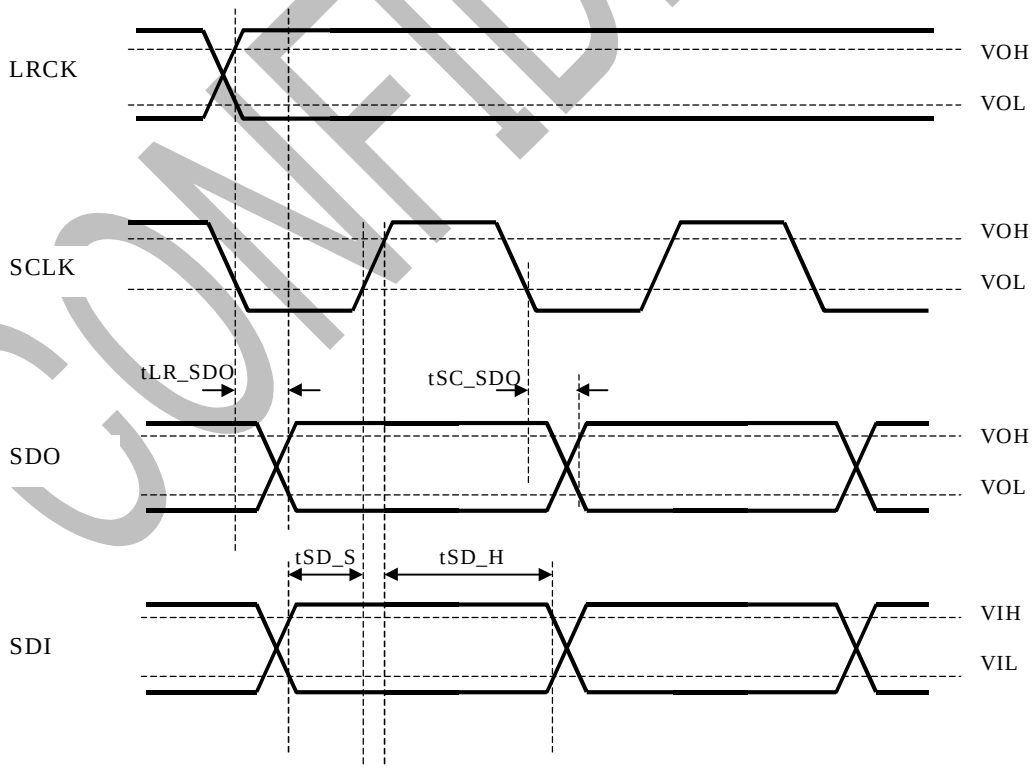


Figure 2. Audio Stream Data Interface Timing

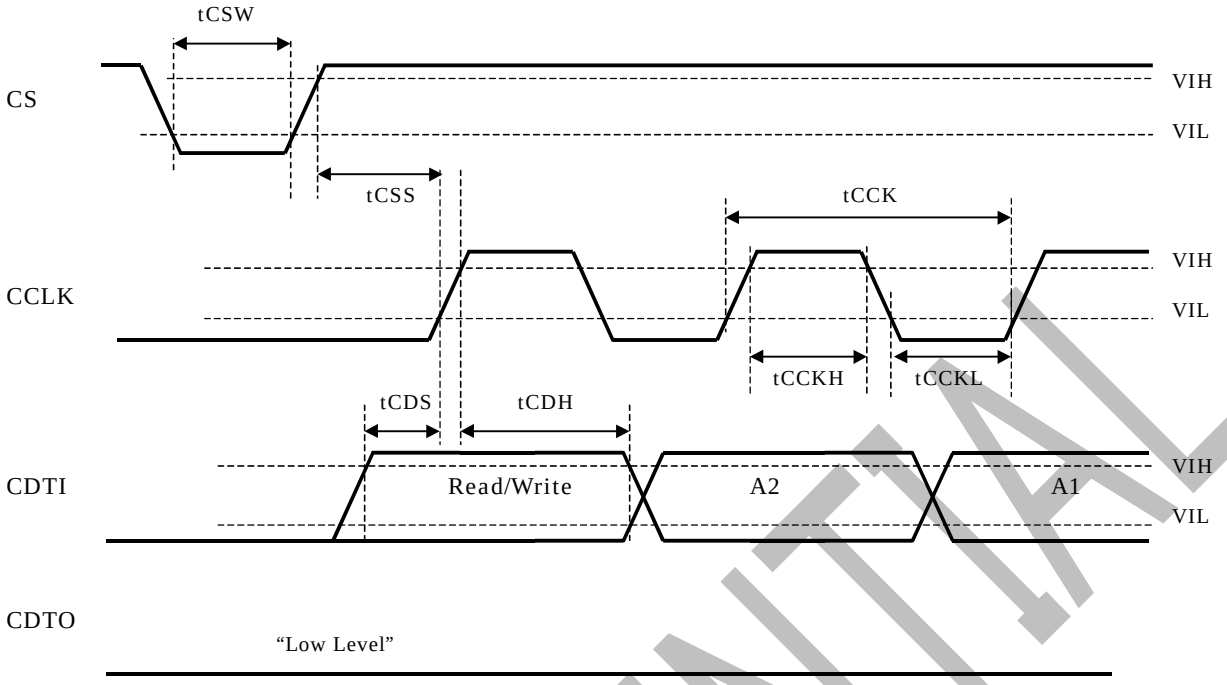


Figure 3. Control Data Interface Timing (Read/Write)

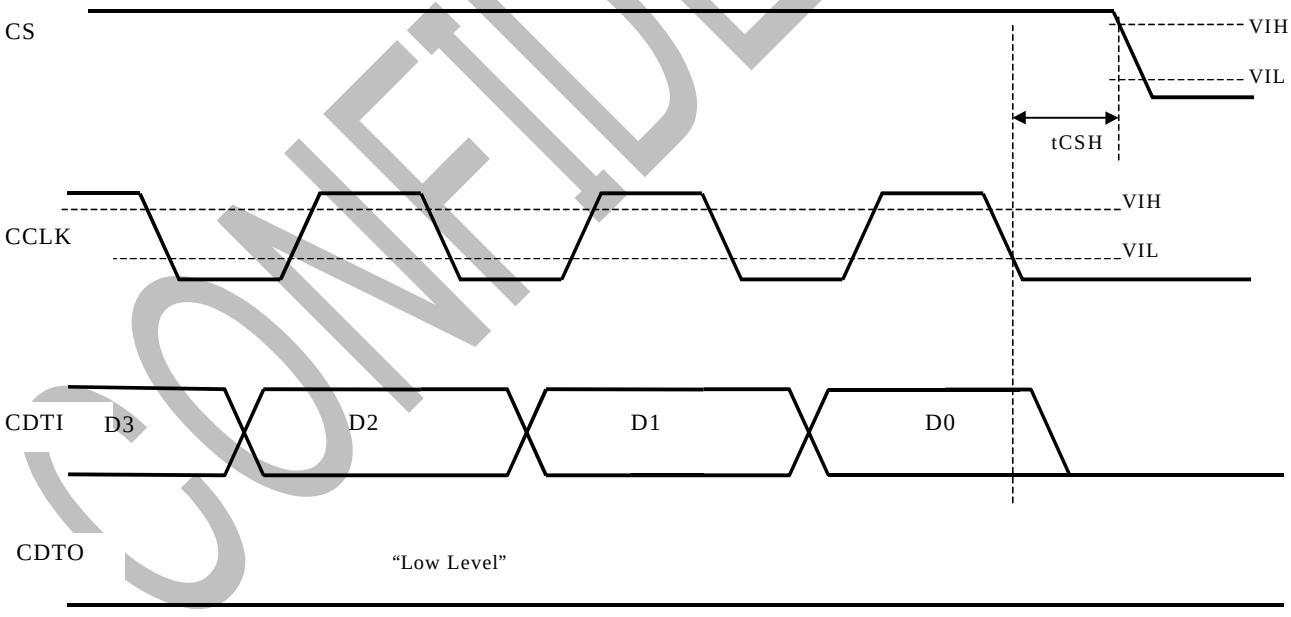


Figure 4. Control Data Interface Timing (Write Timing)

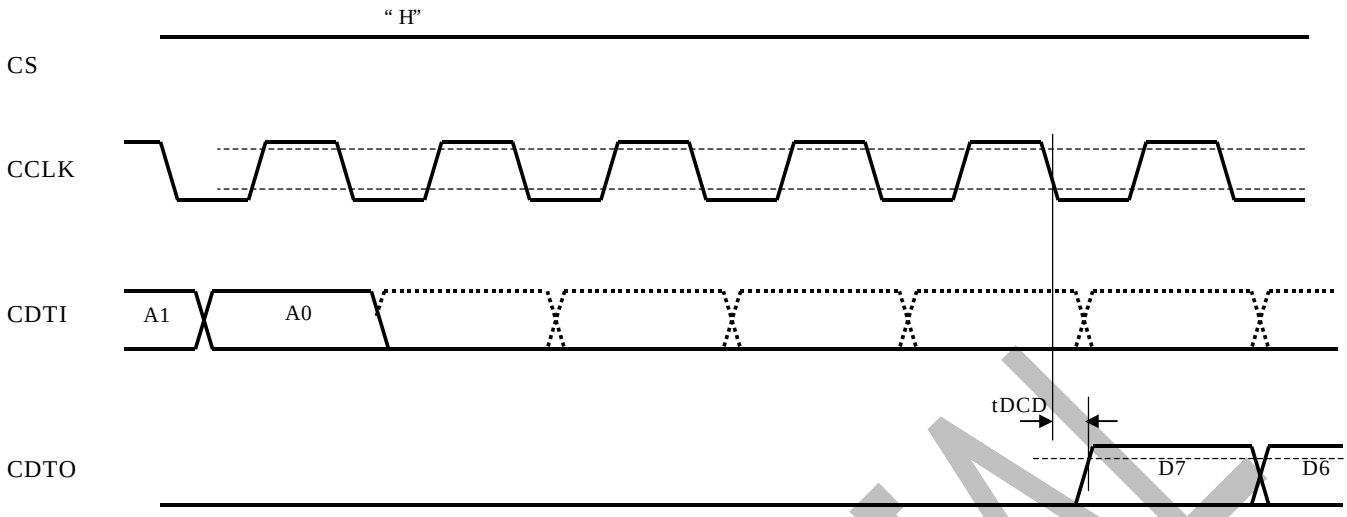


Figure 5. Control Data Interface Timing (Read Timing <1>)

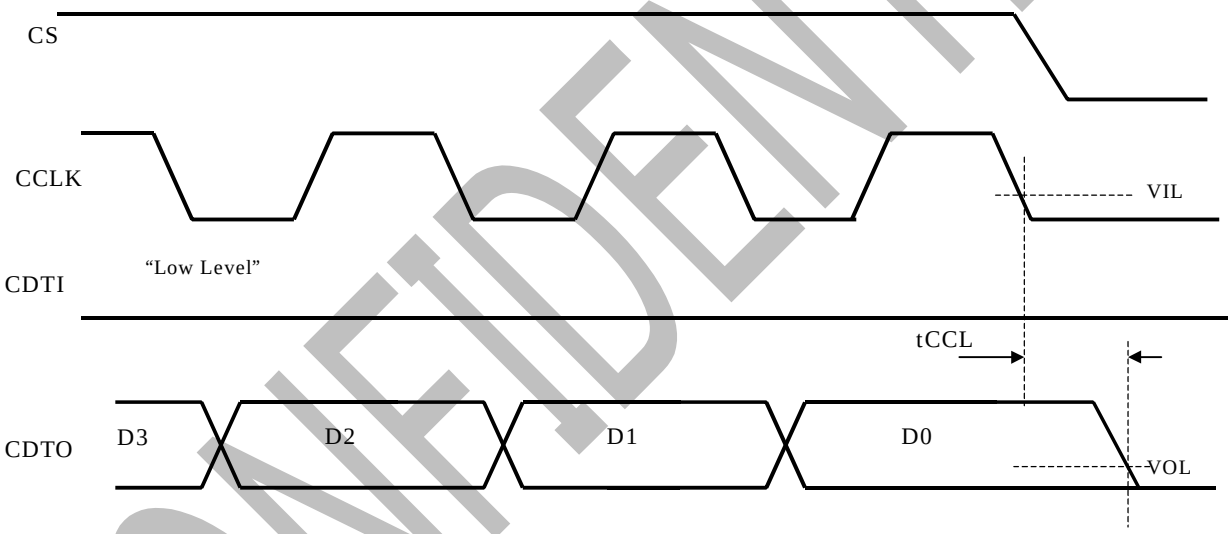


Figure 6. Control Data Interface Timing (Read Timing <2>)

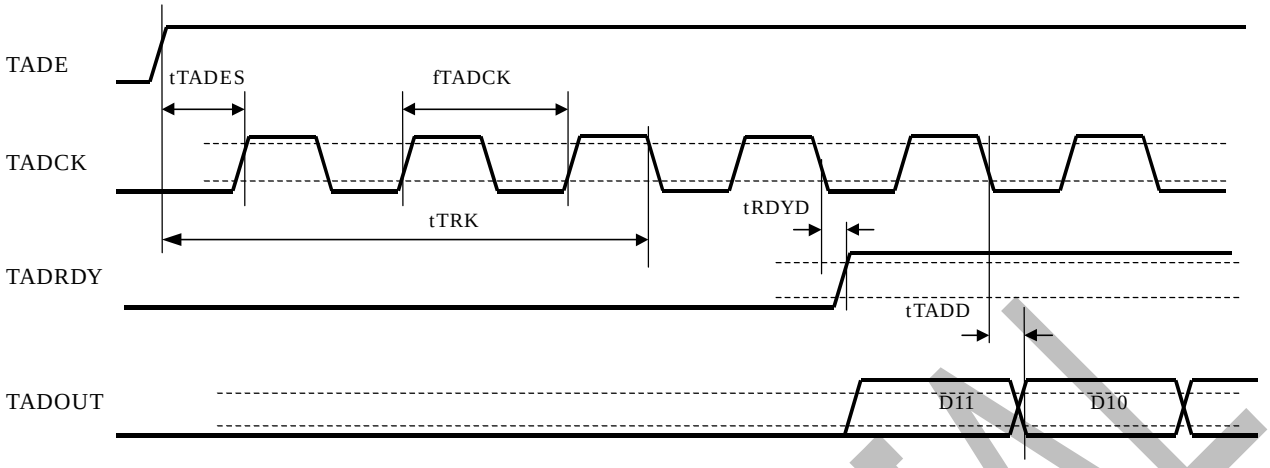


Figure 7. Touch Screen A/D Interface Timing <1>

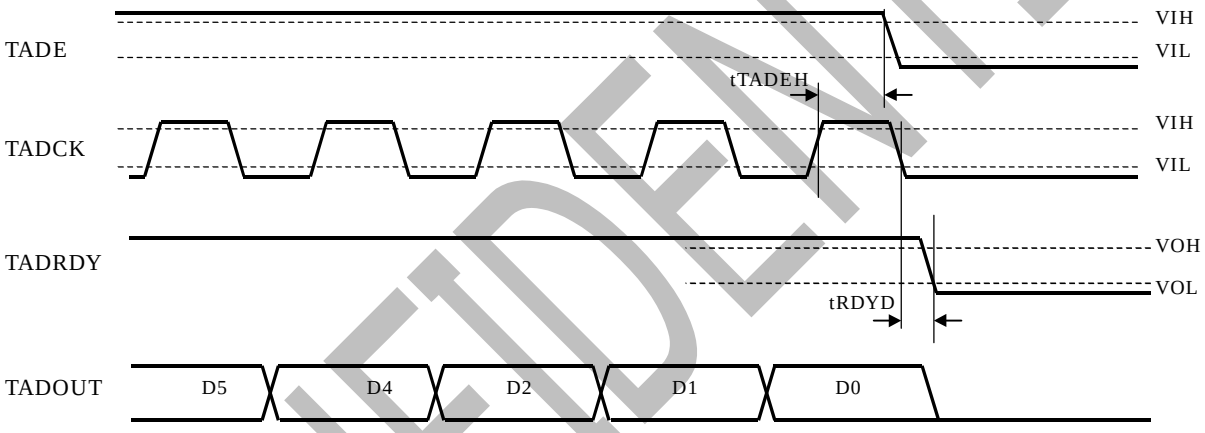


Figure 8. Touch Screen A/D Interface Timing <2>

Overview

The AK4533 consists of three blocks; Audio A/D Converter, Audio D/A Converter, and Touch Screen A/D Converter. These blocks operate independently. The following describes the overview of the device.

(1) 1 channel 16 bit audio A/D converter:
- 64fs oversampling Δ-Σ type
- On-chip decimation LPF and digital HPF
- Audio Format: 2's complement, MSB first, serial output
- Fixed Gain Amplifier for microphone input: +20dB
- Input Programmable Gain Amplifier (IPGA) with automatic gain control (AGC) function
  -8dB to +20dB, 0.5dB/step
- Input signal range of ADC scales with the supply voltage: 0.6 x VA (excluding fixed gain amplifier)
- Power down control independent with DAC block and Touch panel block

(2) 2 channel 16 bit audio D/A converter:
- 128fs/256fs oversampling Δ-Σ type
- 8 times interpolation digital filter
- 2nd order SCF: single-ended
- Audio format: 2's complement, MSB first, serial input
- Digital ATT: 0dB to -22.5dB, 1.5dB/step
- Output signal range of DAC scales with the supply voltage: 0.6 x VA
- Power down control independent with L channel and R channel

(3) 1ch 12bit A/D converter for Touch Screen and Battery Measurement
- 12bit Resolution, Successive Approximation Resistor (SAR) type
- Two pairs of touch screen driver: X-axis and Y-axis
  - Measurement of X-axis position: TSY_TOP pin is automatically selected.
  - Measurement of Y-axis position: TSX_TOP pin is automatically selected.
- Power Down Mode
  - A/D converter goes to power down state
  - Touch Screen Driver is open state.
- Waiting State for Pen Interrupt
  - TSY_BTM is connected to VA, and TSY_TOP is open state
  - TSX_TOP is open state, and TSX_BTM is connected to AGND through internal resistor. When the touch screen is pressed, the device outputs INT signal.
- Measurement of Battery Voltage
  - 2ch BTI inputs
  - Full scale of BTI input is TPVREFIN

(4) Control Registers
- 4-wire I/F: 8bit/word, 8words
- The registers are set to default value by RESETB pin ("L" level)
- This interface is used for IPGA (AGC), PD control, mode selection of Touch Screen

(5) Pin Control
- PDB pin
  - When PDB pin is "L", all blocks in the device ***including*** VCOM buffer goes to power-down state.
  - Internal registers are set to default value.
  - ADC for Touch Screen is power-down state (Pen Interrupt function is disabled).
  - All digital output pins is "L".
  - When PDB pin goes to "H", power-down state is cleared, and the device is ready to normal operation.
  - VCOM buffer start to operation after exiting power-down state.
  - It takes time for VCOM to settle the appropriate voltage through external capacitor. (4ms@4.7uF)
- RESETB pin
  - All blocks in the device ***except for VCOM Buffer*** is power-down state when RESETB pin is "L".
  - When RESETB pin is "L", internal registers are set to default value.
  - ADC for Touch Screen is power-down state (Pen Interrupt function is disabled).
  - All digital output pin is "L", and A/T I/F is NOT available when RESETB is "L".

Audio Block Diagram

Figure 9 shows audio codec block diagram

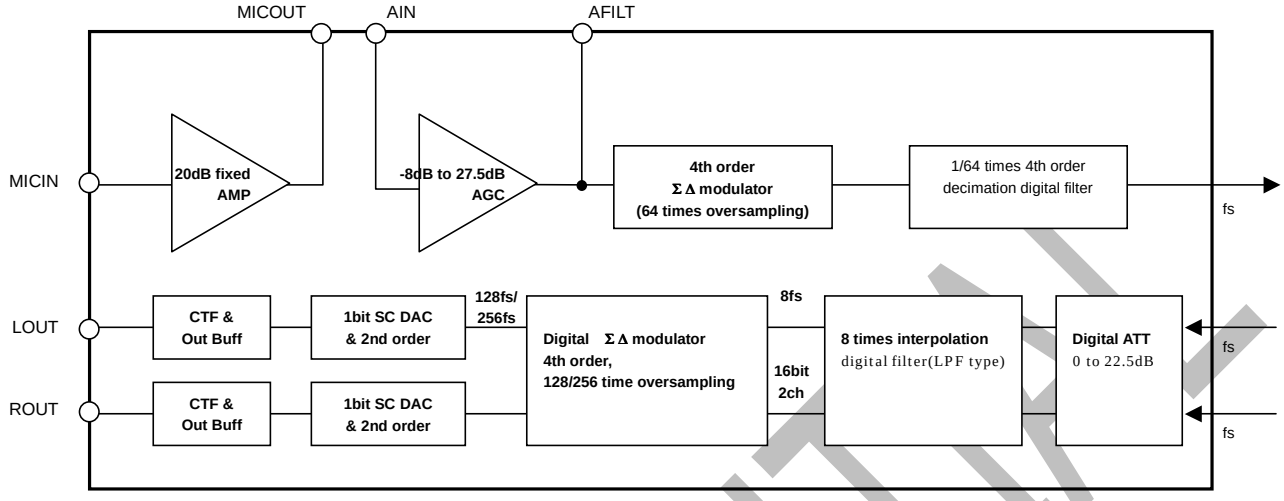


Figure 9. Audio Codec Block Diagram

General Description

■ Input/Output Interface

The AK4533 has the following three I/O interface:

(1) Audio Streaming Interface (AS I/F)
AS I/F is used to transport audio streams (A/D data and D/A data). 5-wire are used for AS I/F; MCLK, SCLK , LRCK, SDO, and SDI

(2) Audio/Touch Screen Control Interface (A/T I/F)
A/T I/F is used to access internal registers for controlling audio function such as volume control or touch screen function. 4-wire are used for A/T I/F; CCLK, CS, CDTO, and CDTI

(3) Touch Screen Interface (TS I/F)
TS I/F is used to transmit A/D data that is output from 12bit Touch Screen A/D converter. 4-wire are used for TS I/F; TADE, TADCK, TADRDY, and TADOUT.

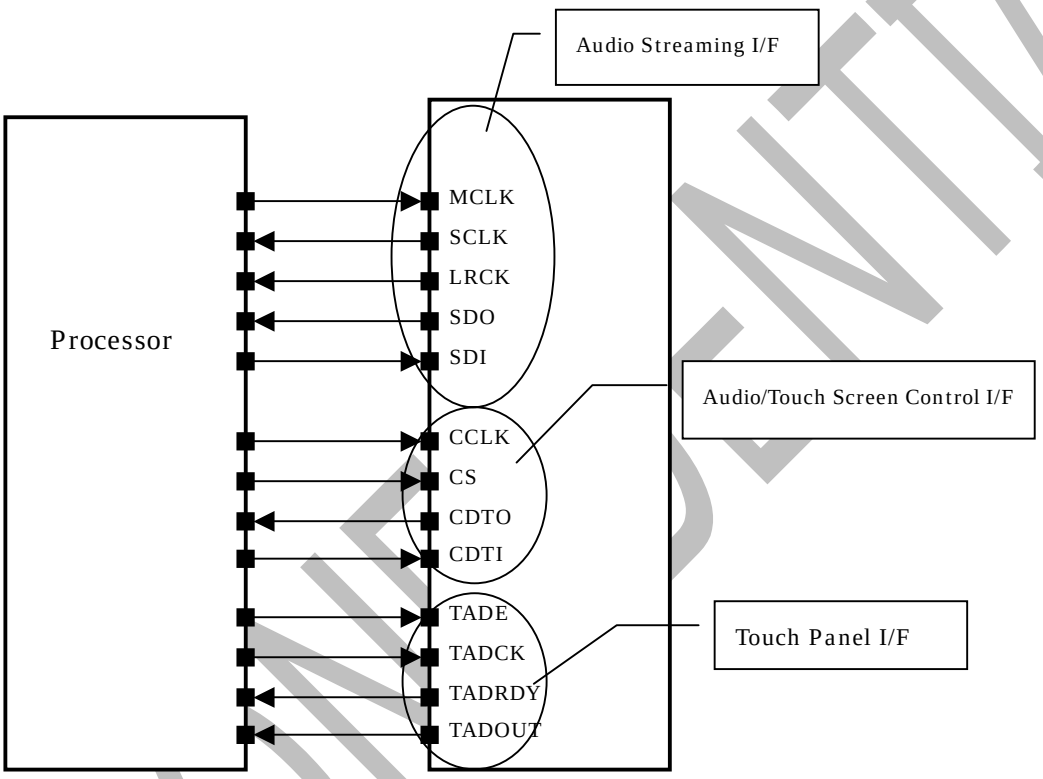


Figure 10. AK4533 Three Interfaces

(a) Audio Streaming I/F (AS I/F)

Audio data is transported by the control of 5-wire; MCLK, SCLK, LRCK, SDO, and SDI.

256fs or 512fs clock is input to MCLK pin as master clock for audio codec. The write the appropriate value to MSEL bit in the register 0h through A/T I/F is needed before master clock is input to the device. If the sampling frequency (fs) is equal to or less than 22.05kHz, MSEL bit should be set to "0", which selects 512fs mode to suppress out-band noise. If fs is more than 22.05kHz, MSEL bit must be set to "1", which select 256fs mode.
Note that MSEL bit should be set under power-down state (ADPD = "1", DALPD="1", DARPD="1")

Bit clock is 32fs that is synchronized to master clock, and is output via SCLK pin. Audio frame signal is also output via LRCK pin, and its frequency is fs. The device keeps LRCK signal high level for 1/2fs period in which left channel data is input to or output from the device, and keeps LRCK signal low level for 1/2fs period in which right channel data is input to the device. If at least one of ADPD bit, DALPD bit, or DARPD bit is "0", LRCK signal and SCLK signal are output from the device. If all of the above bits are "1", SCLK and LRCK are fixed to "L" level.

A/D data is 1 channel, and is output via SDO pin while LRCK is "H". A/D data format is 2's complement, 16 bit, and MSB first. SDO is "L" while LRCK is "L". As A/D data is output at the falling edge of SCLK, A/D data should be latched at the rising edge of SCLK.

Left channel D/A data and right channel D/A data should be input in the first half of Ts and in the second half of Ts respectively. The device latches D/A data at the rising edge of SCLK, D/A data must be input to SDI pin at the falling edge of SCLK. D/A data format is 2's complement, 16 bit, and MSB first.

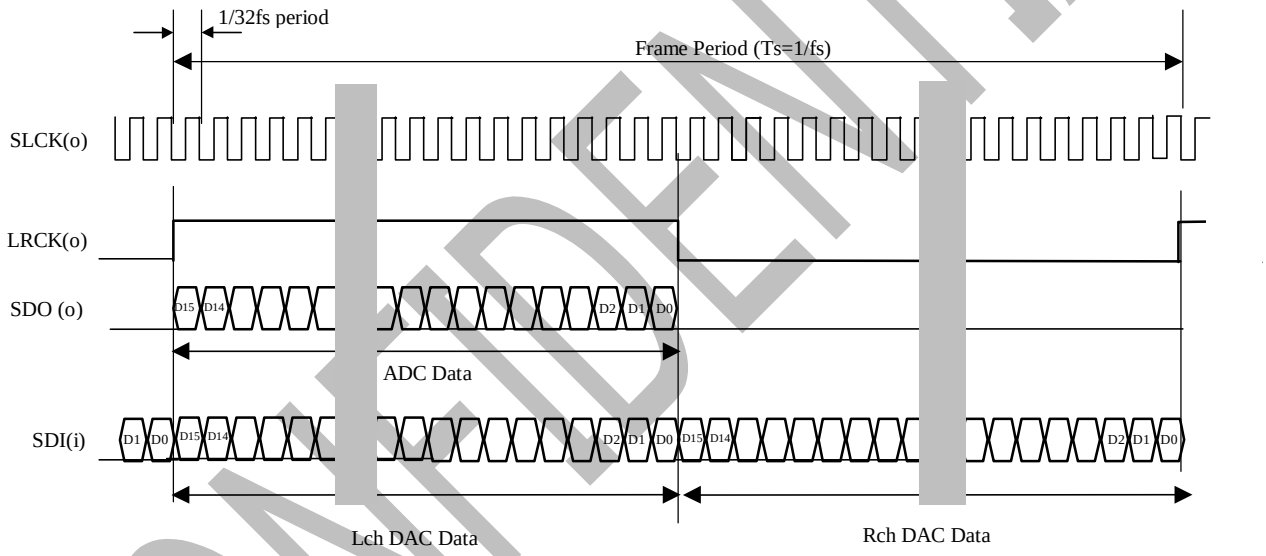


Figure 11. Audio Streaming Data Timing

Table 1 shows the relationship between Sampling frequency (fs) and master clock frequency.

Sampling Frequency (fs)	44.1kHz	22.05kHz	11.025kHz	8.0kHz
MSEL bit	“1”(256fs mode)	“0”(512fs mode)	“0”(512fs mode)	“0”(512fs mode)
MCLK	11.2896MHz	11.2896MHz	5.6448MHz	4.096MHz
SCLK (32fs)	1.4112MHz	705.6kHz	352.8kHz	256kHz
LRCK (1fs)	44.1kHz	22.05kHz	11.025kHz	8.0kHz

Table 1. The relationship between sampling frequency and master clock frequency

(b) Audio/Touch Screen Control Interface(A/T I/F)

The AK4533 incorporates 4 pin (CCLK, CS, CDTO, and CDTI) digital serial interface that links it to the external controller. This interface is used to access to the internal register. T/C I/F protocol has 16 bit field, and consists of three groups; one write/read bit, three address bits, and eight control bits. Data format is MSB first.

■ Write to the register
A/T interface is enabled by the CS pin = "H". In this mode, internal registers may be either written to or read from 4-wire uP interface. The device can recognizes the write request by the first bit = "1". Address and data is also clocked in via CDTI pin at the rising edge of CCLK. For write operation the control data is latched at the rising edge of 16th CCLK, after high-to-low transition. When more than 16 CCLK is input, the device ignores the CCLK. CS can be returned to "L" at the same time of 16th falling edge of CCLK. CS pin should be "L" once after the write cycle terminates.

For read operation, the device can recognizes the read request by the first bit = "0". Address is clocked in via CDTI pin at the rising edge of CCLK. The AK4533 outputs the addressed value via CDTO pin from the 8th falling edge of CCLK. At the 16th falling edge of CCLK, CDTO outputs "L". When more than 16 CCLK is input, CDTO still outputs "L". CS can be returned to "L" at the same time of 16th falling edge of CCLK. CS pin should be "L" once after the write cycle terminates.

CCLK, CS, and CDTI should be "L" while the device is idle state. CDTO is "L" under idle state.
("Idle state" means that the read/write operation is NOT executed)

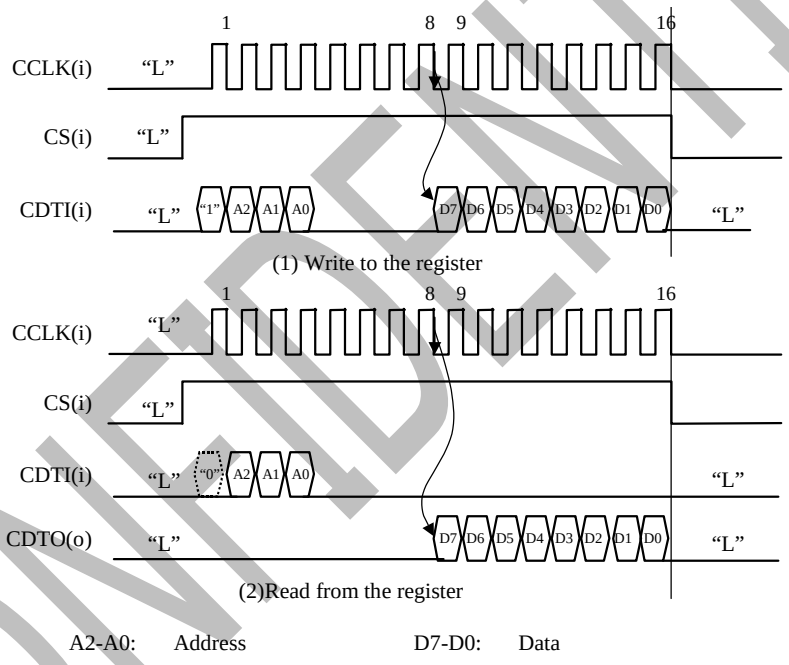


Figure 12. Audio/Touch Screen Control Interface Timing

Table 2 shows the control registers. (See " ■Touch Screen Control Register " for the detail of 07h register)
Note that MCLK should be present when a register is accessed.

Addr		D7	D6	D5	D4	D3	D2	D1	D0	Default
00	AGC Control	AGC	X	X	X	X	X	TH1	TH0	03
01	Limit/Recovery Control	LSTEP1	LSTEP0	X	X	RSTEP1	RSTEP0	RWT1	RWT0	01
02	IPGA Control	X	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0	10
03	Recovery Reference Level	X	REF6	REF5	REF4	REF3	REF2	REF1	REF0	36
04	DATT Control	Mute	X	X	X	M3	M2	M1	M0	00
05	Audio Powerdown & Clock Control	MSEL	X	X	X	X	DARPD	DALPD	ADPD	07
06	Reserve	X	X	X	X	X	X	X	X	00
07	Touch Screen Control	TSPD	PW	X	X	D3	D2	D1	D0	80

(The value of the registers is cleared and is set to default value when PDB pin or RESETB is set to "L".)

Table 2. The AK4533 Register Map

AGC Control
When AGC bit is set to "0", AGC operation is inhibited. IPGA can be changed by writing to IPGA Control Register directly if AGC bit is "0". When AGC bit is set to "1", AGC function is activated.
Before AGC operation, related registers, 00h - 03h, and MSEL (05h), should be set to appropriate value. (TH1/TH0 bits and AGC bit can be set at the same time.)
Note that MSEL bit must be changed under power-down state (D0, D1, and D2 is set to "1")
When AGC operation starts, the AK4533 uses the value of IPGA Control Register as initial value. After that, IPGA value is updated automatically. When the read of 02h register is executed, the AK4533 outputs the value which is updated by AGC circuit. Note that the value is not the same as the value that was stored at the start of AGC operation. The write operation to 02h register is ignored.

When ADC is set to power-down mode (ADPD="1"), 00h - 03h registers are set to default values. After power-down mode is cleared (ADPD = "0"), the write to the register is enabled. The period (516Ts@ MSEL="1", 260TS@MSEL="0") is required until VREFAD is stable. The write to the registers is possible in this initial period, but AGC function is disabled for this period. The AK4533 initiates AGC operation automatically after the end of the period.

Addr = 00h AGC: AGC Operation Enable
(0: Disable 1: Enable)
"1": AGC Operation "0": Gain can be changed directly through A/T I/F

■ **Overview of AGC operation**

The AK4533 detects and compares the analog input level of ADC per 64fs. The AK4533 has three zones for AGC operation; Limit Zone, Recovery Zone, and Insensitive Zone. At first, AGC circuit detects the zone in which the signal level is, and detects how long the signal is in that zone.

If the signal level enters in Limit Zone that is specified by TH0 bit and TH1 bit, AGC automatically decreases IPGA value per the step that is specified by LSTEP0 bit and LSTEP1 bit to suppress the signal.

If the signal is in Recovery Zone in the period that is called as "Recovery Time", AGC automatically increases IPGA value per the step that is specified by RSTEP0 bit and RSTEP1 bi to amplify the signal. Recovery Time is specified by RWT0 bit, RWT1 bit and MSEL bit.

If the signal level is in Insensitive Zone, which is named for the area between Limit Zone and Recovery Zone, AGC does nothing, and Recovery Counter is cleared.

Reference level of Limit Zone and Recovery Zone can be changed by the combination of TH0 bit and TH1 bit as Table 3.

Addr = 00h TH1-0: AGC Level

	TH1	TH0	The Range of Limit Zone	The Range of Recovery Zone	Senseless Zone
	0	0	ADC_INPUT ≥-8.0dBFS	ADC_INPUT ≤ -10.0dBFS	-8.0dBFS > ADC_INPUT > -10.0dBFS
	0	1	ADC_INPUT ≥-6.0dBFS	ADC_INPUT ≤ -8.0dBFS	-6.0dBFS > ADC_INPUT > -8dBFS
	1	0	ADC_INPUT ≥-4.0dBFS	ADC_INPUT ≤ -6.0dBFS	-4.0dBFS > ADC_INPUT > -6dBFS
default	1	1	ADC_INPUT ≥-2.0dBFS	ADC_INPUT ≤ -4.0dBFS	-2.0dBFS > ADC_INPUT > -4.0dBFS

Table 3. Setting of Limit/Recovery Zone

■**Limit Operation**

When signal enters Limit Zone, IPGA value is actually updated when the signal crosses the signal ground. As the special case, if the signal doesn't cross the ground within the timeout period that is specified by the Table 4 although the input signal entered Limit Zone once, the AK4533 forces to decrease IPGA value after the specified timeout passes.

MSEL	"L"		"H"	
	60Ts		124Ts	
Zero-Cross Timeout	8kHz	7.5ms	8kHz	NA
	11.025kHz	5.4ms	11.025kHz	NA
	22.05kHz	2.7ms	22.05kHz	NA
	44.1kHz	NA	44.1kHz	2.8ms

Table 4. Zero-Cross Timeout Table for Limit Operation.

Addr = 01h LSTEP1-0: ATT Step at Limit Operation

LSTEP0 bit and LSTEP1 bit specify the decrement step size of IPGA value at Limit operation. For example, if the current value of IPGA is 0x46, and if LSTEP0 and LSTEP1 are "11", IPGA is updated to 0x42.

	LSTEP1	LSTEP0	ATT STEP
default	0	0	0.5dB
	0	1	1.0dB
	1	0	1.5dB
	1	1	2.0dB

■Recovery Operation

Recovery Time is defined as a reset cycle of Recovery Counter (RC). The cycle can be changed by the combination of MSEL bit, RWT0 bit, and RWT1 bit. Input signal enters Recovery Zone from other Zones, RC initiates counting. If the signal exits from Recovery Zone at lease once, RC is reset. When RC's value exceeds Recovery Time, the AK4533 is ready to update IPGA value, and RC is reset and counts again from "zero". IPGA value is actually updated once just after the signal crosses the ground. Therefore, the update cycle will change. Note that the update is one time in one Recovery Time and that the update of IPGA value is disabled until ROC is "zero" even if the signal crosses the ground several times. The AK4533 compares the IPGA value and Recovery Reference Level at the update timing. If IPGA value is greater than Recovery Reference Level, IPGA value is forced to Recovery Reference Level.

When the input signal enters Recovery Zone from any other Zones at the first time, the AK4533 waits for one Recover Time without updating of IPGA. After that, the AK4533 updates IPGA per one Recovery Time at zero-crossing point.

If the signal doesn't cross the ground, the AK4533 forces to update IPGA value after the time of Table 5 passes.

MSEL	"L"		"H"	
	252Ts		508Ts	
Zero-Cross Timeout	8kHz	31.5ms	8kHz	NA
	11.025kHz	22.9ms	11.025kHz	NA
	22.05kHz	11.4ms	22.05kHz	NA
	44.1kHz	NA	44.1kHz	11.5ms

Table 5. Zero-Cross Timeout Table for Recovery Time

Addr = 01h RSTEP-0: Recovery GAIN Step

RSTEP0 bit and RSTEP1 bit specify the increment step size of IPGA value at Recovery operation. For example, if the current value of IPGA is 0x42, and if RSTEP0 and RSTEP1 are "11", IPGA is set to 0x46.

	RSTEP1	RSTEP0	GAIN STEP
Default	0	0	0.5dB
	0	1	1.0dB
	1	0	1.5dB
	1	1	2.0dB

Addr = 01h RWT1-0: Recovery Time

	MSEL	RWT1	RWT0		Recovery Time			
					8kHz	11.025kHz	22.05kHz	44.1kHz
	0	0	0	256Ts	32ms	23ms	11.6ms	-
Default	0	0	1	512Ts	64ms	46ms	23ms	-
	0	1	0	1024Ts	128ms	93ms	46ms	-
	0	1	1	2048Ts	256ms	185ms	93ms	-
	1	0	0	512Ts	-	-	-	11.6ms
	1	0	1	1024Ts	-	-	-	23ms
	1	1	0	2048Ts	-	-	-	46ms
	1	1	1	4096Ts	-	-	-	93ms

Addr = 02h IPGA6-0: IPGA Control

When AGC bit is set to "0", IPGA value can be changed by the write operation to this register via A/T I/F directly.
When AGC bit is set to "1", The write to IPGA register is ignored. The AK4533 outputs updated value when the read operation is processed.

IPGA6-0

	DATA (HEX)	GAIN (dB)	STEP
	47	27.5	
	46	27.0	
	45	26.5	
	44	26.0	
	43	25.5	
	42	25.0	
	:	:	
Default	10	0.0	
	:	:	0.5dB
	06	-5.0	
	05	-5.5	
	04	-6.0	
	03	-6.5	
	02	-7.0	
	01	-7.5	
	00	-8	

Addr = 03h REF6-0: Recovery Reference Level

This value specifies the upper reference level of Recovery Operation when AGC is activated.
IPGA value is forced to set the same value as Recovery Reference Level when IPGA tries to exceed Recovery Reference Level under Recovery Operation. Therefore, IPGA is not greater than Recovery Reference Level.

Write the appropriate value when AGC bit is set to "0". Must NOT change this value while AGC is active.

REF6-0

	DATA (HEX)	Reference Level (dB)	STEP
	47	27.5	
	46	27.0	
	45	26.5	
	:	:	
default	36	19.0	
	:	:	0.5dB
	10	0.0	
	:	:	
	06	-5.0	
	05	-5.5	
	04	-6.0	
	03	-6.5	
	02	-7.0	
	01	-7.5	
	00	-8	

Addr = 04h Mute Mute Control
When the Mute bit is set to "1", input data to D/A converter is forced to set to zero regardless of D/A data from SDI pin. When the Mute bit is set to "0", D/A data is enabled. When reset, default value of Mute bit is "0".

Addr = 04h M3-0: Digital ATT Output Control
These bits control the attenuation level of DAC output. Step size of ATT is approximately 1.5dB. This value is still preserved even if DALPD bit and/or DARPD bit are set and/or reset.

	DATA (HEX)	DATT (dB)	STEP
default	00	0	
	01	1.48	
	02	2.95	
	03	4.43	
	04	6.02	
	05	7.5	
	06	8.97	
	07	10.45	1.5dB
	08	12.04	
	09	13.52	
	0A	14.99	
	0B	16.47	
	0C	18.06	
	0D	19.54	
	0E	21.01	
	0F	22.49	

Figure 13 describes the recovery operation.

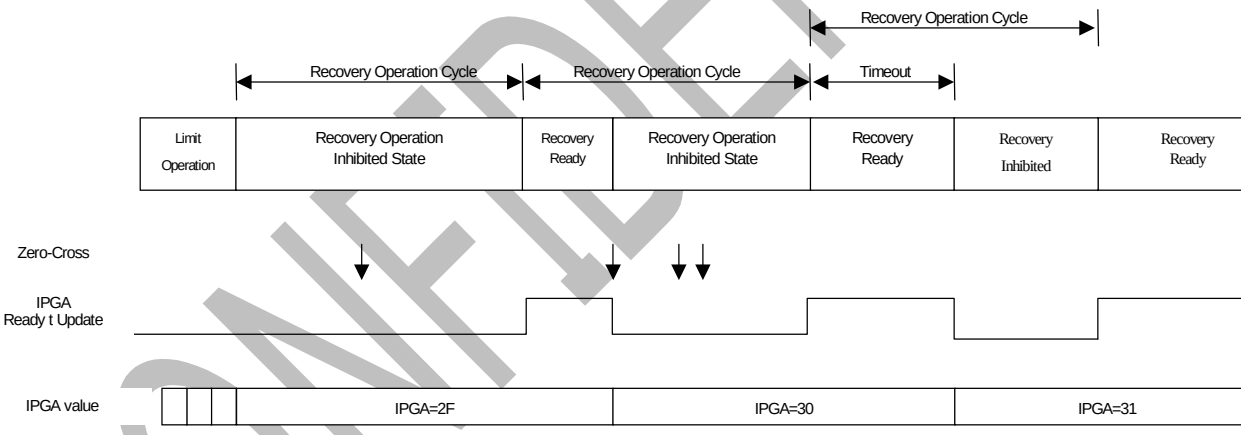


Figure 13. The Flow of Recovery Operation

MCLK Control

Master Clock frequency for audio codec is input to MCLK pin.
If sampling frequency is equal to or less than 22.05kHz, MSEL bit should be set to "0", requiring 512fs clock as MCLK pin. If sampling frequency is more than 22.05kHz, MSEL bit should be "1", requiring 256fs clock as MCLK pin. When MSEL bit is changed, MSEL bit must be written with all "1" of ADPD bit, DALPD bit and DARPD bit (power-down state). In addition to this, master clock, MCLK should be stopped.

MSEL: Selection of 256/512fs
"0": 512fs Default
"1": 256fs

Power-down Control

ADPD, DALPD, and DARPD can control power-down state of ADC and DAC. The AK4533 can power down Left channel of DAC and Right channel DAC independently.

ADPD: A/D Converter Power-down Enable
(0: Disable 1: Enable)
The write "1" to ADPD bit enables IPGA block and ADC to power down, and 00h - 03h registers are reset to default value.
The AK4533 ignores the write operation to 00h -03h registers.
The read operation is possible (The AK4533 outputs default value)
The write "0" to ADPD bit enables normal operation of ADC block.

The period (516Ts@ MSEL="1", 260Ts@ MSEL="0" is required until VREFAD is stable. The write to the registers is possible in this initial period, but AGC function is disabled for this period. The AK4533 initiates AGC operation automatically after the end of the period.

DALPD: Left Channel D/A Converter Power-down Enable
(0: Disable 1: Enable)
The write "1" to DALPD bit enables Left Channel D/A converter to power down. DALPD bit is set to "0", Left Channel of D/A converter goes to normal state.

DARPD: Right Channel D/A Converter Power-down Enable
(0: Disable 1: Enable)
The write "1" to DARPD bit enables Right Channel D/A converter to power down. DARPD bit is set to "0", Right Channel of D/A converter goes to normal state.

■ **System Clock and Power-up Timing**

MCLK, the master clock, must be present while ADC or/and DAC is under normal operation. Otherwise, excessive current may result from abnormal operation of internal dynamic logic. Clock should be stopped after power-down state.

PDB pin must be set to "H" first, and then, RESETB pin must be set to "H". After RESETB pin is cleared, ADC, and DAC are still in power-down mode. In order to activate ADC and/or DAC, write DALPD bit, DARPD bit and/or ADPD bit to "0" through A/T I/F. Note that MCLK must be present when ADC and/or DAC is under normal operation.
MCLK should be present when all registers except for MSEL bit should be accessed. MSEL bit should be updated without MCLK input.

MCLK can be stopped after RESETB = "L" or all of ADPD, DALPD, and DARPD are set to "1".

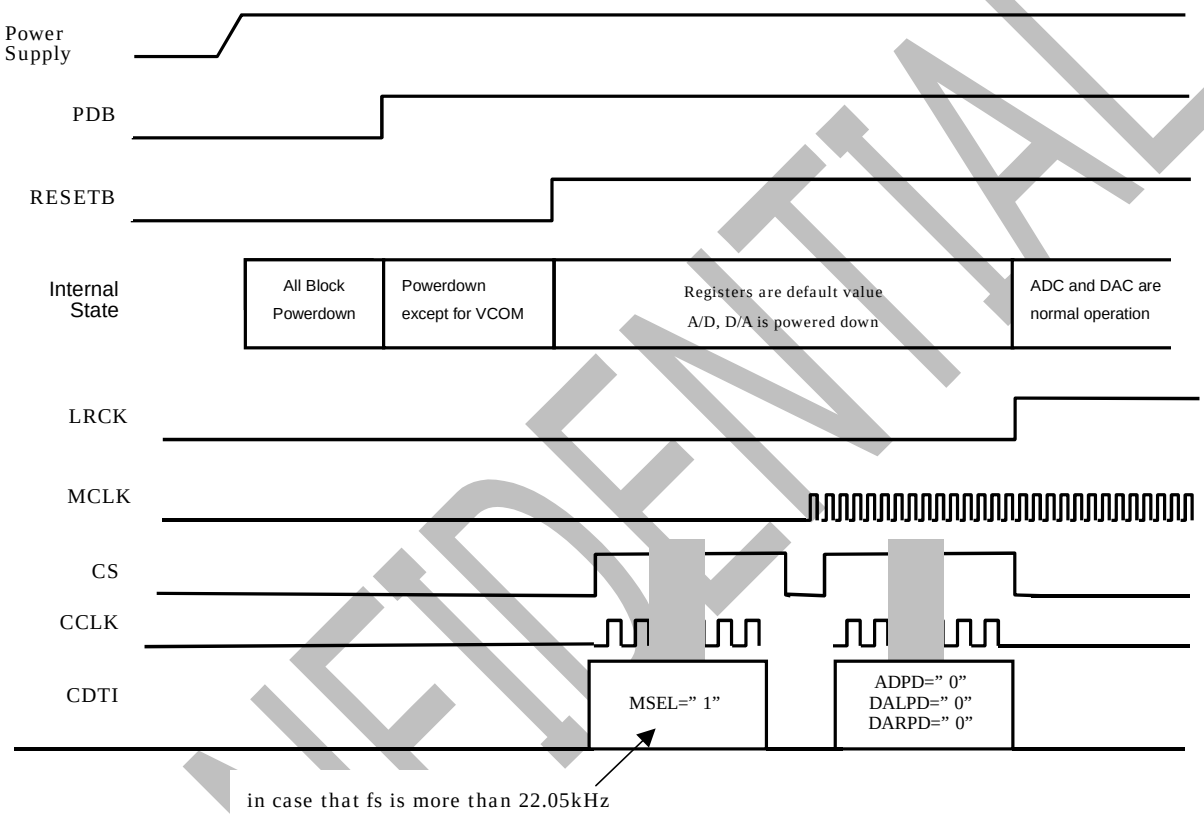


Figure 14. Power-up Timing (1)

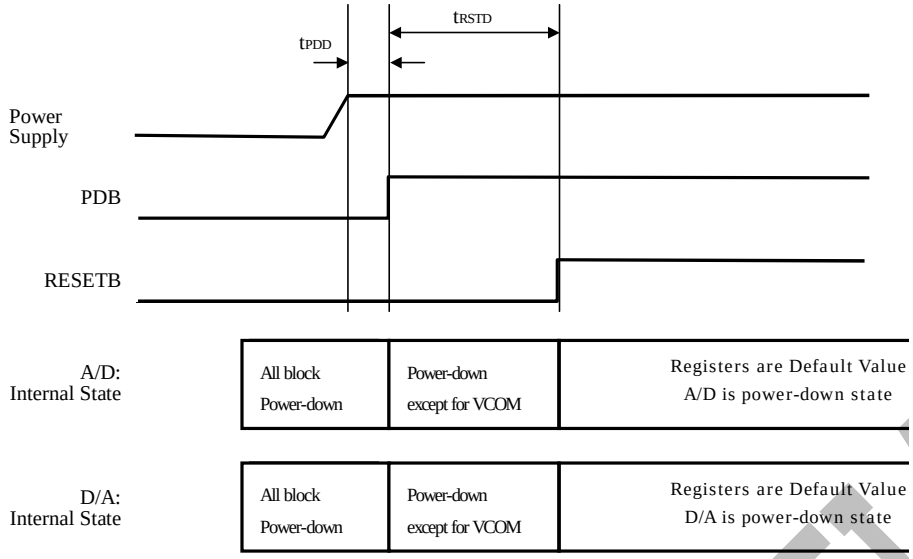


Figure 15. Power-up Timing (2)

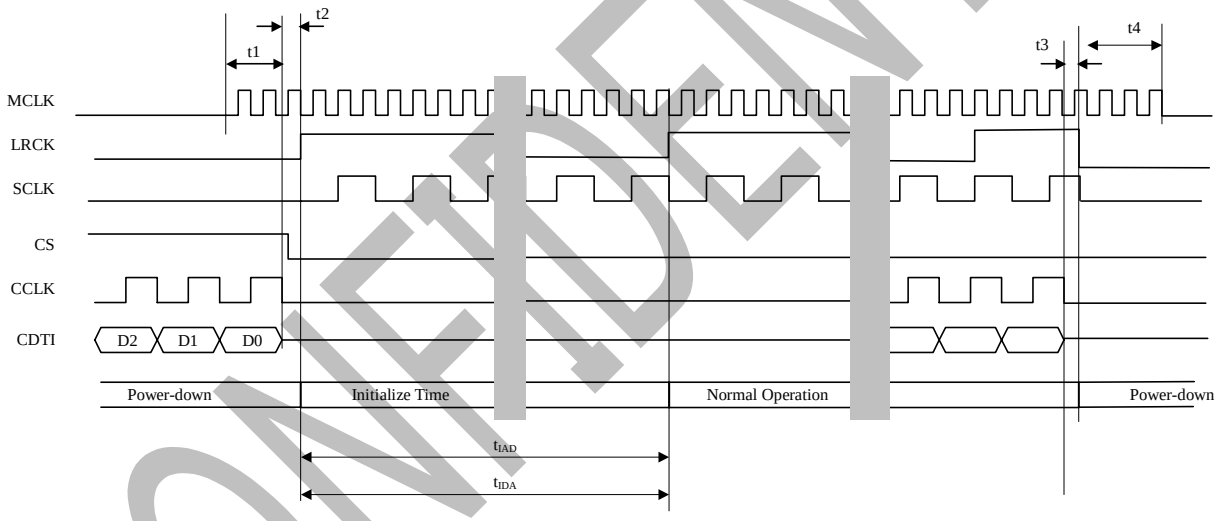


Figure 16. Power-down Timing (1)

Parameter	Symbol	min	Typ	max	Units
Audio					
from Power stable to PDB↑	tPDD	0 *Note1)*			ms
from PDB ↑ to RESETB↑	tRSTD	0 *Note 2)*	4 *Note 3)*		ms
from RESETB↓ to PDB↓		0 *Note 2)*			
Clear Power-down mode					
from MCLK input to 16CCLK↓	t1	1			tMCLK
from 16CCLK↓ to LRCK↑	t2			1	tMCLK
Initialize Time *Note 4)*					
A/D (MSEL="L")	tIAD		260		Ts
A/D (MSEL="H")	tIAD		516		Ts
D/A	tIDA		2		Ts
Power Down					
from 16CCLK↓ to LRCK stop ("L")	t3		10		ns
from 16CCLK↓ to SCLK Stop ("L")	t3		10		ns
from 16CCLK↓ to MCLK stop	t4	0			tMCLK

tMCLK= 1/fMCLK
Ts=1/fs

Note 1) VA, VD pins and PDB pins can be powered at the same time. However, PDB should NOT be powered before VA and VD. Otherwise, the device may be damaged, and the device may be destroyed at worst case.

Note 2) PDB pin and RESETB can be set to "H" at the same time. But note that the pop noise occurs at the transition of PDB. Keeping PDB pin high is suggested for preventing pop noise while the device is powered. Power management can be controlled by RESETB pin.

Note 3) The time in which VCOM settles to 95% of VDD with 4.7 μF and 0.1 μF capacitors.

Note 4) ADC initialization cycle, which takes 516@ MSEL="H", or 260Ts@TSEL-"L", starts after exiting ADC's power-down mode. In this cycle, the write to the register is possible, but the device disables AGC function. The device enables AGC automatically after this initialization cycle completes. DAC initialization cycle is 2Ts.

■ A/D Converter for Touch Screen

The AK4533 has 12 bit resolution Successive Approximation Resistor (SAR) A/D converter for touch screen, and the measurement of buttery voltage.
As A/D converter uses capacitive redistribution architecture, internal capacitors also operate as sample/hold circuit.

TSY_TOP pin or TSX_TOP pin, which is used for detecting the pressed position, is selected as analog input to ADC. VA is referred to as full scale of ADC. When BTI_1 pin, or BTI_2 pin is selected for the measurement of buttery voltage as analog input to A/D converter, TPVREFIN is referred to as full scale of ADC.

Tracking time, which is defined as the time to store the charge into internal capacitors, depends on the output impedance (Rin) of touch screen. If Rin is 500 Ω, at least 1.5 µs is required for tracking time. The AK4533 uses 3 TADCK cycles for tracking: If TADCK is 2MHz, tracking time is 0.5µs * 3 cycles = 1.5µs. If Rin is larger value at the measurement of buttery voltage, not only enough tracking time is required, but also the clock frequency of TADCK should be lower than 2MHz.

Data format of Touch Screen A/D converter is binary as Table 6.

Input Voltage	Output Code
(VREF-1.5LSB) - VREF	FFF
(VREF-2.5LSB) - (VREF-1.5LSB)	FFE
---------	---------
0.5LSB - 1.5LSB	001
0 - 0.5LSB	000

VREF : VA or TPVREFIN

Table 6. Data format

Figure 17 shows the touch screen controller block, and the connection between touch screen and the AK4533. Two times of A/D conversion is needed to detect the pressed position: one is for X-axis, and another is for Y-axis. A pair of terminals of touch screen is biased while another terminal is hi-Z state. ADC measures the voltage that is induced to TOP side of hi-Z terminals. For example, if TSX_TOP and TSX BTM are biased to VA, and AGND respectively, the ADC can output the dot on X-axis by measuring TSY_TOP voltage.

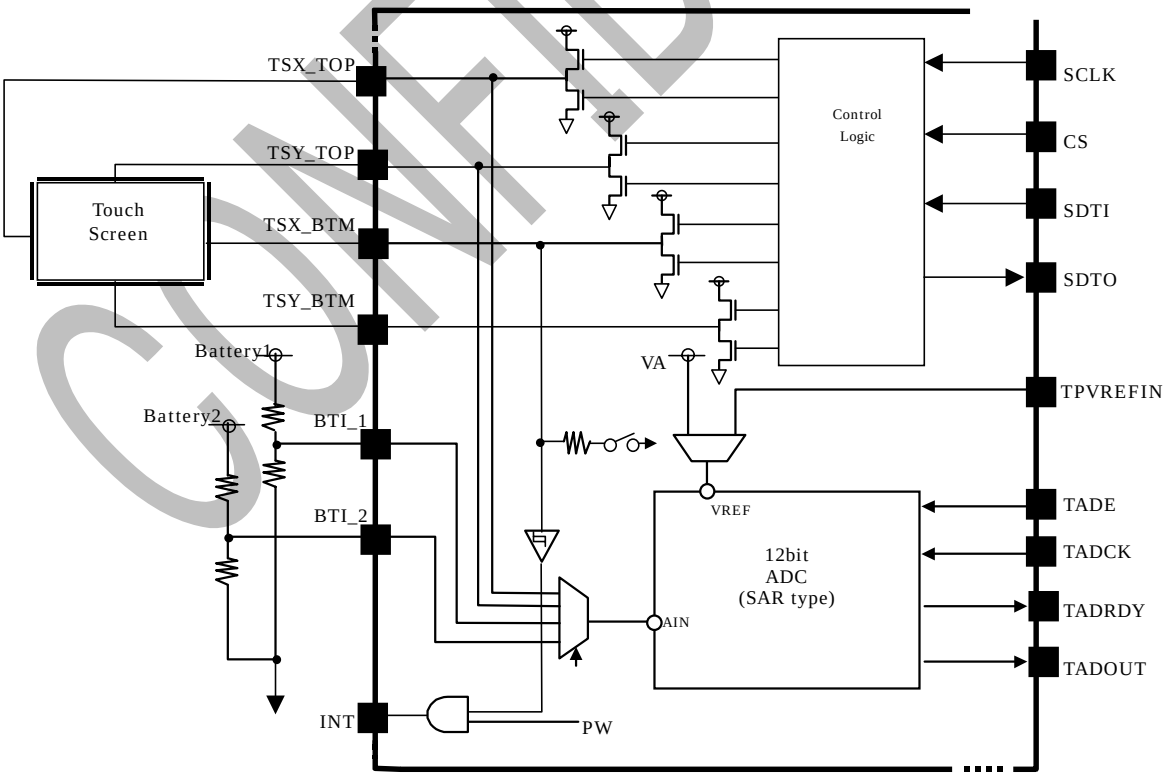


Figure 17. Connection between AK4533 and Touch Screen

The interface of touch screen controller block shares with audio control interface. (For the detail of read/write sequence, please see "Figure 12. Audio/Touch Screen Control Interface Timing")

■ Touch Screen Control Register

Addr		D7	D6	D5	D4	D3	D2	D1	D0	Default
07	Touch Screen Control	TSPD	PW	X	X	D3	D2	D1	D0	80

Table 7. Touch Screen Control Register

D3:D0 Selection of Input Channel/Output Channel

Table 8 describes the relationship between D3:D0 bits and the states of TSX_TOP, TSX_BTM, TSY_TOP, TSY_BTM, AIN, and VREF.

As TSX_TOP, TSX_BTM, TSY_TOP, and TSY_BTM can output one of the three voltage level, VA, AGND, and Hi-Z by the combination of D3:D0 bits, touch screen control block is very flexible. For example, there are two ways to measure the x-axis spot as No.1 configuration or No.2 configuration in Table 8.

Touch Screen Control Register(07h)							The State of Touch Screen Terminals				Analog Input	VREF Input	
No.	D7 (TSPD)	D6 (PW)	D3	D2	D1	D0	TSX_ TOP	TSX_ BTM	TSY_ TOP	TSY_ BTM	AIN	VREF	Note
0	0	0	0	0	0	0	VA	AGND	OPEN	OPEN	TSY_TOP	VA	X-axis Measurement
1	0	0	0	0	0	1	AGND	VA	OPEN	OPEN	TSY_TOP	VA	X-axis Measurement
2	0	0	0	0	1	0	OPEN	OPEN	VA	AGND	TSX_TOP	VA	Y-axis Measurement
3	0	0	0	0	1	1	OPEN	OPEN	AGND	VA	TSX_TOP	VA	Y-axis Measurement
4	0	0	0	1	0	0	AGND	OPEN	AGND	OPEN	X	VA	Discharge
5	0	0	0	1	0	1	OPEN	OPEN	OPEN	OPEN	X	VA	
6	0	0	0	1	1	0	AGND	AGND	OPEN	OPEN	X	VA	Discharge
7	0	0	0	1	1	1	OPEN	OPEN	AGND	AGND	X	VA	Discharge
8	0	0	1	X	X	0	OPEN	OPEN	OPEN	OPEN	BTI_1	TPVREFIN	Battery Measurement
9	0	0	1	X	X	1	OPEN	OPEN	OPEN	OPEN	BTI_2	TPVREFIN	Battery Measurement
10	0	1	1	X	X	0	OPEN	AGND_R	OPEN	VA	BTI_1	TPVREFIN	Pen Waiting & Battery Measurement
11	0	1	1	X	X	1	OPEN	AGND_R	OPEN	VA	BTI_2	TPVREFIN	Pen Waiting & Battery Measurement
12	1	1	X	X	X	X	OPEN	AGND_R	OPEN	VA	X	X	Pen Waiting & Power Down State
13	1	0	X	X	X	X	OPEN	OPEN	OPEN	OPEN	X	X	Power Down State (Default)

VA	Power Supply Voltage
AGND	Analog Ground
OPEN	Hi-Z state
BTI_1,BTI_2	Measurement of Buttery Voltage
TPVREFIN	External Reference Voltage
AGND_R	TSX_BTM is connected to AGND through internal resistor.

Table 8. The relationship between input/output channel and D3:D0 bits

TSPD Power-down Control of Touch Screen
If TSPD is set to "1", Touch Screen block including ADC goes to power-down mode regardless of D3,D2,D1,and D0 bits.
TSPD=”1” Power Down
TSPD=”0” Normal Operation

PW Waiting State for Interrupt
If PW bit is set to "1", the AK4533 goes to waiting state which can notify whether the touch screen is pressed or not. If the touch screen is pressed under this state, INT signal goes to "H", and goes to "L" when the pen is released. INT pin is "L" while the screen is not pressed. If PW bit is set to "0", INT pin is "L" regardless of pressing or releasing.

PW= “1” Interrupt Enable
PW= “0” Interrupt Disable

■ Interface for Touch Screen A/D Converter

A/D data for Touch Screen is controlled by 4-wire I/F, TADE, TADCK, TADRDY, and TADOUT.

The rising transition on TADE pin initiates a conversion cycle. Tracking and A/D conversion takes 16 TADCK with TADE "H" state.
First 3 TADCK is for tracking time. At the falling edge of 4th TADCK, TADRDY goes "H", which shows that most significant bit (MSB) is ready to output on TADOUT, and the AK4533 outputs MSB at the same time on TADOUT. The AK4533 continues to output A/D data serially at the falling edge of TADCK. At the 15th falling edge of TADCK, the AK4533 outputs least significant bit (LSB). TADOUT can be returned to "L" at the falling edge of 16th TADCK.

TADE must be set to "L" per completion of one A/D conversion cycle. TADE can be set to "L" at the same time of the falling edge of 16th TADCK.

If 17 or more TADCK is input to the device, the output of TADOUT is "L".

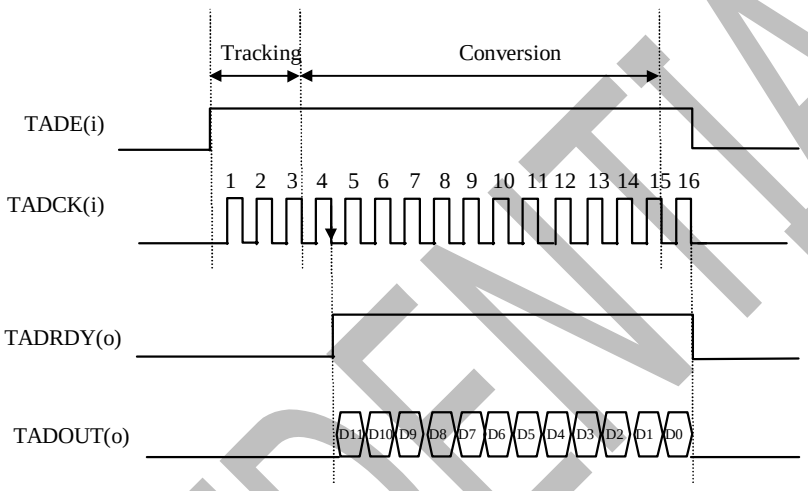


Figure 18. The Timing of Touch Screen A/D Converter

■ Measurement Sequence

Figure 19 shows the case in which TPX_TOP and TPY_BTM terminals are supplied by VA and AGND respectively, and in which ADC measures the voltage on TPY_TOP pin. The write 0x00 to 07h register via A/T I/F activates this configuration. A/D data should be read through TC I/F after the input voltages to touch screen are stable.

The value must NOT be written to 07h register while TADE is "H".

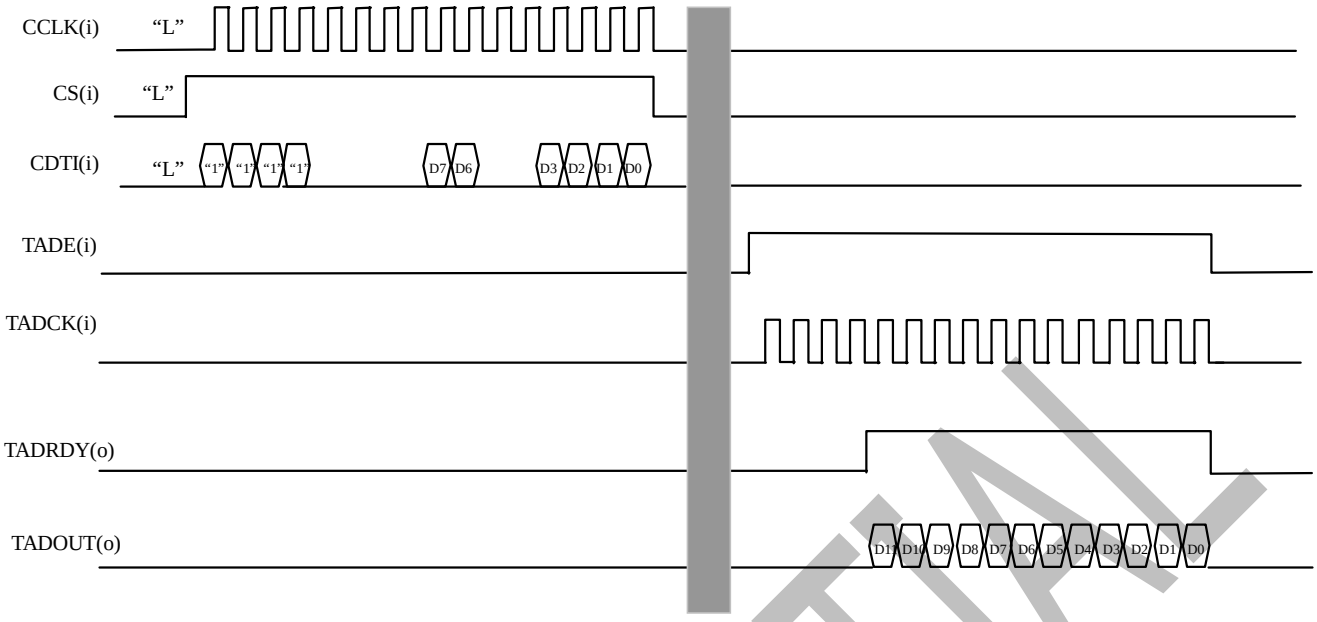


Figure 19. Control Sequence of Touch Screen

■ Power Down of Touch Screen

When the TSPD bit in Touch Screen Control register (07h) is set to "1", touch screen driver and A/D converter goes to power-down mode. As the register value is still preserved in power-down mode, the register can be accessed under power-down mode.

■ Waiting State for Pen Interrupt and INT Signal

When the PW bit in Touch Screen Control register (07h) is set to "1", the AK4533 goes to the state which waits for the interrupt caused by touching the screen. INT pin outputs "H" through internal schmitt trigger buffer while the screen is being touched. INT signal can notify to the external circuit that the screen is touched.

The AK4533 supplies VA to TSY_BTM with keeping TSY_TOP and TSX_TOP open state under Waiting State for Pen Interrupt. And TSX_BTM is connected to AGND through the internal resistor, Ro.
If the screen is not touched, the current doesn't flow from Y-Plate to X-Plate because two plates are not connected, and TSX_BTM is "L" because this terminal is connected to AGND through Ro.

When the screen is touched, the current flows from Y-Plate to X-Plate. As the resistor value of touch screen is much smaller than that of Ro, the level of TSX_BTM is "H". This INT signal can be used as the interrupt signal to the micro controller. When the screen is touched, INT goes "H", and returned "L" when the pen is released.

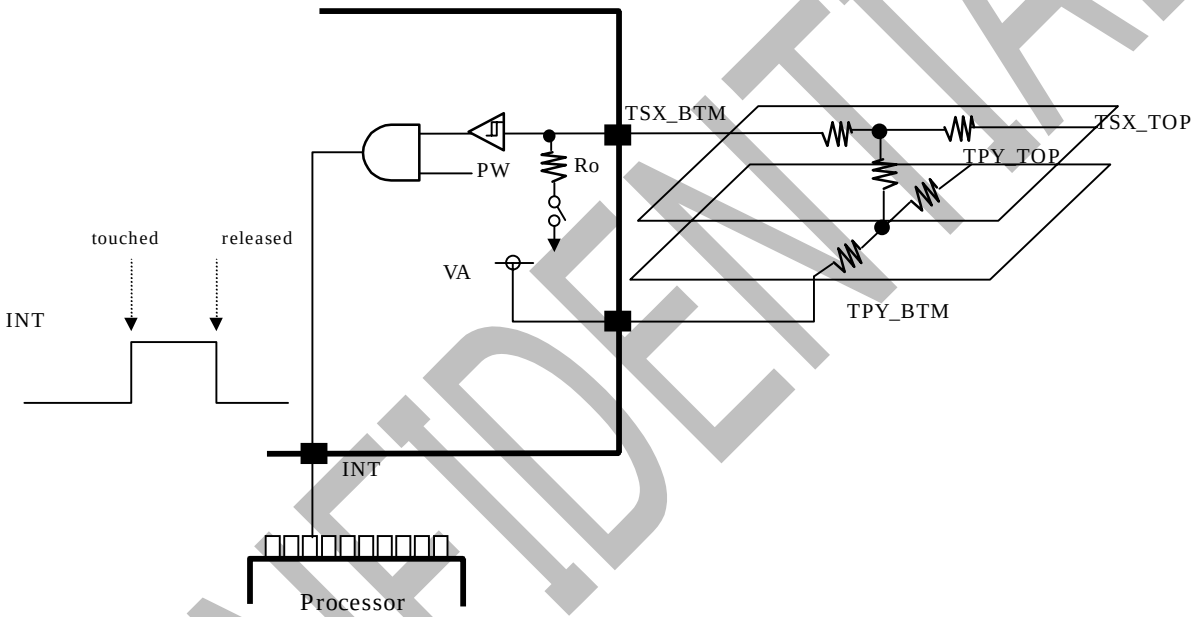


Figure 20. Waiting for Pen Interrupt

■ Measurement of Battery Voltage

The voltage that is divided by the appropriate registers is input to BTI_1 pin or BTI_2 pin in order to measure battery voltage. TPVREFIN is referred to as full scale.

A/T I/F is used for the selection of input channels, BTI_1 or BTI_2. The input voltage to BTI_1 and BTI_2 must NOT exceed VA voltage.

If the impedance of input signal is high, enough tracking time is required to charge the internal capacitors through BTI_1 or BIT_2. And if the input impedance of TPVREFIN is high, clock frequency of TADCK must be low.

<The relationship between BIT_1/2 input impedance and tracking time>
For example, if the external battery voltage that is divided by two 30k Ω resistors is input to BTI_1 or BTI_2, the input impedance is 15 k Ω. In this case, tracking times should be at least 50μs. If the input impedance is 30 k Ω, tracking time should be at least 100 μs.

<The relationship between TPVREFIN and TADCK>
For example, external reference voltage that is divided by 10 k Ω and 30k Ω is input to TPVREFIN, input impedance of TPVREFIN is about 7.5k Ω. In this case, the clock frequency of TADCK should be 160kHz or less.

As full-scale error increases with high input impedance, high input impedance is not suggested. If the full scale error and long conversion time can be ignored, high input impedance may be used.

As the measurement of battery voltage and detecting pen interrupt can be controlled independently, micro-controller can knows the interrupt while the battery measurement.

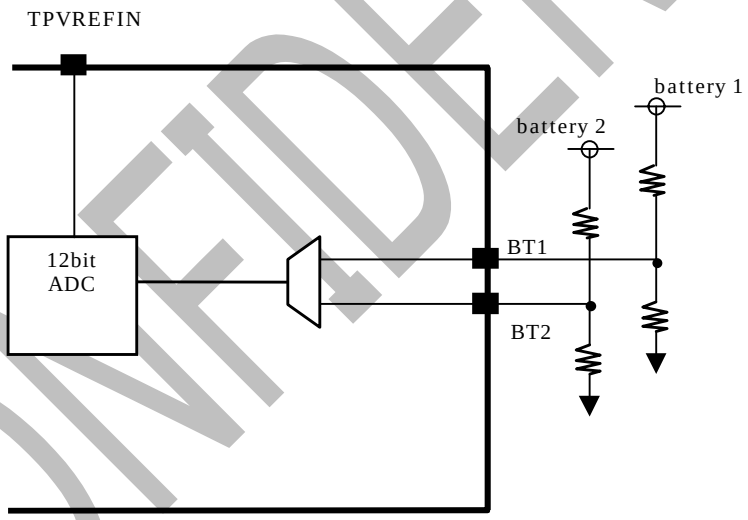


Figure 21. Block Diagram of Battery Measurement

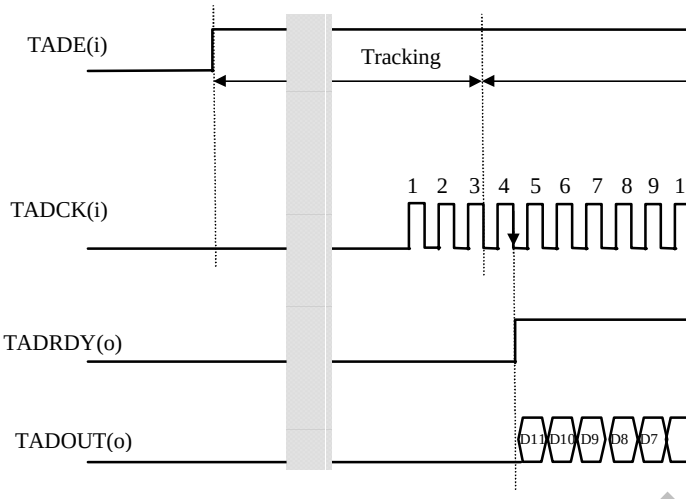


Figure 22. The relationship between BIT_1/2 input impedance and tracking time

■ **System Diagram**

Figure 23shows the system diagram. VA and VD should be powered at the same time, or VA should be powered earlier than VD. In order to achieve this sequence, VD is supplied from VA via 10 Ω resistor as shown in Figure 23. The voltage should not be supplied to the input pins including TPVREFIN, BTI_1, and BTI_2 before VA and VD are powered.

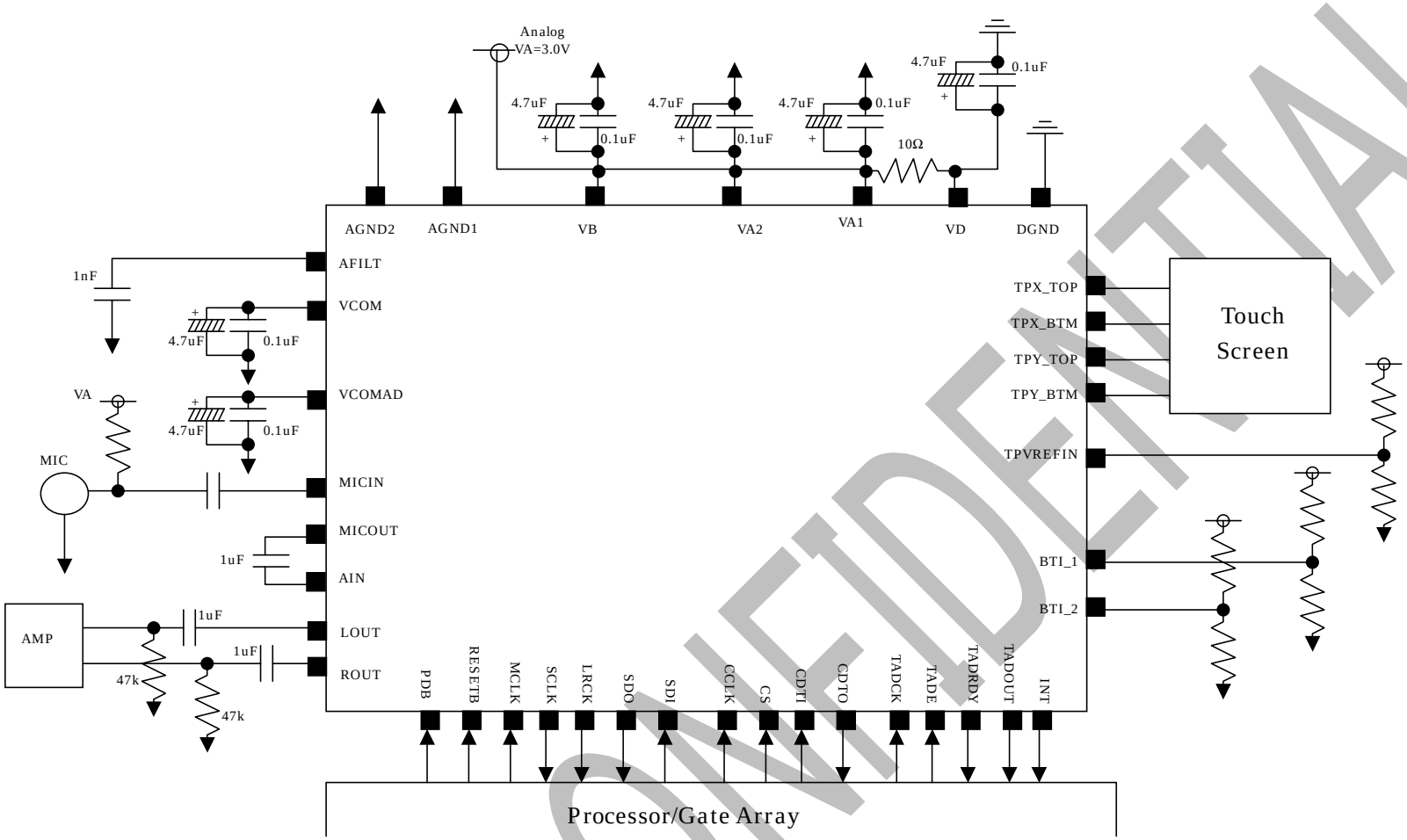
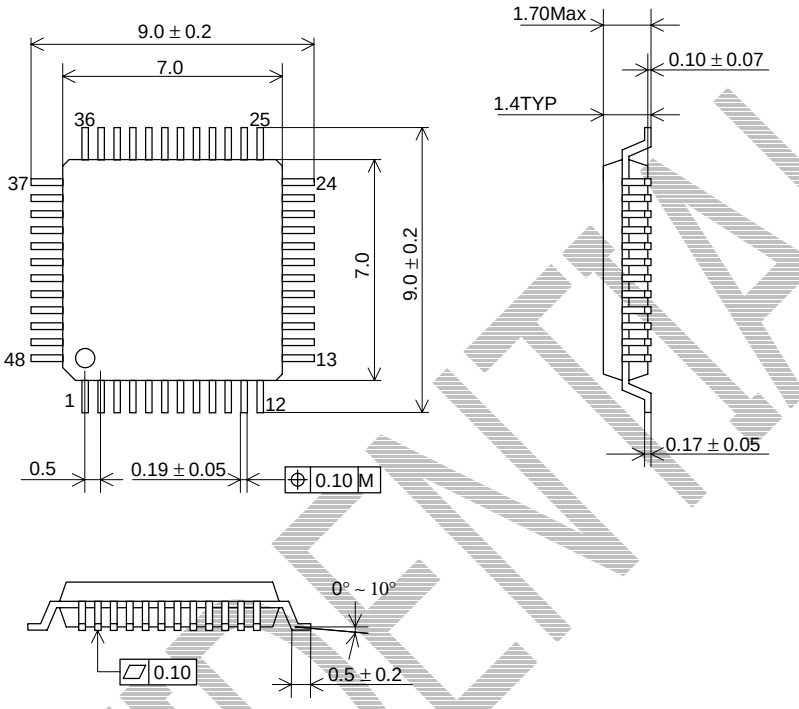


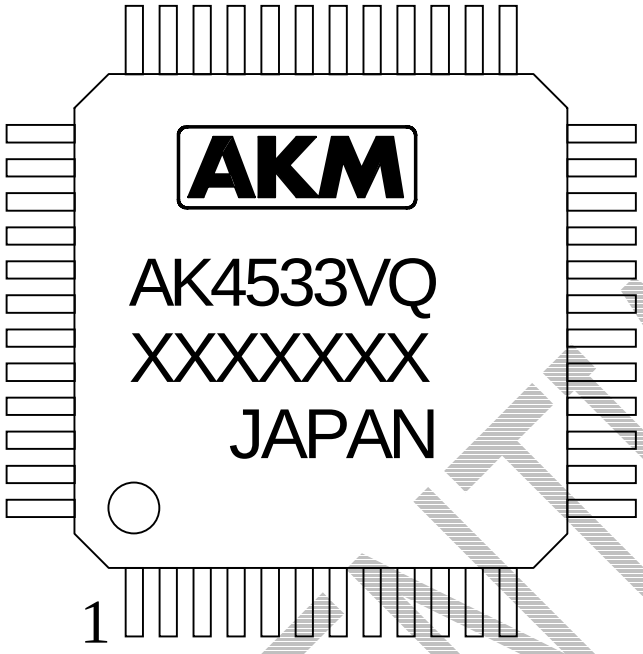
Figure 23. The AK4533 System Diagram

Package

48pin LQFP(Unit:mm)



Marking



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4533VQ
4) Country of Origin
5) Asahi Kasei Logo

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