

FEATURES

- InGaP HBT Technology
- Low profile 1.1 mm
- Small Package Outline 6 mm x 6 mm
- EGPRS Capable (class 12)
- Integrated Reference Voltage

GMSK MODE

- Integrated power control (CMOS)
- +35 dBm GSM850/900 Output Power
- +33 dBm DCS/PCS Output Power
- 55 % GSM850/900 PAE
- 52 % DCS/PCS PAE
- Power control range > 50 dB

EDGE MODE

- +28.5 dBm GSM850/900 Output Power
- +27.5 dBm DCS/PCS Output Power
- -66 dBc Typical ACPR (400 kHz)
- -78 dBc Typical ACPR (600 kHz)

APPLICATIONS

- Dual/Tri/Quad Band Handsets, PDAs and Data Devices

PRODUCT DESCRIPTION

This quad band power amplifier module supports dual, tri and quad band applications for both GMSK and 8-PSK modulation schemes. There are two amplifier chains, one to support GSM850/900 bands, the other for DCS/PCS bands.

The module includes an integrated power control scheme for use in the GMSK mode. This facilitates fast and easy production calibration and reduces the number of external components required to complete a power control function. The amplifier's power control range is typically 55 dB, with the output power set by applying an analog voltage to V_{RAMP} .

In EDGE mode, the V_{RAMP} pin is disabled and no specific voltage is required for proper operation. Output power is controlled by varying the input power.

All of the RF ports for this device are internally matched to 50Ω .

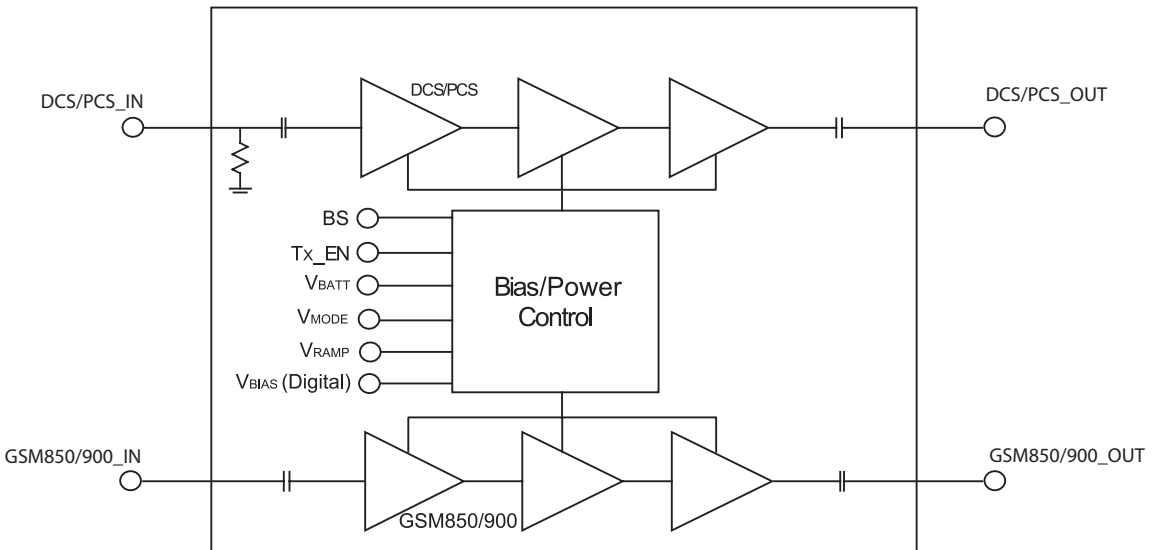


Figure 1: Block Diagram

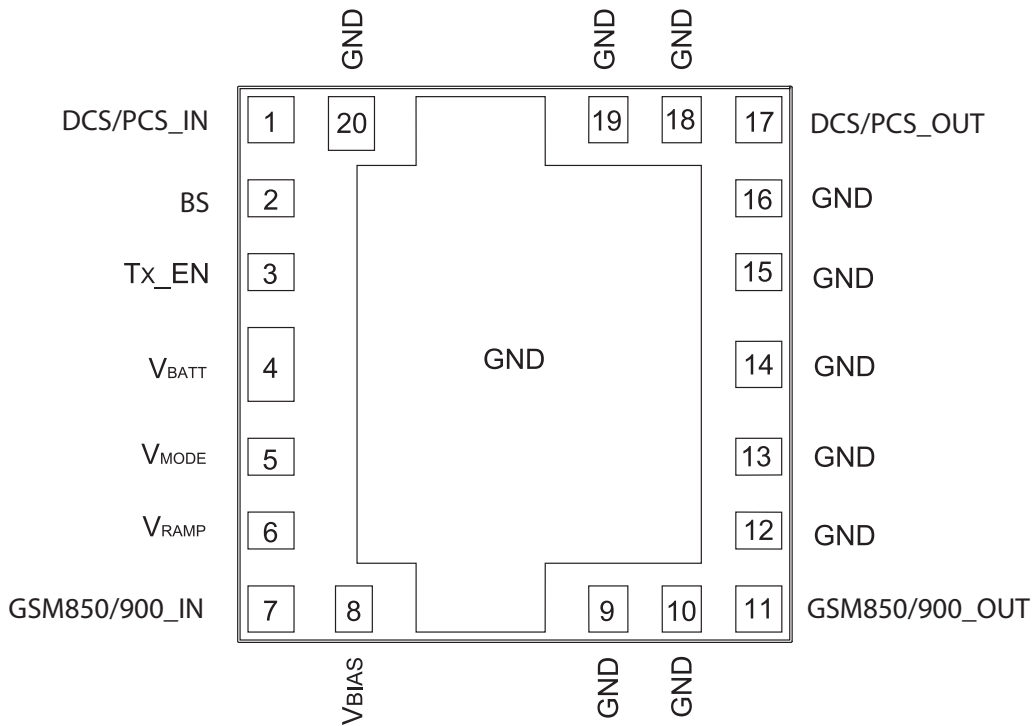


Figure 2: Pinout (X - ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	DCS/PCS_IN	RF input to the DCS/PCS PA. There is a 175 Ω shunt resistor before the DC blocking capacitor to set the input impedance
2	BS	Band select logic pin. Logic low selects the GSM PA and a logic high selects the DCS/PCS PA
3	TX_EN	TX enable logic pin, a logic high will enable the PA
4	V _{BATT}	Battery supply connection
5	V _{MODE}	Logic pin for selection of GMSK or 8PSK (EDGE) mode. A logic low selects GMSK mode and a logic high selects the 8PSK mode
6	V _{RAMP}	Analog output power control pin
7	GSM850/900_IN	RF input to GSM850/900 PA.
8	V _{BIAS}	V _{BIAS} logic input. A logic low sets a low bias point for current savings at low power levels, a logic high sets a high bias point for meeting linearity performance up to the maximum specified linear output power
9	GND	Ground
10	GND	Ground
11	GSM850/900_OUT	RF output for GSM850/900 bands (DC blocked)
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	DCS/PCS_OUT	RF output for DCS/PCS bands (DC blocked)
18	GND	Ground
19	GND	Ground
20	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Supply Voltage (V_{BATT})	-0.5	+6	V
RF Input Power (RF_{IN})	-	12	dBm
Control Voltage (V_{RAMP})	-0.3	3.0	V
Storage Temperature (T_{STG})	-55	150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: ESD Ratings

PARAMETER	METHOD	RATING	UNIT
ESD Threshold voltage (RF ports)	HBM	2.5	kV
ESD Threshold voltage (control inputs)	HBM	2.5	kV

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Human body model HBM employed is resistance = 1500 Ω , capacitance = 100pF.

Table 4: Digital Inputs

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic High Voltage	V_{IH}	1.2	-	3.0	V
Logic Low Voltage	V_{IL}	-0.5	-	0.5	V
Logic High Current	$ I_{IH} $	-	-	30	μA
Logic Low Current	$ I_{IL} $	-	-	30	μA

Table 5: Logic Control Table

OPERATIONAL MODE	V _{MODE}	BS	TX_EN	V _{BIAS}	NOTES
GSM850/900 GMSK	LOW	LOW	HIGH	X	V _{RAMP} Controls Output Power, X = Don't Care
DCS/PCS GMSK	LOW	HIGH	HIGH	X	V _{RAMP} Controls Output Power, X = Don't Care
GSM850/900 EDGE	HIGH	LOW	HIGH	HIGH	V _{RAMP} Control Disabled, Fixed Gain PA
DCS/PCS EDGE	HIGH	HIGH	HIGH	HIGH	V _{RAMP} Control Disabled, Fixed Gain PA
GSM850/900 EDGE (Low Power Levels) ⁽¹⁾	HIGH	LOW	HIGH	LOW	V _{RAMP} Control Disabled, Fixed Gain PA
DCS/PCS EDGE (Low Power Levels) ⁽²⁾	HIGH	HIGH	HIGH	LOW	V _{RAMP} Control Disabled, Fixed Gain PA
PA DISABLED	X	X	LOW	X	X = Don't Care

Notes:

(1) $P_{OUT} \leq +20$ dBm.(2) $P_{OUT} \leq +19$ dBm.

Table 6: Operating Ranges

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Case temperature	T_C	-20	-	85	$^{\circ}\text{C}$
Supply voltage	V_{BATT}	3.2	3.6	4.5	V
Control voltage	V_{RAMP}	0.25	-	2.2	V
Power supply leakage current	$V_{\text{BATT}} = 4.5 \text{ V},$ $V_{\text{RAMP}} = 0 \text{ V}, \text{TX_EN} = \text{LOW}$ No RF applied	-	-	5	μA
V_{RAMP} Input Capacitance	-	-	3	-	pF
V_{RAMP} Input Current	-	-	-	10	μA
Rise Time (T_{RISE})	$P_{\text{OUT}} = -10 \text{ dBm} \rightarrow P_{\text{MAX}}$ (within 0.2 dB)	-	0.4	1	μs
Fall Time (T_{FALL})	$P_{\text{OUT}} = P_{\text{MAX}} \rightarrow -10 \text{ dBm}$ (within 0.2 dB)	-	0.5	1	μs
Mode Switch	GMSK \rightarrow EDGE EDGE \rightarrow GMSK	-	0.4	1	μs
V_{BIAS} Switch	High Power \rightarrow Low Power Low Power \rightarrow High Power	-	-	1	μs
Duty Cycle	-	-	-	50	%

Table 7: Electrical Characteristics for GSM850 GMSK Mode

Unless otherwise specified: $V_{BATT} = 3.6\text{ V}$, $P_{IN} = +2.0\text{ dBm}$, Pulse Width = 1154 μs , Duty Cycle 25%,
 $Z_{IN} = Z_{OUT} = 50\Omega$, $T_C = 25\text{ }^\circ\text{C}$, $V_{RAMP} = 2.2\text{ V}$, $BS = \text{LOW}$, $TX_EN = \text{HIGH}$, $V_{MODE} = \text{LOW}$

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_o)	824	-	849	MHz	
Input Power	0	+2	+4	dBm	
Output Power, P_{MAX}	34.5	35.1	-	dBm	
Degraded Output Power	32.5	33.5	-	dBm	$V_{BATT} = 3.2\text{ V}$, $T_C = +85\text{ }^\circ\text{C}$ $P_{IN} = 0\text{ dBm}$
PAE @ P_{MAX}	47	54	-	%	
Forward Isolation 1	-	-45	-30	dBm	$TX_EN = \text{LOW}$, $P_{IN} = +4\text{ dBm}$
Forward Isolation 2	-	-28	-10	dBm	$TX_EN = \text{HIGH}$, $V_{RAMP} = 0.25\text{ V}$, $P_{IN} = +4\text{ dBm}$
Cross Isolation F_o @ DCS/PCS port $2F_o$, $3F_o$ @ DCS/PCS port	- - -	-2 -22	+2 -16	dBm	$P_{OUT} \leq 34.5\text{ dBm}$
Harmonics Second Harmonic ($2F_o$) Third Harmonic ($3F_o$) 4 F_o to 15 F_o	- - -	-21 -20 -20	-10 -10 -8	dBm	$P_{OUT} \leq 34.5\text{ dBm}$
Stability (all spurious)	Output Load VSWR = 6:1, All Phases $P_{OUT} \leq 34.5\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$, RBW = 3 MHz
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$, RBW = 3 MHz
Ruggedness	No Degradation, No Damage			Load VSWR = 10:1, All Phase Angles; $P_{OUT} \leq 34.5\text{ dBm}$	
RX Noise Power	-	-84	-81	dBm	$F_{TX} = 849\text{ MHz}$, RBW = 100 kHz $F_{RX} = 869\text{ to }894\text{ MHz}$, $P_{OUT} \leq 34.5\text{ dBm}$
Input Return Loss	-	-	2.5:1	VSWR	

Table 8: Electrical Characteristics for GSM900 GMSK Mode

Unless otherwise specified: $V_{BATT} = 3.6\text{ V}$, $P_{IN} = +2.0\text{ dBm}$, Pulse Width = 1154 μs , Duty Cycle 25%,
 $Z_{IN} = Z_{OUT} = 50\Omega$, $T_C = 25\text{ }^\circ\text{C}$, $V_{RAMP} = 2.2\text{ V}$, $BS = \text{LOW}$, $TX_EN = \text{HIGH}$, $V_{MODE} = \text{LOW}$

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_o)	880	-	915	MHz	
Input Power	0	+2	+4	dBm	
Output Power, P_{MAX}	34.5	35.1	-	dBm	
Degraded Output Power	32.5	33.5	-	dBm	$V_{BATT} = 3.2\text{ V}$, $T_C = +85\text{ }^\circ\text{C}$ $P_{IN} = 0\text{ dBm}$
PAE @ P_{MAX}	49	55	-	%	
Forward Isolation 1	-	-45	-30	dBm	$TX_EN = \text{LOW}$, $P_{IN} = +4\text{ dBm}$
Forward Isolation 2	-	-27	-10	dBm	$TX_EN = \text{HIGH}$, $V_{RAMP} = 0.25\text{ V}$, $P_{IN} = +4\text{ dBm}$
Cross Isolation F_o @ DCS/PCS port $2F_o$, $3F_o$ @ DCS/PCS port	- - -	-2 -21	+2 -16	dBm	$P_{OUT} \leq 34.5\text{ dBm}$
Harmonics Second Harmonic ($2F_o$) Third Harmonic ($3F_o$) $4F_o$ to $15F_o$	- - -	-21 -23 -20	-10 -10 -8	dBm	$P_{OUT} \leq 34.5\text{ dBm}$
Stability (all spurious)	Output Load VSWR = 6:1, All Phases $P_{OUT} \leq 34.5\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$, RBW = 3 MHz
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$, RBW = 3 MHz
Ruggedness	No Degradation, No Damage			Load VSWR = 10:1, All Phase Angles; $P_{OUT} \leq 34.5\text{ dBm}$	
RX Noise Power 10 MHz Offset	-	-80	-75	dBm	$F_{TX} = 915\text{ MHz}$, RBW = 100 kHz $F_{RX} = 925\text{ to }935\text{ MHz}$, $P_{OUT} \leq 34.5\text{ dBm}$
20 MHz Offset	-	-84	-81		$F_{TX} = 915\text{ MHz}$, RBW = 100 kHz $F_{RX} = 935\text{ to }960\text{ MHz}$, $P_{OUT} \leq 34.5\text{ dBm}$
Input Return Loss	-	-	2.5:1	VSWR	

Table 9: Electrical Characteristics for GSM850 EDGE Mode
Unless otherwise specified: V_{BATT} = 3.6 V, Pulse Width = 1154 μ s, Duty Cycle 25%
Z_{IN} = Z_{OUT} = 50 Ω , T_c = 25 °C, BS = LOW, TX_EN = HIGH, VMODE = HIGH

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F _o)	824	-	849	MHz	
Linear P _{OUT} (High Power Mode) Linear P _{OUT} (Low Power Mode)	28.5 20	- -	- -	dBm	V _{BIAS} = High V _{BIAS} = Low
Linear Degraded Output Power L _D _P _{OUT} (High Power Mode) ⁽¹⁾ L _D _P _{OUT} (Low Power Mode) ⁽²⁾	26 17.5	- -	- -	dBm	Meets ACPR and EVM limits specified under nominal conditions
Linear Gain (High Power Mode)	29.0	31.5	34.0	dB	V _{BIAS} = High
Linear Gain (Low Power Mode)	24.0	28.5	34.0	dB	V _{BIAS} = Low
Gain Variation	-	-0.015	-	dB/°C	-20 °C ≤ T _c ≤ +85 °C
Power-Added Efficiency	-	22	-	%	P _{OUT} = 28.5 dBm
I _{cq} (Low Power Mode)	-	100	-	mA	V _{BIAS} = Low
Error Vector Magnitude (EVM)	-	2	5	%	
Linearity ACPR1 ACPR2 ACPR3	- - -	-38 -66 -79	-33 -58 -64	dBc	P _{OUT} ≤ 28.5 dBm, BW = 30 kHz F _o ± 200 kHz F _o ± 400 kHz F _o ± 600 kHz
Cross Isolation F _o @ DCS/PCS port 2F _o , 3F _o @ DCS/PCS port	- -	-7 -50	0 -20	dBm	P _{OUT} ≤ 28.5 dBm
Harmonics Second Harmonic (2F _o) Third Harmonic (3F _o) 4F _o to 15F _o	- - -	-40 -35 -20	-20 -15 -10	dBm	P _{OUT} ≤ 28.5 dBm
Stability (all spurious)	Output Load VSWR = 6:1 All Phases, P _{OUT} ≤ 28.5 dBm				
	-	-	-36	dBm	F _{OUT} < 1 GHz, RBW = 3 MHz
	-	-	-30	dBm	F _{OUT} > 1 GHz, RBW = 3 MHz
Ruggedness	No Degradation, No Damage			Load VSWR = 10:1, All Phase Angles; P _{OUT} ≤ 28.5 dBm	
RX Noise Power	-	-83	-80	dBm	F _{TX} = 849 MHz, RBW = 100 kHz F _{RX} = 869 to 894MHz, P _{OUT} ≤ 28.5 dBm
Input Return Loss	-	-	2.5:1	VSWR	

Notes:

(1) V_{BIAS} = High, V_{BATT} = Range (3.2 V ≤ V_{BATT} ≤ 4.5 V), Temp = Range (-20 °C ≤ T_c ≤ +85 °C).(2) V_{BIAS} = Low, V_{BATT} = Range (3.2 V ≤ V_{BATT} ≤ 4.5 V), Temp = Range (-20 °C ≤ T_c ≤ +85 °C).

Table 10: Electrical Characteristics for GSM900 EDGE Mode
Unless otherwise specified: $V_{BATT} = 3.6\text{ V}$, Pulse Width = 1154 μs , Duty Cycle 25%
 $Z_{IN} = Z_{OUT} = 50\Omega$, $T_c = 25\text{ }^\circ\text{C}$, BS = LOW, TX_EN = HIGH, VMODE = HIGH

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_o)	880	-	915	MHz	
Linear P_{OUT} (High Power Mode) Linear P_{OUT} (Low Power Mode)	28.5 20	- -	- -	dBm	$V_{BIAS} = \text{High}$ $V_{BIAS} = \text{Low}$
Linear Degraded Output Power Ld_P_{OUT} (High Power Mode) ⁽¹⁾ Ld_P_{OUT} (Low Power Mode) ⁽²⁾	26 17.5	- -	- -	dBm	Meets ACPR and EVM limits specified under nominal conditions
Linear Gain (High Power Mode)	29.0	32.0	34.0	dB	$V_{BIAS} = \text{High}$
Linear Gain (Low Power Mode)	24	29.0	34	dB	$V_{BIAS} = \text{Low}$
Gain Variation	-	-0.015	-	dB/ $^\circ\text{C}$	$-20\text{ }^\circ\text{C} \leq T_c \leq +85\text{ }^\circ\text{C}$
Power-Added Efficiency	-	22	-	%	$P_{OUT} = 28.5\text{ dBm}$
I_{cq} (Low Power Mode)	-	100	-	mA	$V_{BIAS} = \text{Low}$
Error Vector Magnitude (EVM)	-	2	5	%	
Linearity ACPR1 ACPR2 ACPR3	- - -	-36 -67 -79	-33 -58 -64	dBc	$P_{OUT} \leq 28.5\text{ dBm}$, BW = 30 kHz $F_o \pm 200\text{ kHz}$ $F_o \pm 400\text{ kHz}$ $F_o \pm 600\text{ kHz}$
Cross Isolation F_o @ DCS/PCS port $2F_o$, $3F_o$ @ DCS/PCS port	- -	-7 -50	0 -20	dBm	$P_{OUT} \leq 28.5\text{ dBm}$
Harmonics Second Harmonic ($2F_o$) Third Harmonic ($3F_o$) $4F_o$ to $15F_o$	- - -	-40 -35 -20	-20 -15 -10	dBm	$P_{OUT} \leq 28.5\text{ dBm}$
Stability (all spurious)	Output Load VSWR = 6:1 All Phases, $P_{OUT} \leq 28.5\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$, RBW = 3 MHz
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$, RBW = 3 MHz
Ruggedness	No Degradation, No Damage				Load VSWR = 10:1, All Phase Angles; $P_{OUT} \leq 28.5\text{ dBm}$

Notes:

(1) $V_{BIAS} = \text{High}$, $V_{BATT} = \text{Range}$ ($3.2\text{ V} \leq V_{BATT} \leq 4.5\text{ V}$), $Temp = \text{Range}$ ($-20\text{ }^\circ\text{C} \leq T_c \leq +85\text{ }^\circ\text{C}$).

(2) $V_{BIAS} = \text{Low}$, $V_{BATT} = \text{Range}$ ($3.2\text{ V} \leq V_{BATT} \leq 4.5\text{ V}$), $Temp = \text{Range}$ ($-20\text{ }^\circ\text{C} \leq T_c \leq +85\text{ }^\circ\text{C}$).

Table 10: Electrical Characteristics for GSM900 EDGE Mode (Continued)
Unless otherwise specified: $V_{BATT} = 3.6\text{ V}$, Pulse Width = $1154\mu\text{s}$, Duty Cycle 25%
 $Z_{IN} = Z_{OUT} = 50\Omega$, $T_C = 25\text{ }^\circ\text{C}$, BS = LOW, TX_EN = HIGH, VMODE = HIGH

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
RX Noise Power 10 MHz Offset	-	-80	-75	dBm	$F_{TX} = 915\text{ MHz}$, $RBW = 100\text{ kHz}$ $F_{RX} = 925\text{ to }935\text{ MHz}$, $P_{OUT} \leq 28.5\text{ dBm}$ $F_{TX} = 915\text{ MHz}$, $RBW = 100\text{ kHz}$ $F_{RX} = 935\text{ to }960\text{ MHz}$, $P_{OUT} \leq 28.5\text{ dBm}$
20 MHz Offset	-	-83	-80		
Input Return Loss	-	-	2.5:1	VSWR	

Table 11: Electrical Characteristics for DCS GMSK Mode

Unless otherwise specified: $V_{BATT} = 3.6\text{ V}$, $P_{IN} = +2.0\text{ dBm}$, Pulse Width = 1154 μs , Duty Cycle 25%,
 $Z_{IN} = Z_{OUT} = 50\Omega$, $T_C = 25\text{ }^\circ\text{C}$, $V_{RAMP} = 2.2\text{ V}$, $BS = \text{HIGH}$, $TX_EN = \text{HIGH}$, $V_{MODE} = \text{LOW}$

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency	1710	-	1785	MHz	
Input Power	0	+2	+4	dBm	
Output Power, P_{MAX}	32	33	-	dBm	
Degraded Output Power	29.5	31	-	dBm	$V_{BATT} = 3.2\text{ V}$, $T_C = +85\text{ }^\circ\text{C}$ $P_{IN} = 0\text{ dBm}$
PAE @ P_{MAX}	45	53	-	%	
Forward Isolation 1	-	-40	-30	dBm	$TX_EN = \text{LOW}$, $P_{IN} = +4\text{ dBm}$
Forward Isolation 2	-	-27	-10	dBm	$TX_EN = \text{HIGH}$, $V_{RAMP} = 0.25\text{ V}$, $P_{IN} = +4\text{ dBm}$
Harmonics Second Harmonic ($2F_o$) Third Harmonic ($3F_o$) $4F_o$ to $15F_o$	- - -	-23 -28 -20	-10 -10 -8	dBm	$P_{OUT} \leq 32\text{ dBm}$
Stability (all spurious)	Output Load VSWR = 6:1 All Phases , $P_{OUT} \leq 32\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$, RBW = 3 MHz
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$, RBW = 3 MHz
Ruggedness	No Degradation, No Damage			Load VSWR = 10:1 All Phase Angles; $P_{OUT} \leq 32\text{ dBm}$	
RX Noise Power	-	-87	-78	dBm	$F_{TX} = 1785\text{ MHz}$, RBW = 100 kHz, $F_{RX} = 1805\text{ to }1880\text{ MHz}$, $P_{OUT} \leq 32\text{ dBm}$
Input Return Loss	-	-	2.5:1	VSWR	

Table 12: Electrical Characteristics for PCS GMSK Mode

Unless otherwise specified: $V_{BATT} = 3.6\text{ V}$, $P_{IN} = +2.0\text{ dBm}$, Pulse Width = 1154 μs , Duty Cycle 25%,
 $Z_{IN} = Z_{OUT} = 50\Omega$, $T_C = 25\text{ }^\circ\text{C}$, $V_{RAMP} = 2.2\text{ V}$, BS = HIGH, TX_EN = HIGH, VMODE = LOW

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_o)	1850	-	1910	MHz	
Input Power	0	+2	+4	dBm	
Output Power, P_{MAX}	32	33	-	dBm	
Degraded Output Power	29.5	31	-	dBm	$V_{BATT} = 3.2\text{ V}$, $T_C = +85\text{ }^\circ\text{C}$ $P_{IN} = 0\text{ dBm}$
PAE @ P_{MAX}	45	52	-	%	
Forward Isolation 1	-	-38	-30	dBm	TX_EN = LOW, $P_{IN} = +4\text{ dBm}$
Forward Isolation 2	-	-26	-10	dBm	TX_EN = HIGH, $V_{RAMP} = 0.25\text{ V}$, $P_{IN} = +4\text{ dBm}$
Harmonics Second Harmonic ($2F_o$) Third Harmonic ($3F_o$) 4 F_o to 15 F_o	- - -	-25 -30 -20	-10 -10 -8	dBm	$P_{OUT} \leq 32\text{ dBm}$
Stability (all spurious)	Output Load VSWR = 6:1, All $P_{OUT} \leq 32\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$, RBW = 3 MHz
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$, RBW = 3 MHz
Ruggedness	No Degradation, No Damage				Load VSWR = 10:1, All Phase Angles; $P_{OUT} \leq 32\text{ dBm}$
RX Noise Power	-	-88	-79	dBm	$F_{TX} = 1910\text{ MHz}$, RBW = 100 kHz $F_{RX} = 1930\text{ to }1990\text{ MHz}$, $P_{OUT} \leq 32\text{ dBm}$
Input Return Loss	-	-	2.5:1	VSWR	

Table 13: Electrical Characteristics for DCS EDGE Mode
**Unless otherwise specified: $V_{BATT} = 3.6\text{ V}$, Pulse Width = 1154 μs , Duty Cycle 25%,
 $Z_{IN} = Z_{OUT} = 50\Omega$, $T_C = 25\text{ }^\circ\text{C}$, $BS = \text{HIGH}$, $TX_EN = \text{HIGH}$, $V_{MODE} = \text{HIGH}$**

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_o)	1710	-	1785	MHz	
Linear P_{OUT} (High Power Mode) Linear P_{OUT} (Low Power Mode)	27.5 19	- -	- -	dBm	$V_{BIAS} = \text{High}$ $V_{BIAS} = \text{Low}$
Linear Degraded Output Power LD_P_{OUT} (High Power Mode) ⁽¹⁾ LD_P_{OUT} (Low Power Mode) ⁽²⁾	25 16.5	- -	- -	dBm	Meets ACPR and EVM limits specified under nominal conditions
Linear Gain (High Power Mode)	34	37	40	dB	$V_{BIAS} = \text{High}$
Linear Gain (Low Power Mode)	30	36	40	dB	$V_{BIAS} = \text{Low}$
Gain Variation	-	-0.04	-	dB/ $^\circ\text{C}$	$-20\text{ }^\circ\text{C} \leq T_C \leq +85\text{ }^\circ\text{C}$
Power-Added Efficiency	-	20	-	%	$P_{OUT} = 27.5\text{ dBm}$
I_{CQ} (Low Power Mode)	-	120	-	mA	$V_{BIAS} = \text{Low}$
Error Vector Magnitude (EVM)	-	2	5	%	
Linearity ACPR1 ACPR2 ACPR3	- - -	-39 -65 -78	-33 -58 -64	dBc	$P_{OUT} \leq 27.5\text{ dBm}$, $BW = 30\text{ kHz}$ $F_o \pm 200\text{ kHz}$ $F_o \pm 400\text{ kHz}$ $F_o \pm 600\text{ kHz}$
Harmonics Second Harmonic ($2F_o$) Third Harmonic ($3F_o$) $4F_o$ to $7F_o$	- - -	-38 -47 -20	-20 -20 -10	dBm	$P_{OUT} \leq 27.5\text{ dBm}$
Stability (all spurious)	Output Load VSWR = 6:1 All Phases, $P_{OUT} \leq 27.5\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$, $RBW = 3\text{ MHz}$
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$, $RBW = 3\text{ MHz}$
Ruggedness	No Degradation, No Damage			Load VSWR = 10:1, All Phase Angles; $P_{OUT} \leq 27.5\text{ dBm}$	
RX Noise Power	-	-81	-76	dBm	$F_{TX} = 1785\text{ MHz}$, $RBW = 100\text{ kHz}$ $F_{RX} = 1805\text{ to }1880\text{ MHz}$ $P_{OUT} \leq 27.5\text{ dBm}$
Input Return Loss	-	-	2.5:1	VSWR	

Notes:

(1) $V_{BIAS} = \text{High}$, $V_{BATT} = \text{Range}$ ($3.2\text{ V} \leq V_{BATT} \leq 4.5\text{ V}$), $Temp = \text{Range}$ ($-20\text{ }^\circ\text{C} \leq T_C \leq +85\text{ }^\circ\text{C}$).

(2) $V_{BIAS} = \text{Low}$, $V_{BATT} = \text{Range}$ ($3.2\text{ V} \leq V_{BATT} \leq 4.5\text{ V}$), $Temp = \text{Range}$ ($-20\text{ }^\circ\text{C} \leq T_C \leq +85\text{ }^\circ\text{C}$).

Table 14: Electrical Characteristics for PCS EDGE Mode
**Unless otherwise specified: $V_{BATT} = 3.6\text{ V}$, Pulse Width = 1154 μs , Duty Cycle 25%,
 $Z_{IN} = Z_{OUT} = 50\Omega$, $T_C = 25\text{ }^\circ\text{C}$, BS = HIGH, TX_EN = HIGH, VMODE = HIGH**

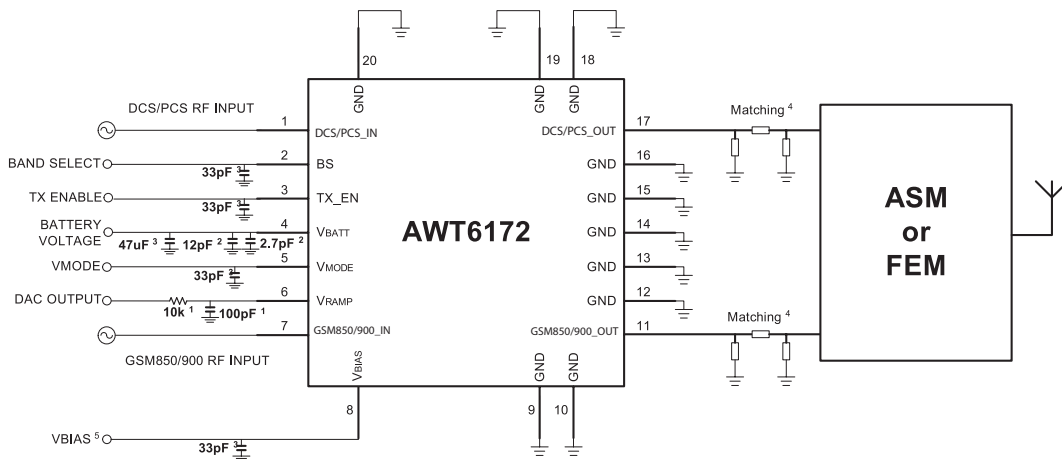
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_o)	1850	-	1910	MHz	
Linear P _{OUT} (High Power Mode) Linear P _{OUT} (Low Power Mode)	27.5 19	- -	- -	dBm	V _{BIAS} = High V _{BIAS} = Low
Linear Degraded Output Power Ld_P _{OUT} (High Power Mode) ⁽¹⁾ Ld_P _{OUT} (Low Power Mode) ⁽²⁾	25 16.5	- -	- -	dBm	Meets ACPR and EVM limits specified under nominal conditions
Linear Gain (High Power Mode)	33.0	36	39.5	dB	V _{BIAS} = High
Linear Gain (Low Power Mode)	29	35	39	dB	V _{BIAS} = Low
Gain Variation	-	-0.044	-	dB/°C	-20 °C ≤ T _c ≤ +85 °C
Power-Added Efficiency	-	20	-	%	P _{OUT} = 27.5 dBm
I _{cq} (Low Power Mode)	-	120	-	mA	V _{BIAS} = Low
Error Vector Magnitude (EVM)	-	2	5	%	
Linearity ACPR1 ACPR2 ACPR3	- - -	-38 -64 -77	-33 -57 -64	dBc	P _{OUT} ≤ 27.5 dBm, BW = 30 kHz F _o ± 200 kHz F _o ± 400 kHz F _o ± 600 kHz
Harmonics Second Harmonic (2F _o) Third Harmonic (3F _o) 4F _o to 15F _o	- - -	-40 -46 -20	-20 -20 -10	dBm	P _{OUT} ≤ 27.5 dBm
Stability (all spurious)	Output Load VSWR = 6:1 All Phases, P _{OUT} ≤ 27.5 dBm				
	-	-	-36	dBm	F _{OUT} < 1 GHz, RBW = 3 MHz
	-	-	-30	dBm	F _{OUT} > 1 GHz, RBW = 3 MHz
Ruggedness	No Degradation, No Damage			Load VSWR = 10:1, All Phase Angles; P _{OUT} ≤ 27.5 dBm	
RX Noise Power	-	-82	-76	dBm	F _{TX} = 1910 MHz, RBW = 100 kHz F _{RX} = 1930 to 1990 MHz P _{OUT} ≤ 27.5 dBm
Input Return Loss	-	-	2.5:1	VSWR	

Notes:

(1) V_{BIAS} = High, V_{BATT} = Range (3.2 V ≤ V_{BATT} ≤ 4.5 V), Temp = Range (-20 °C ≤ T_c ≤ +85 °C).(2) V_{BIAS} = Low, V_{BATT} = Range (3.2 V ≤ V_{BATT} ≤ 4.5 V), Temp = Range (-20 °C ≤ T_c ≤ +85 °C).

AWT6172

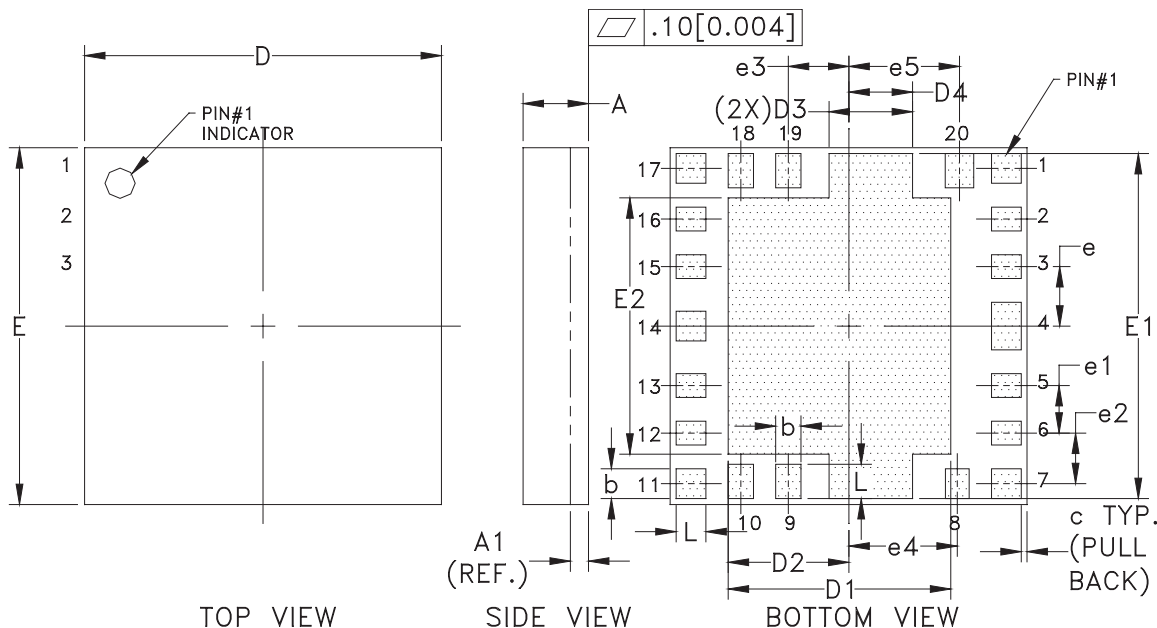
APPLICATION INFORMATION



- 1) Component values depends on baseband chipset used.
- 2) This component should be placed as close to the device pin as possible.
- 3) These components are recommended as good design practice for improving noise rejection characteristics. The values specified are not critical as they may not be required in the final application.
- 4) Actual matching component values depend on PCB layout and ASM/FEM used.
- 5) VBIAS can be controlled by either using a digital control signal or be connected to VRAMP.

Figure 3: Recommended Application Circuit

PACKAGE OUTLINE



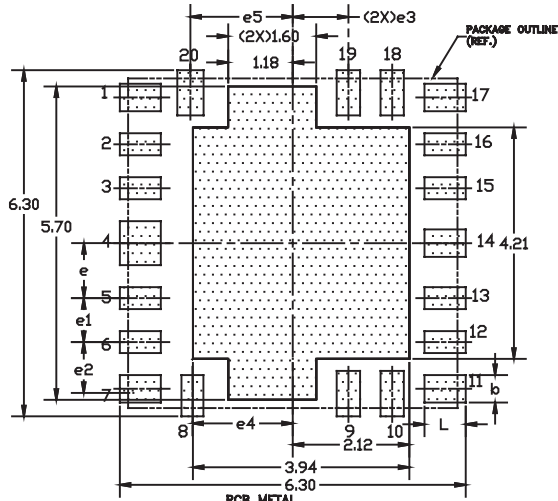
SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.84	0.98	1.12	0.033	0.038	0.044	—
A1	0.32 (REF.)			0.013 (REF.)			—
b	SEE TERMINAL CHART			SEE TERMINAL CHART			—
c	—	0.10	—	—	0.004	—	—
D	5.88	6.00	6.12	0.231	0.236	0.240	—
D1	3.65	3.73	3.80	0.143	0.147	0.150	—
D2	1.95	2.03	2.10	0.077	0.080	0.083	—
D3	1.31	1.39	1.46	0.051	0.055	0.057	2X
D4	0.98	1.06	1.13	0.038	0.042	0.044	—
E	5.88	6.00	6.12	0.231	0.236	0.240	—
E1	5.71	5.79	5.86	0.224	0.228	0.230	—
E2	4.23	4.31	4.38	0.166	0.170	0.172	—
e	1.00			0.039			4X
e1	0.80			0.031			6X
e2	0.85			0.033			4X
e3	1.02			0.040			2X
e4	1.82			0.071			—
e5	1.86			0.073			—
L	SEE TERMINAL CHART			SEE TERMINAL CHART			—

NOTES:

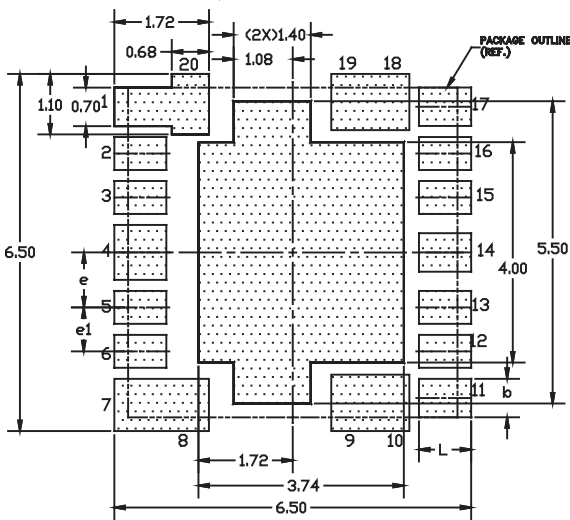
- CONTROLLING DIMENSIONS: MILLIMETERS
- UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
- PITCH ("e") DIMENSION INFORMATION:
 - * e (4X) (CENTER OF PACKAGE) TERMINAL #'s 4 to 3, 4 to 5, 14 to 15 and 14 to 13.
 - * e1 (6X) TERMINAL #'s 5 to 6, 9 to 10, 12 to 13, 15 to 16, 18 to 19 and 2 to 3.
 - * e2 (4X) TERMINAL #'s 6 to 7, 11 to 12, 16 to 17 and 1 to 2.
 - * e3 (2X) CENTER OF PACKAGE to TERMINAL #'s 9 and 19.
 - * e4 CENTER OF PACKAGE to TERMINAL #8.
 - * e5 CENTER OF PACKAGE to TERMINAL #20.
- TOLERANCE FOR b AND L DIMENSIONS=±0.03[0.001]

TERMINAL #	SYMBOL b	SYMBOL L
	NOMINAL - MILLIMETERS [INCHES]	
1-7-11-14-17	0.50[0.020]	0.50[0.020]
2-3-5-6-8 12-13-15-16	0.40[0.016]	0.50[0.020]
9-10-18-19	0.42[0.017]	0.58[0.023]
4	0.80[0.031]	0.50[0.020]
20	0.48[0.019]	0.58[0.023]

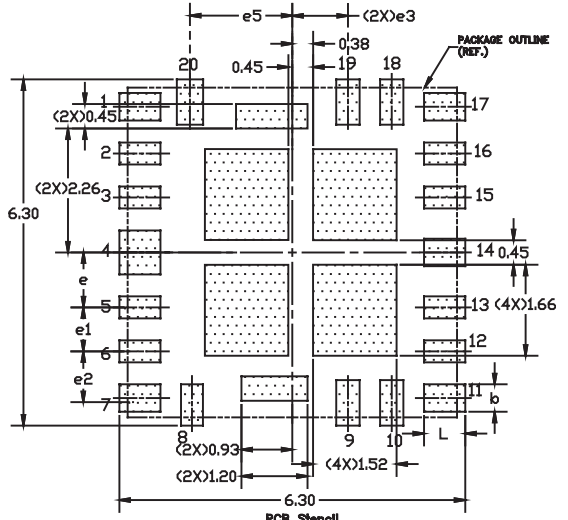
Figure 4: M33 Package Outline - 20 Pin 6 mm x 6 mm x 1.1 mm Surface Mount Module



PCB METAL
TOP (X-RAY) VIEW
ONLY PACKAGE I/O'S AND
GROUND REQUIREMENTS
SHOWN.



PCB SOLDER MASK
TOP (X-RAY) VIEW



PCB Stencil
TOP (X-RAY) VIEW
ONLY PACKAGE I/O'S AND
GROUND REQUIREMENTS
SHOWN.

NOTES:

- (1) OUTLINE DRAWING REFERENCE:
98000-075
- (2) UNLESS SPECIFIED DIMENSIONS
ARE SYMMETRICAL ABOUT CENTER
LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.

Figure 5: Recommended PCB Footprint

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE= $\pm 0.076[0.003]$.
3. PITCH ("e") DIMENSION INFORMATION:
 - * e (4X) (CENTER OF PACKAGE) TERMINAL #'s 4 to 3,
4 to 5, 14 to 15 and 14 to 13.
 - * e1 (6X) TERMINAL #'s 5 to 6, 9 to 10, 12 to 13,
15 to 16, 18 to 19 and 2 to 3.
 - * e2 (4X) TERMINAL #'s 6 to 7, 11 to 12, 16 to 17
and 1 to 2.
 - * e3 (2X) CENTER OF PACKAGE to TERMINAL #'s 9 AND 19.
 - * e4 CENTER OF PACKAGE to TERMINAL #8.
 - * e5 CENTER OF PACKAGE to TERMINAL #20.

PCB Metal & Stencil Aperture

TERMINAL #	SYMBOL b	SYMBOL L
	NOMINAL - MILLIMETERS	INCHES
1-7-11-14-17	0.50[0.020]	0.75[0.029]
2-3-5-6 12-13-15-16	0.40[0.016]	0.75[0.029]
9-10-18-19	0.825[0.032]	0.425[0.017]
4	0.80[0.031]	0.75[0.029]
8	0.75[0.029]	0.40[0.016]
20	0.825[0.032]	0.48[0.019]

PCB Solder Mask

TERMINAL #	SYMBOL b	SYMBOL L
	NOMINAL - MILLIMETERS	INCHES
11-14-17	0.700[0.028]	0.950[0.037]
2-3-5-6 12-13-15-16	0.600[0.024]	0.950[0.037]
18/19	1.000[0.039]	1.420[0.056]
4	1.000[0.039]	0.950[0.037]
7/8	0.950[0.037]	1.720[0.068]
9/10	1.000[0.039]	1.420[0.056]

Symbol	MILLIMETERS	INCHES
e	1.00	0.039
e1	0.80	0.031
e2	0.85	0.033
e3	1.02	0.040
e4	1.82	0.071
e5	1.86	0.073

Figure 5B: Recommended PCB Footprint Notes

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT6172RM33P8	-20 °C to +85°C	RoHS-compliant 20 Pin 6 mm x 6 mm x 1.1 mm Surface Mount Module	Tape and Reel, 2500 pieces per reel
AWT6172RM33P9	-20 °C to +85°C	RoHS-compliant 20 Pin 6 mm x 6 mm x 1.1 mm Surface Mount Module	Partial Tape and Reel
AWT6172HM33P8	-20 °C to +85°C	Halogen-free and RoHS-compliant 20 pin 6mm x 6mm x 1.1mm Surface Mount Module	Tape and Reel, 2500 pieces per reel
AWT6172HM33P9	-20 °C to +85°C	Halogen-free and RoHS-compliant 20 pin 6mm x 6mm x 1.1mm Surface Mount Module	Partial Tape and Reel

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