Voltage Comparator

AVAILABLE AS MILITARY / SPACE SPECIFICATIONS

- SMD 5962-00524 pending
- Radiation Tolerant
- MIL-STD-883, 1.2.1 "QML" pending

FEATURES

- Operates from single 5V supply
- Radiation Guaranteed to 100K RADS TID
- Input current: 200 nA max. over temperature
- Offset current: 20 nA max. over temperature
- WIDE Differential input voltage range: ±30V
- Typical Power consumption: 135 mW at ±15V

OPTIONS MARKINGS

• Packages	
8 pin Ceramic DIP	C008
10 pin Cerpack(flatpak)	CP10
10 pin Cerpack Gullwing	GW10
8 Lead Metal Can	TO99
• Process / Temperature Ranges	
MILITARY (-55°C to +125°C)	/XT
MIL-STD-883 paragraph 1.2.1	/883
MIL-STD-883 CLASS 'S'	/SPACE

GENERAL DESCRIPTION

The AS111 is a voltage comparator that has input currents nearly a thousand times lower than other similar devices. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the AS111 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than some devices (200 ns response time vs 40 ns), this device is also much less prone to spurious oscillations.

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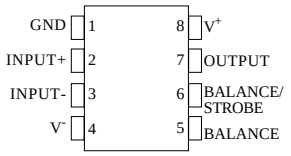
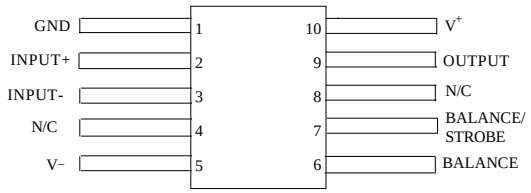
PIN ASSIGNMENT

(Top View)

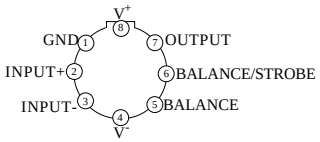
8 Pin Ceramic DIP (C008)



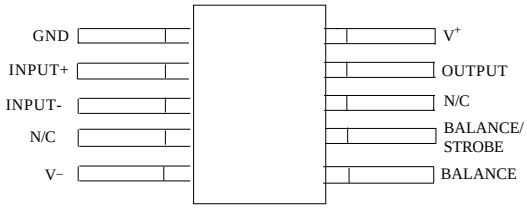
10 Pin CerPack flatpak(CP10)



8 Lead Metal Can (TO99)

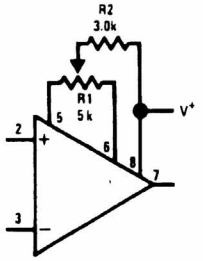


10 Pin CerPack Gullwing(GW10)

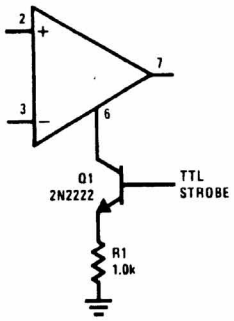


TYPICAL APPLICATIONS[3]

Offset Balancing

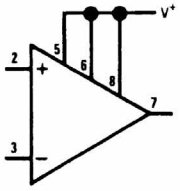


Strobing



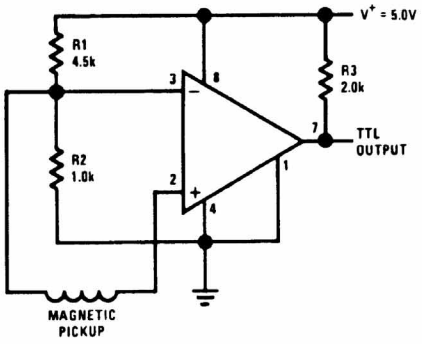
Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

Increasing Input Stage Current (Note 1)

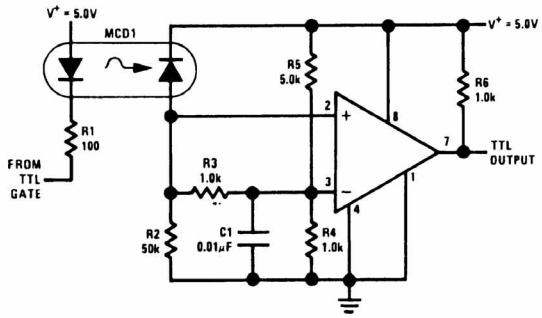


Note 1: Increases typical common mode slew from 7.0V/µs to 18V/µs.

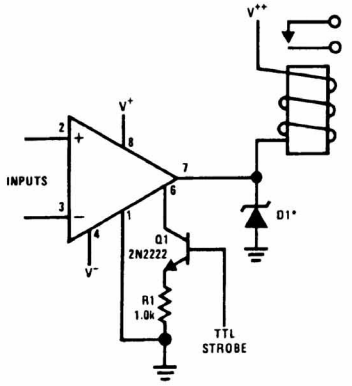
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe

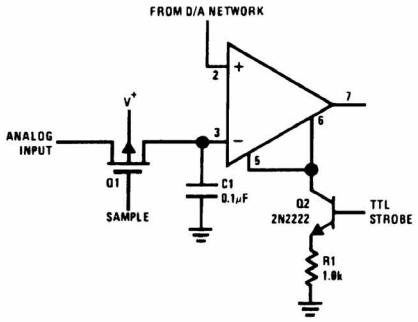


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

Note: Do Not Ground Strobe Pin.

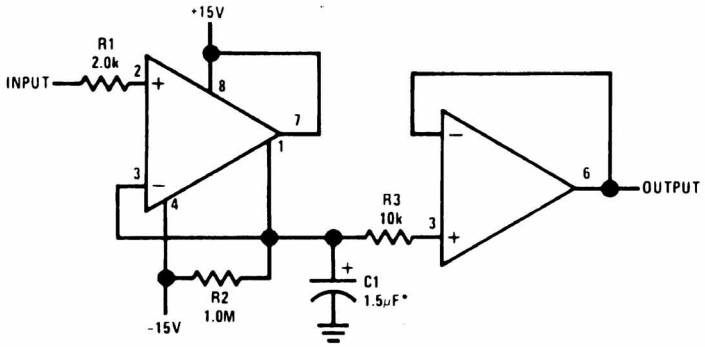
TYPICAL APPLICATIONS (CONTINUED)[3]

Strobing off Both Input and Output Stages (Note 2)

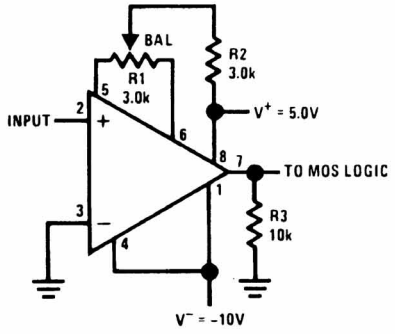


NOTE: Do Not Ground Strobe Pin
NOTE 2: Typical input current is 50pV with inputs strobed off.
NOTE 3: Pin connections shown on schematic diagram and typical applications are for TO08 metal can package.

Positive Peak Detector



Zero Crossing Detector Driving MOS Logic



*Solid tantalum

ABSOLUTE MAXIMUM RATINGS*,[5]

Operating Temperature Range ..... -55C ≤ Ta ≤ +125C
Maximum Junction Temperature ..... +175C
Storage Temperature Range ..... -65C ≤ Ta ≤ +150C
Lead Temperature (soldering for 60 sec) 300C
Total Supply Voltage (V_{84})..... 36V
Output to Negative Supply Voltage (V_{74})..... 50V
Ground to Negative Supply Voltage (V_{14})..... 30V
Differential Input Voltage..... ±30V
Input Voltage[4]..... ±15V
Output Short Circuit Duration..... 10 sec
Lead Temperature (Soldering, 10 sec)..... 260°C
Voltage at Stobe Pin..... V^+ -5V
Maximum Strobe Current 10mA
Sink Current 50mA
Package Weight:
10 Lead Cerpack Flatpak 240mg
10 Lead Cerpack Gullwing 220mg
8 Lead Metal Can 950mg
8 Lead Cerdip 1100mg

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 4: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
Note 5: The maximum junction temperature of the AS111 is 175°C. For operating at elevated temperatures, devices in the TO08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 50°C/W, junction to case. The thermal resistance of the C008 dual-in-line package is 130°C/W, junction to ambient, and 20°C/W Junction to Case. The thermal resistance of the CP10 Cerpack Flatpak & the GW10 Cerpack Gullwing are 230°C/W for juntion to ambient and 25°C/W Junction to Case. These figures are based on Still Air & 1/2 Watt power dissipation.

(The following Table applies to the Subgroup column in the Electrical Characteristics Tables)

SUBGROUP	Description	TEMP(°C)
1	Static DC tests	+25
2	Static DC tests	+125
3	Static DC tests	-55
4	Dynamic Tests	+25
5	Dynamic Tests	+125
6	Dynamic Tests	-55
7	Functional Tests	+25
8	Functional Tests	+125
9	Functional Tests	-55

Electrical Characteristics

DC PARAMETERS: (SEE NOTE 8)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = +2.5V, -Vcc = -2.5V, Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
Vio(R)	Raised Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
Iio	Input Offset Current	Vin = 0V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
Iio(R)	Raised Input Offset Current	Vin = 0V, Rs = 50K Ohms			-25	+25	nA	1, 2
					-50	+50	nA	3
Iib+	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-100	0.1	nA	1, 2
					-150	0.1	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3

Electrical Characteristics

DC PARAMETERS: (SEE NOTE 8) (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iib-	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-100	0.1	nA	1, 2
					-150	0.1	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
Vo(STB)	Collector Output Voltage (ST)	Vin+ = Gnd, Vin- = 15V, Istb = -3mA, Rs = 50 Ohms	1		14		V	1, 2, 3
CMR	Common Mode Rejection	-28V≤-Vcc≤-0.5V, Rs=50 Ohms, 2V≤+Vcc≤29.5V, Rs=50 Ohms, -14.5V≤Vcm≤13V,Rs=50 Ohms			80		dB	1, 2, 3
Vol	Low Level Output Voltage	+Vcc = 4.5V, -Vcc = Gnd, Iout = 8mA, ±Vin = 0.5V, Vid = -6mV				0.4	V	1, 2, 3
		+Vcc = 4.5V, -Vcc = Gnd, Iout = 8mA, ±Vin = 3V, Vid = -6mV				0.4	V	1, 2, 3
		Iout = 50mA, ±Vin = 13V, Vid = -5mV				1.5	V	1, 2, 3
		Iout = 50mA, ±Vin = -14V, Vid = -5mV				1.5	V	1, 2, 3
Icex	Output Leakage Current	+Vcc = 18V, -Vcc = -18V, Vout = 32V			-1	10	nA	1
					-1	500	nA	2
Ii	Input Leakage Current	+Vcc = 18V, -Vcc = -18V, +Vin = +12V, -Vin = -17V	7		-5	500	nA	1, 2, 3
		+Vcc = 18V, -Vcc = -18V, +Vin = -17V, -Vin = +12V	7		-5	500	nA	1, 2, 3
Icc+	Power Supply Current					6	mA	1, 2
						7	mA	3
Icc-	Power Supply Current				-5		mA	1, 2
					-6		mA	3
Delta Vio/Delta T	Temperature Coefficient Input Offset Voltage	25 C ≤ T ≤ 125 C			-25	25	uV/C	2
		-55 C ≤ T ≤ 25 C			-25	25	uV/C	3
Delta Iio/Delta T	Temperature Coefficient Input Offset Current	25 C ≤ T ≤ 125 C			-100	100	pA/C	2
		-55 C ≤ T ≤ 25 C			-200	200	pA/C	3

Electrical Characteristics

DC PARAMETERS: (SEE NOTE 8) (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ios	Short Circuit Current	Vout = 5V, t ≤ 10mS, Vin- = 0.1V, Vin+ = 0V	3, 5			200	mA	1
			3, 5			150	mA	2
			3, 5			250	mA	3
Vio(adj)+	Input Offset Voltage (Adjustment)	Vout = 0V, Vin = 0V, Rs = 50 Ohms	3		5		mV	1
Vio(adj)-	Input Offset Voltage (Adjustment)	Vout = 0V, Vin = 0V, Rs = 50 Ohms	3			-5	mV	1
Ave+	Voltage Gain (Emitter)	Rl = 600 Ohms	3, 6		10		V/mV	4
			3, 6		8		V/mV	5, 6
Ave-	Voltage Gain (Emitter)	Rl = 600 Ohms	3, 6		10		V/mV	4
			3, 6		8		V/mV	5, 6

AC PARAMETERS: (SEE NOTE 8)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: ±Vcc = ±15V, Vcm = 0

trLHC	Response Time (Collector Output)	Vod(Overdrive) = -5mV, Cl = 50pF, Vin = -100mV	4			300	nS	7, 8B
			4			640	nS	8A
trHLC	Response Time (Collector Output)	Vod(Overdrive) = 5mV, Cl = 50pF, Vin = 100mV	4			300	nS	7, 8B
			4			500	nS	8A

Electrical Characteristics

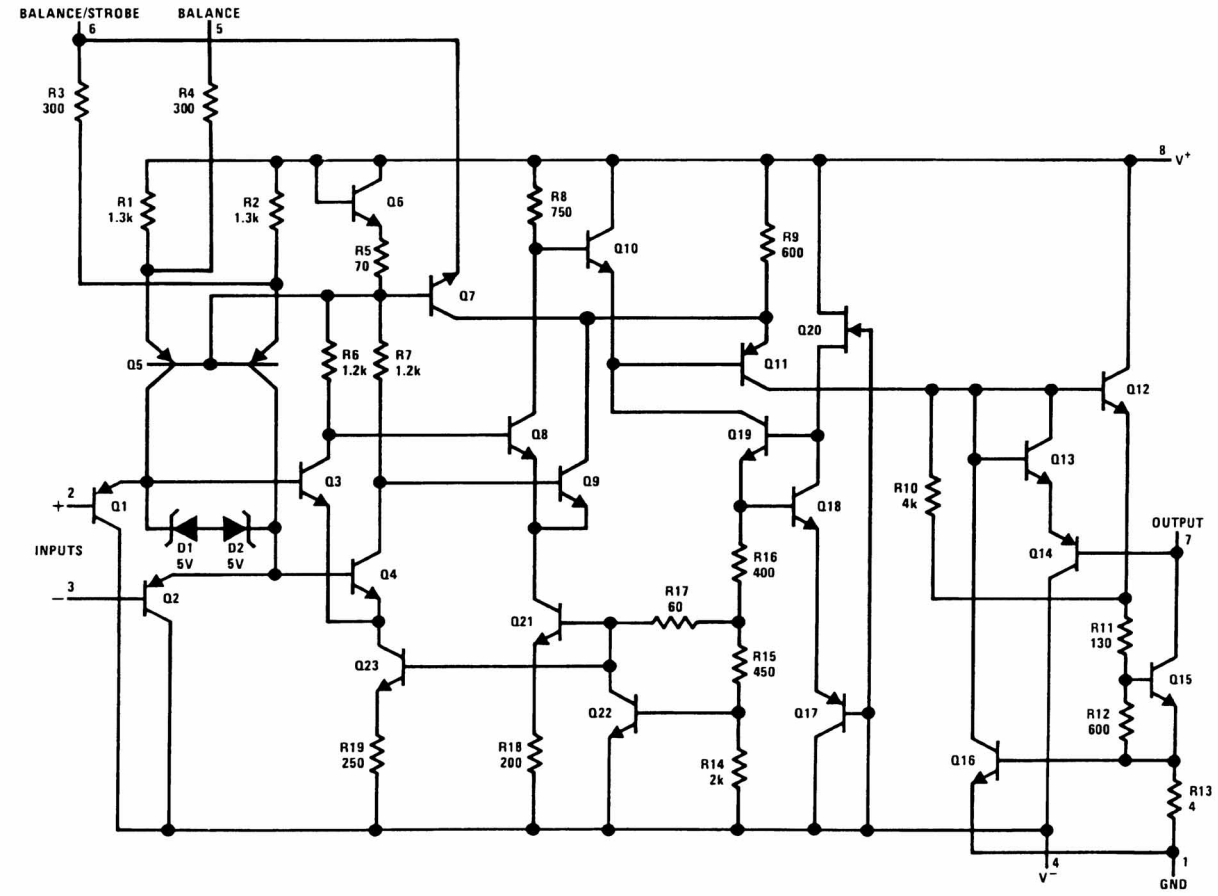
DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V. "Delta calculations performed on /SPACE devices at group B, subgroup 5 only".

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-0.5	0.5	mV	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-0.5	0.5	mV	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-0.5	0.5	mV	1
Iib+	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-12.5	12.5	nA	1
Iib-	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-12.5	12.5	nA	1
Icex	Output Leakage Current	+Vcc = 18V, -Vcc = -18V, Vout = 32V			-5	5	nA	1

Note 1: Istb = -2mA at -55 C.
Note 2: Calculated parameter.
Note 3: Use DC tape for Ios and Vio(adj), Ave+ and Ave- as indicated in TAPE NAME section of this JRETS.
Note 4: Uses AC tape and hardware.
Note 5: Actual min. limit used is 5mA due to test setup.
Note 6: Datalog reading in K = V/mV.
Note 7: Vid is voltage difference between inputs.
Note 8: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiaton end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5, Condition A.

Schematic Diagram[20]



NOTE 20: Pin connections shown on schematic diagram are for the TO08 can package.

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the AS111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kW to 100 kW), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the AS111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 1 below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in Figure 1.

2. Certain sources will produce a cleaner comparator out put waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.

3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.

(continued)

APPLICATION HINTS (CONTINUED)

4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S=10 kW, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only(second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the AS111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the AS111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the AS111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)

6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of Figure 2, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of Figure 3 could be used, but it is rather awkward. See the notes in paragraph 7 below.

7. When both inputs of the AS111 are connected to active signals, or if a high-impedance signal is driving the positive input of the AS111 so that positive feedback would be disruptive, the circuit of Figure 1 is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.

8. These application notes apply specifically to the AS111 family of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).

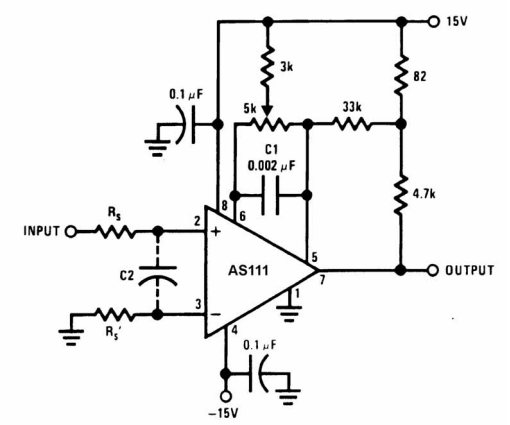


FIGURE 1. Improved Positive Feedback

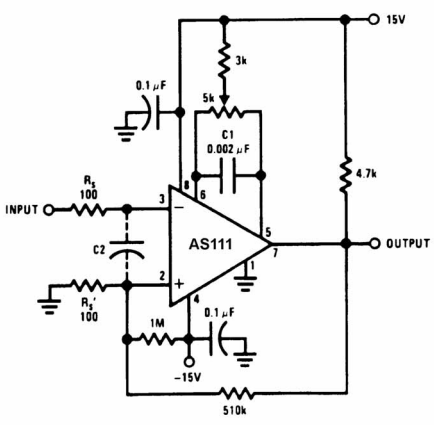


FIGURE 2. Conventional Positive Feedback

NOTE: Pin connections shown are for the TO08 can package.

APPLICATION HINTS (CONTINUED)

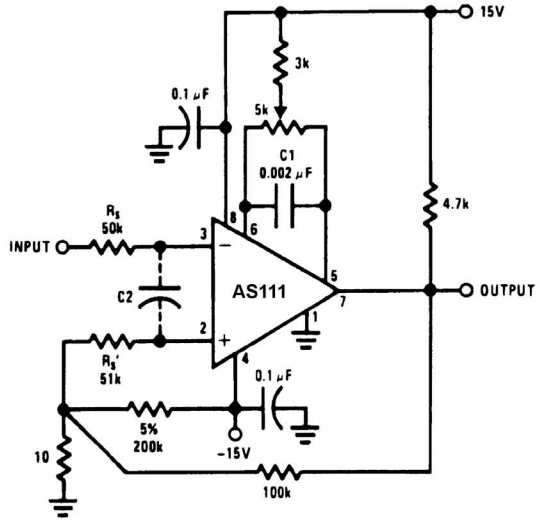
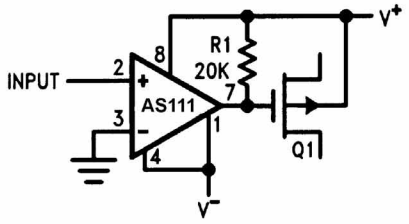


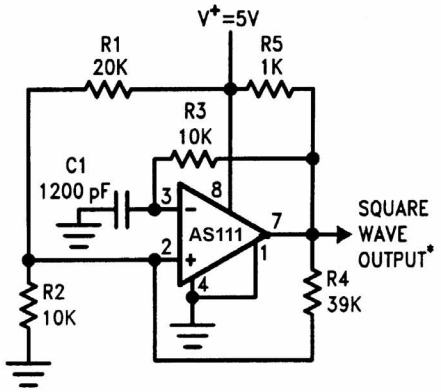
FIGURE 3. Positive Feedback with High Source Resistance

TYPICAL APPLICATIONS (Pin numbers refer to TO08 can package)

Zero Crossing Detector Driving MOS Switch



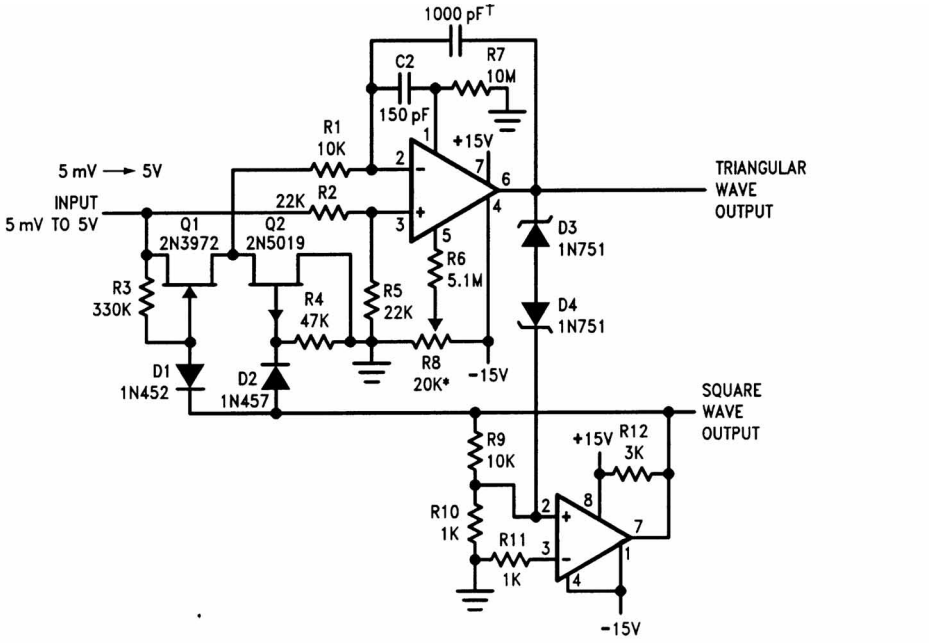
100 kHz Free Running Multivibrator



*TTL or DTL fanout of two

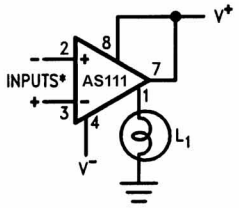
TYPICAL APPLICATIONS (Pin numbers refer to TO08 can package)(Continued)

10Hz to 10kHz Voltage Controlled Oscillator

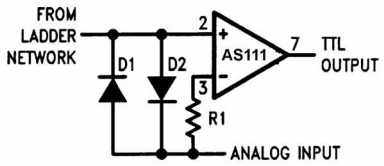


*Adjust for symmetrical square wave time when V_{IN} = 5 mV
†Minimum capacitance 20 pF Maximum frequency 50 kHz

Driving Ground-Referred Load

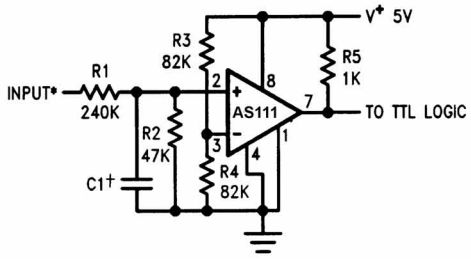


Using Clamp Diodes to Improve Response



*Input polarity is reversed when using pin 1 as output.

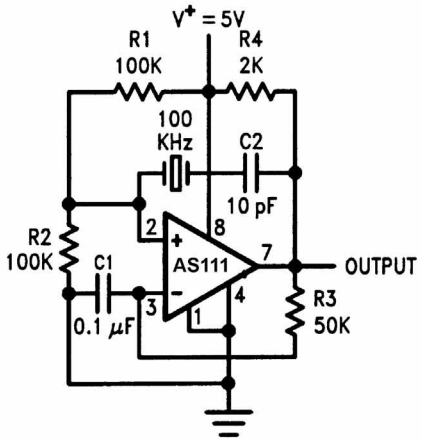
TTL Interface with High Level Logic



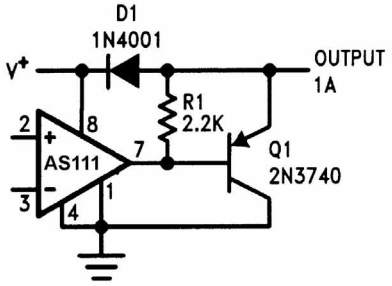
*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptibility to noise spikes.

TYPICAL APPLICATIONS (Pin numbers refer to TO08 can package)(Continued)

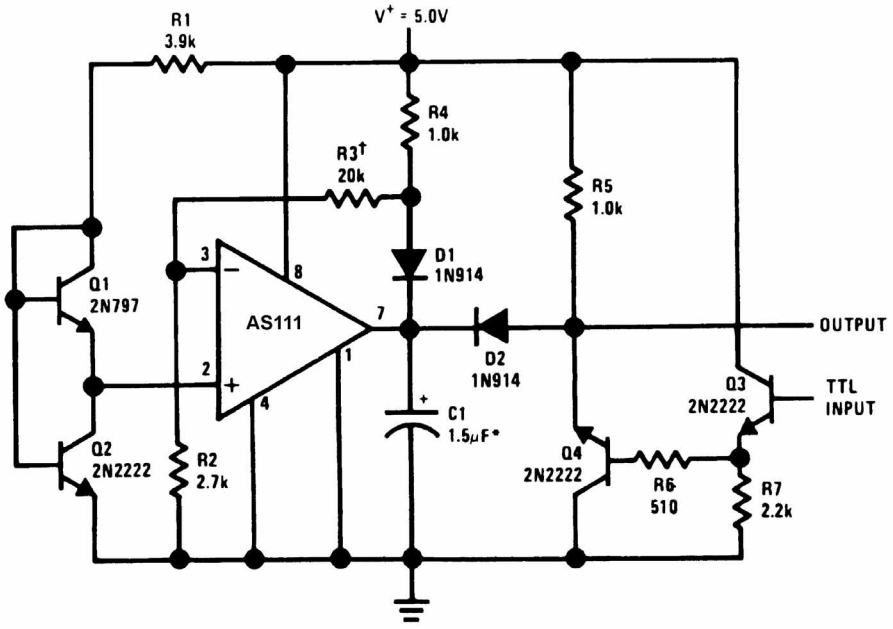
Crystal Oscillator



Comparator and Solenoid Driver

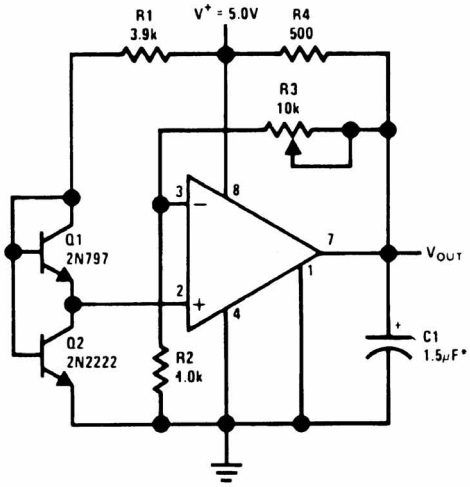


Precision Squarer



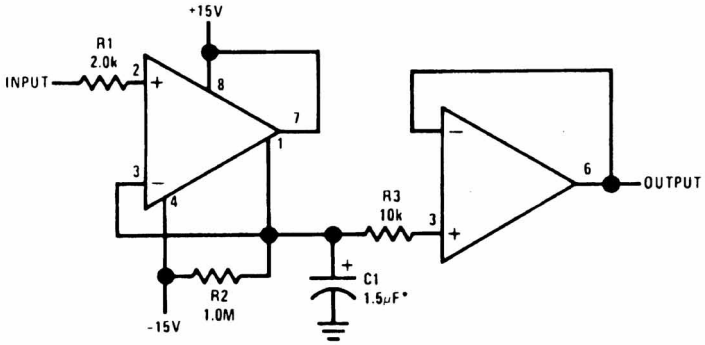
TYPICAL APPLICATIONS (Pin numbers refer to TO08 can package)(Continued)

Low Voltage Adjustable Reference Supply

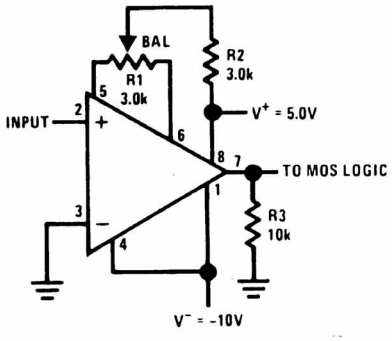


*Solid tantalum

Positive Peak Detector

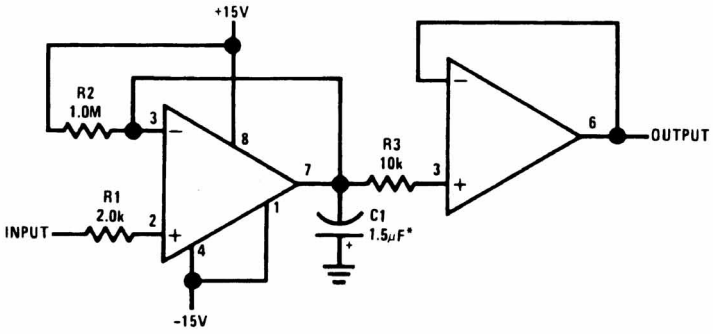


Zero Crossing Detector Driving MOS Logic



*Solid tantalum

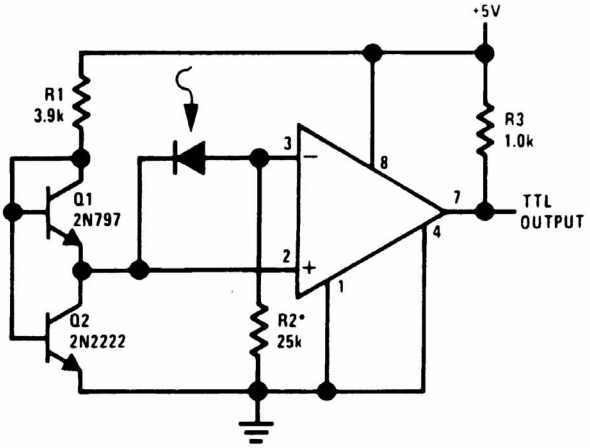
Negative Peak Detector



*Solid tantalum

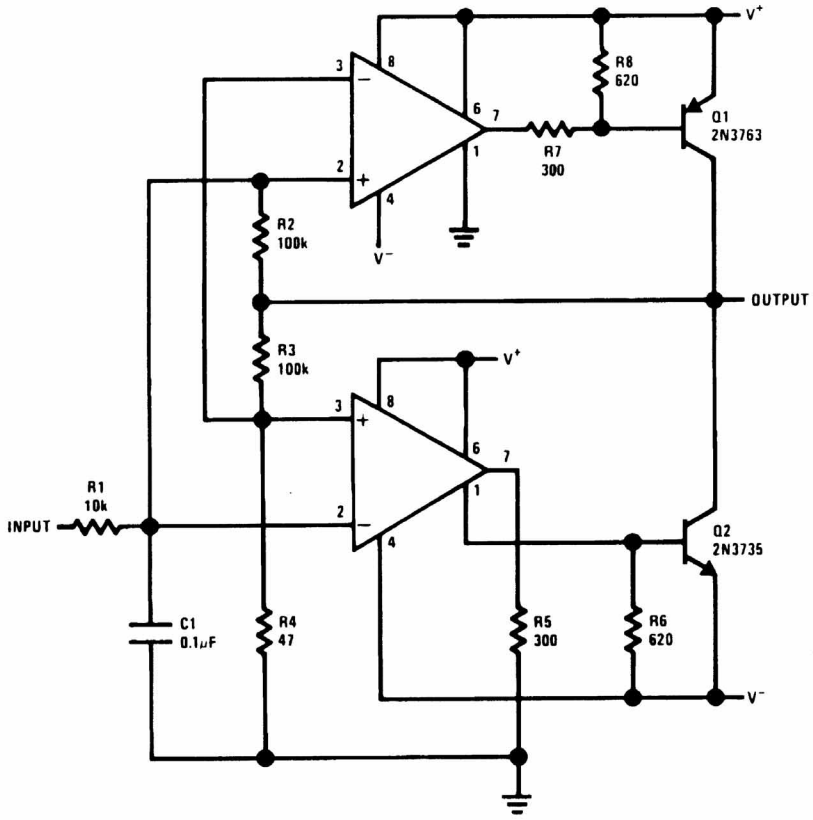
TYPICAL APPLICATIONS (Pin numbers refer to TO08 can package)(Continued)

Precision Photodiode Comparator



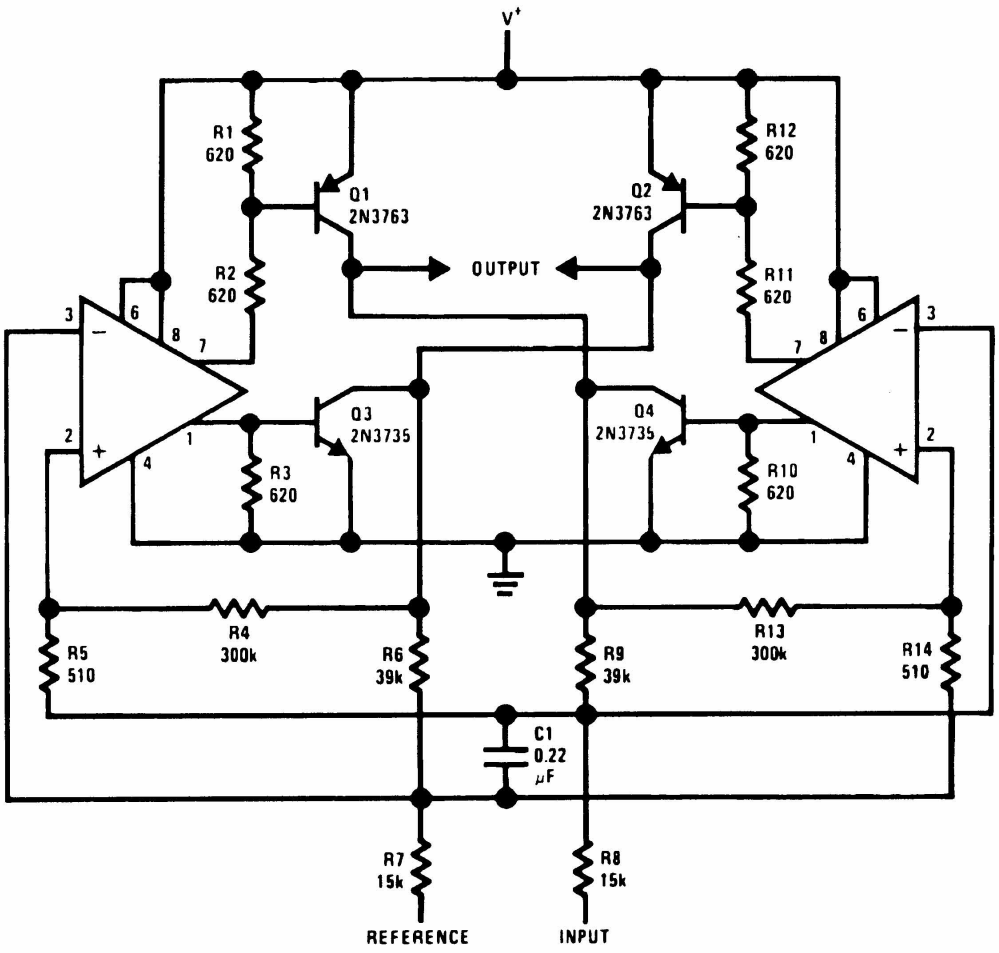
*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

Switching Power Amplifier



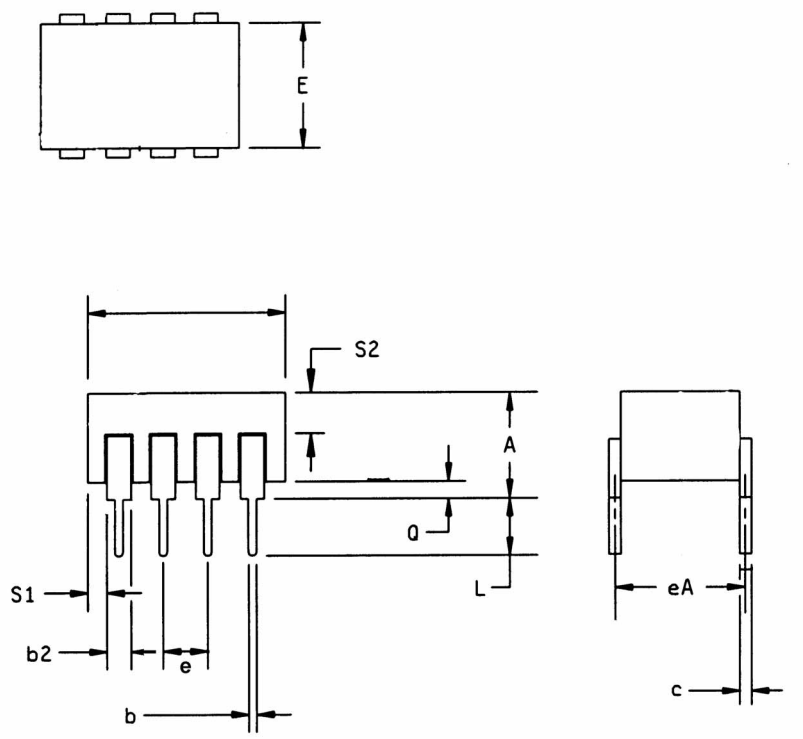
TYPICAL APPLICATIONS (Pin numbers refer to TO08 can package)(Continued)

Switching Power Amplifier



MECHANICAL DEFINITIONS*

ASI Case (Package Designator C008)
SMD 5962-00524, Case Outline P (GDIP1-T8)



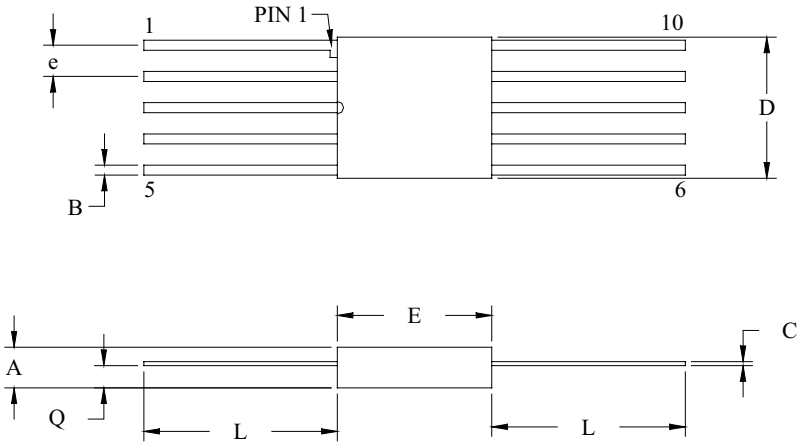
SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	---	0.200
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	0.405
E	0.220	0.310
e	0.100 BCS	
eA	0.300 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	---
S2	0.005	---

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case (Package Designator CP10)
SMD 5962-00524, Case Outline H

MIL-STD-1835 outline drawing GDFP1-F10



	Min	Max
A	.045	.085
B	.010	.022
C	.004	.009
D	.226	.251
E	.235	.260
e	.050 BSC	
L	.250	.370
Q	.026	.045

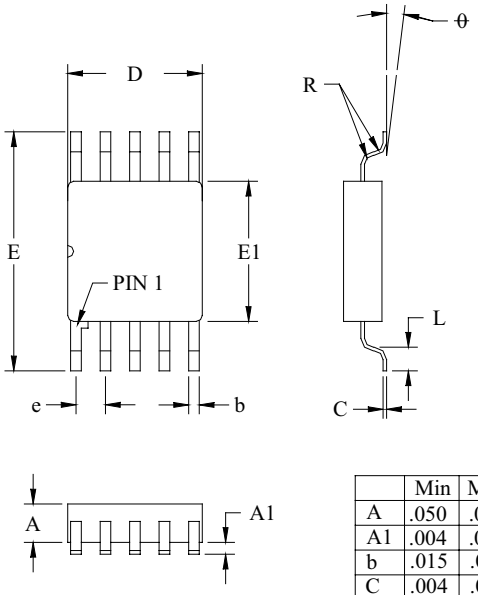
Notes:
1. Lead Finish: Solder dipped with Sn 60 or Sn63 solder conforming to MIL-PRF-38535 to a min thickness of 200 micro-inches. Solder may be applied over lead base metal or Sn plate. Max limit may be increased by .003 inches after lead finish applied.
2. Lead 1 identification shall be:
a) A notch or other mark within this area.
b) a TAB on lead 1, either side.

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case (Package Designator GW10)
SMD 5962-00524, Case Outline Z

MIL-STD-1835 outline drawing GDFP1-G10



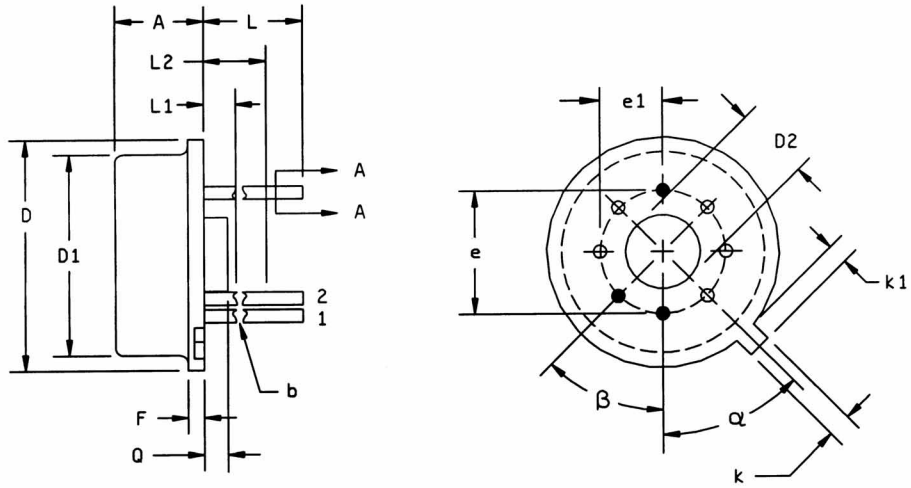
	Min	Max
A	.050	.080
A1	.004	.012
b	.015	.022
C	.004	.009
D	.228	.253
E	.400	.420
E1	.235	.260
e	.050 BSC	
L	.037	.043
R	.013	.017
θ	0	7

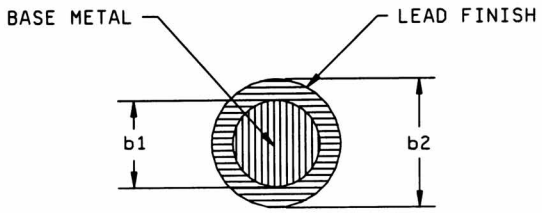
Notes:
1. Lead Finish: Solder dipped with Sn 60 or Sn63 solder conforming to MIL-PRF-38535 to a min thickness of 200 micro-inches. Solder may be applied over lead base metal or Sn plate. Max limit may be increased by .003 inches after lead finish applied.
2. Lead 1 identification shall be:
a) A notch or other mark within this area.
b) a TAB on lead 1, either side.

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case (Package Designator TO08)
SMD 5962-86877, Case Outline G





SECTION A-A

SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	0.165	0.185
b	0.016	0.019
b1	0.016	0.021
b2	0.016	0.024
D	0.335	0.375
D1	0.305	0.335
D2	0.110	0.160
e	0.200 BSC	
e1	0.100 BSC	
F	---	0.040
k	0.027	0.034
k1	0.027	0.045
L	0.500	0.750
L1	---	0.050
L2	0.250	---
Q	0.010	0.045
α	45° BSC	
β	45° BSC	

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: AS111C008/XT

Device Number	RAD Level	Package Type	Process
AS111	P,R, or blank	C008	/*

EXAMPLE: AS111PCP10/883C

Device Number	RAD Level	Package Type	Process
AS111	P,R, or blank	CP10	/*

EXAMPLE: AS111PGW10/SPACE

Device Number	RAD Level	Package Type	Process
AS111	P,R, or blank	GW10	/*

EXAMPLE: AS111RTO99/SPACE

Device Number	RAD Level	Package Type	Process
AS111	P,R or blank	TO99	/*

+ RADIATION Levels:
BLANK = No Radiation Guarantee
P = 30K Rads(Si) Total Dose
R = 100K Rads(Si) Total Dose

***AVAILABLE PROCESSES:**

XT = Extended Temperature Range -55°C to +125°C
/883C = MIL-STD-883 paragraph 1.2.1 -55°C to +125°C
/SPACE = MIL-STD-883 para 1.2.1 -55°C to +125°C

NOTE: ASI supports Customer specified drawings (SCDs), please contact your SALES or Factory Representative for information.

ASI TO DSCC PART NUMBER CROSS REFERENCE

ASI PART NUMBER	DSCC PART NUMBER

DSCC part numbers pending , contact your ASI Sales or factory rep for updated status.

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*