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AK4691

4ch ADC + 2ch DAC with MIC/HP/SPK-AMP

GENERAL DESCRIPTION

The AK4691 is a 16bit, 4ch ADC and 2ch DAC with Microphone-Amplifier, Headphone-Amplifier, and Speaker-Amplifier. The recording block corresponds to supports 4-channel inputs, and also has 3-input selector for Internal/External MIC and LINE, output power for Microphone, Pre-Amp, and ALC (Automatic Level Control) circuit. The playback bock has Lineout-Amplifier, Headphone-Amplifier, and Speaker-Amplifier. The AK4691 is suitable for portable applications such as built-in LCD. The AK4691 is available in a 57pin BGA, utilizing less board space than competitive offerings.

FEATURES

1. Recording Function
- **4-channel Single-ended Pre-Amp**
  (Pre-Amp Gain: 0dB, +18dB, +20dB, +24dB or +28dB)
- **2-channel Line Input**
- **3-input Selector (Internal MIC, External MIC or LINE)**
- **4-channel Digital ALC (Automatic Level Control)**
- **ADC Performance: S/(N+D): 82dB, DR, S/N: 90dB (Pre-Amp=+24dB)**
  S/(N+D): 85dB, DR, S/N: 90dB (LINE)
- **Wind-noise Reduction Filter**
- **Stereo Separation Emphasis**
- **Fade-in/out Function**

2. Playback Function
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital Volume (+12dB ~ –115.0dB, 0.5dB Step, Mute)**
- **Digital ALC (Automatic Level Control)**
- **Stereo Separation Emphasis**
- **Stereo Line Output**
  - **Performance: S/(N+D): 85dB, S/N: 90dB**
  - **Output Level: -3.9dBV @ AVDD=LVDD=3.0V, LVOL=0dB**
    +2dBV @ AVDD=3.0V, LVDD=4.5V, LVOL=+5.9dB
- **Stereo Headphone-Amp**
  - **S/(N+D): 70dB, S/N: 90dB**
  - **Output Power: 58mW @ 16Ω (LVDD=3.3V)**
  - **Pop Noise Free at Power ON/OFF**
- **Mono Speaker-Amp**
  - **S/(N+D): 50dB@240mW, S/N: 90dB**
  - **BTL Output**
  - **Output Power: 400mW @ 8Ω (SVDD=3.3V)**
- **Analog Mixing**

3. Power Management

4. Master Clock:

(1) PLL Mode
- **Frequencies:**
  11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)
  1fs (LRCK pin)
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Frequencies: 256fs, 512fs or 1024fs (MCKI pin)**

5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs

6. Sampling Rate:
- **PLL Slave Mode (LRCK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **PLL Master Mode:**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **EXT Slave Mode:**
  7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 48kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

7. μP I/F: 3-wire Serial, I^2C Bus (Ver 1.0, 400kHz Fast-Mode)
8. Master/Slave mode
9. Audio Interface Format: MSB First, 2's complement
- **ADC: 16bit MSB justified, I^2S, TDM Mode**
- **DAC: 16bit MSB justified, 16bit LSB justified, 16-24bit I^2S, TDM Mode**

10. Ta = –30 ~ 85°C
11. Power Supply Voltage:
- **Analog (AVDD), Digital (DVDD): 2.6 ~ 3.6V**
- **MIC (MVDD): 2.6 ~ 5.5V**
- **Lineout & Headphone (LVDD): 2.6 ~ 5.5V**
- **Speaker (SVDD): 2.6 ~ 3.6V**
- **Digital I/F (TVDD1, TVDD2): 1.6 ~ 3.6V**

12. Package: 57pin BGA (5mm x 5mm, 0.5mm pitch, height: 1.0mm)

■ Block Diagram

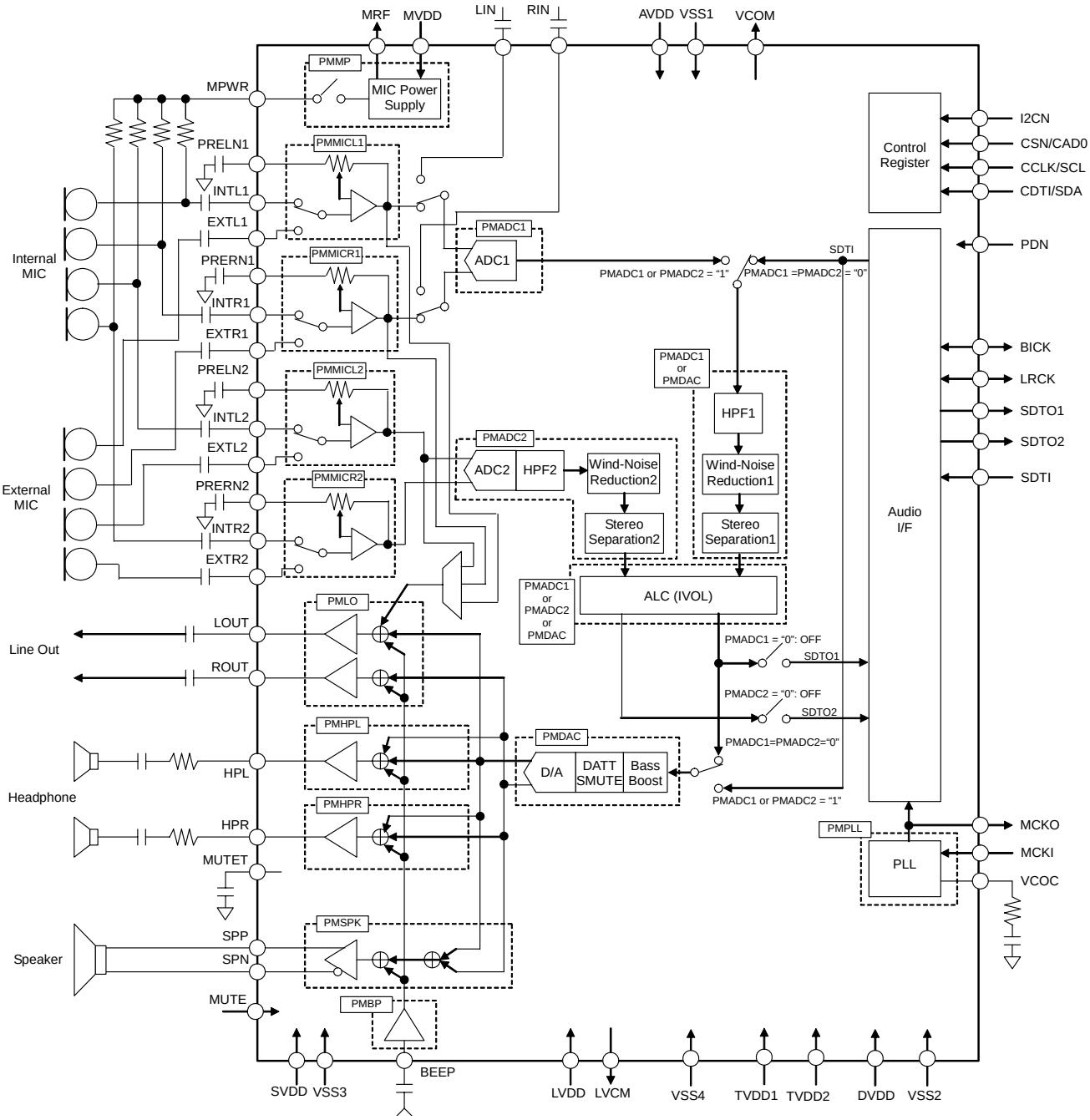
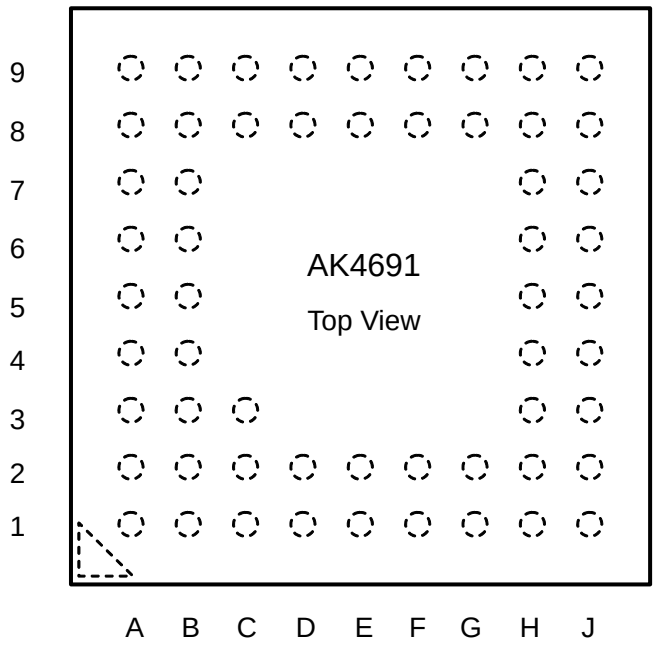


Figure 1. Block Diagram

■ Ordering Guide

AK4691EG	–30 ~ +85°C	57pin BGA
AKD4691	Evaluation board for AK4691	

■ Pin Layout



9	NC	VCOC	VCOM	AVDD	RIN	LOUT	LVCM	MUTET	NC
8	MRF	PRELN1	VSS1	LIN	BEEP	ROUT	LVDD	HPL	VSS4
7	PRERN2	PRELN2						VSS3	HPR
6	PRERN1	MVDD						SVDD	SPP
5	MPWR	INTL1			Top View			PDN	SPN
4	INTL2	EXTL1						CDTI/SDA	MUTE
3	INTR1	EXTL2	NC					CSN/CAD0	CCLK/SCL
2	INTR2	EXTR1	TVDD1	MCKI	SDTO2	LRCK	MCKO	TVDD2	NC
1	NC	EXTR2	I2CN	SDTI	SDTO1	BICK	DVDD	VSS2	NC
	A	B	C	D	E	F	G	H	J

PIN/FUNCTION

No.	Pin Name	I/O	Function
Power Supply			
D9	AVDD	-	Analog Power Supply Pin, 2.6 ~ 3.6V
C8	VSS1	-	Ground 1 Pin
C9	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of ADC inputs and DAC outputs.
G1	DVDD	-	Digital Power Supply Pin, 2.6 ~ 3.6V
H1	VSS2	-	Ground 2 Pin
H6	SVDD	-	Speaker-Amp Power Supply Pin, 2.6 ~ 3.6V
H7	VSS3	-	Ground 3 Pin
B6	MVDD	-	MIC Block Power Supply Pin, 2.6 ~ 5.5V
A5	MPWR	O	MIC Power Output Pin
A8	MRF	O	MIC Power Supply Ripple Filter Pin
G8	LVDD	-	Headphone & LINEOUT-Amp Power Supply Pin, 2.6 ~ 5.5V
G9	LVCM	O	LINEOUT-Amp Common Voltage Output Pin, 0.5 x LVDD
J8	VSS4	-	Ground 4 Pin
C2	TVDD1	-	Digital I/F(Audio Interface) Power Supply 1 Pin, 1.6 ~ 3.6V
H2	TVDD2	-	Digital I/F(Control Register Interface) Power Supply 2 Pin, 1.6 ~ 3.6V
Audio Interface			
D2	MCKI	I	External Master Clock Input Pin
G2	MCKO	O	Master Clock Output Pin
F2	LRCK	I/O	Input / Output Channel Clock Pin
F1	BICK	I/O	Audio Serial Data Clock Pin
D1	SDTI	I	Audio Serial Data Input Pin
E1	SDTO1	O	Audio Serial Data Output 1 Pin
E2	SDTO2	O	Audio Serial Data Output 2 Pin
Control Register Interface			
C1	I2CN	I	Control Mode Select Pin "L": I^2C Bus, "H": 3-wire Serial
H3	CSN	I	Chip Select Pin (I2CN pin = "H")
	CAD0	I	Chip Address 0 Select Pin (I2CN pin = "L")
J3	CCLK	I	Control Data Clock Pin (I2CN pin = "H")
	SCL	I	Control Data Clock Pin (I2CN pin = "L")
H4	CDTI	I	Control Data Input Pin (I2CN pin = "H")
	SDA	I/O	Control Data Input/Output Pin (I2CN pin = "L")
MIC Block			
B5	INTL1	I	Internal MIC Lch Input 1 Pin
B4	EXTL1	I	External MIC Lch Input 1 Pin
B8	PRELN1	I	Lch Pre-Amp Negative Input 1 Pin
A3	INTR1	I	Internal MIC Rch Input 1 Pin
B2	EXTR1	I	External MIC Rch Input 1 Pin
A6	PRERN1	I	Rch Pre-Amp Negative Input 1 Pin
A4	INTL2	I	Internal MIC Lch Input 2 Pin
B3	EXTL2	I	External MIC Lch Input 2 Pin
B7	PRELN2	I	Lch Pre-Amp Negative Input 2 Pin
A2	INTR2	I	Internal MIC Rch Input 2 Pin
B1	EXTR2	I	External MIC Rch Input 2 Pin
A7	PRERN2	I	Rch Pre-Amp Negative Input 2 Pin
ADC Block			
D8	LIN	I	Lch Line Input Pin
E9	RIN	I	Rch Line Input Pin

No.	Pin Name	I/O	Function
DAC Block			
F9	LOUT	O	Lch Stereo Line Output Pin
F8	ROUT	O	Rch Stereo Line Output Pin
HP-Amp Block			
H8	HPL	O	Lch Headphone-Amp Output Pin
J7	HPR	O	Rch Headphone-Amp Output Pin
H9	MUTET	O	Mute Time Constant Control Pin Connected to VSS4 pin with a capacitor for mute time constant.
SPK-Amp Block			
J5	SPN	O	Speaker Amp Negative Output Pin
J6	SPP	O	Speaker Amp Positive Output Pin
Other Functions			
J4	MUTE	I	Mute Pin "L": Normal Operation, "H": Mute
B9	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to VSS1 with one resistor and capacitor in series.
H5	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initialize the control register.
E8	BEEP	I	BEEP Signal Input Pin
A1 A9 C3 J1 J2 J9	NC	-	No Connection Pin No internal bonding. This pin should be connected to ground.

Note 1. All input pins except analog input pins (BEEP, INTL1/2, EXTL1/2, INTR1/2, EXTR1/2, LIN, and RIN) should not be left floating.
Note 2. All analog input pins (INTL1/2, EXTL1/2, INTR1/2, EXTR1/2, LIN, and RIN pins) except the BEEP pin should be supplied signal via AC-coupling capacitor.
Note 3. The BEEP pin should be supplied signal via AC-coupling capacitor and resistor.
Note 4. Analog output pins (HPL, HPR, LOUT, and ROUT pins) except the SPP and SPN pins should deliver signal via AC-coupling capacitor.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, VCOC, SPN, SPP, HPR, HPL, MUTET, ROUT, LOUT, BEEP	These pins should be open.
	INTL1, INTL2, INTR1, INTR2, EXTL1, EXTL2, EXTR1, EXTR2, LIN, RIN	These pins should be open and each path should be switched off.
Digital	MCKO, SDTO1, SDTO2	These pins should be open.
	MCKI, SDTI, MUTE	These pins should be connected to VSS2.
Other	NC	This pin should be connected to ground (VSS1, VSS2, VSS3 or VSS4).

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4 = 0V; Note 5, Note 6)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
	MIC-Amp	MVDD	–0.3	6.0	V
	Speaker-Amp	SVDD	–0.3	6.0	V
	Headphone-Amp/LINEOUT-Amp	LVDD	–0.3	6.0	V
	Digital I/F 1	TVDD1	–0.3	6.0	V
	Digital I/F 2	TVDD2	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 7)		VINA1	–0.3	AVDD+0.3	V
(Note 8)		VINA2	–0.3	MVDD+0.3	V
Digital Input Voltage (Note 9)		VIND1	–0.3	TVDD1+0.3	V
(Note 10)		VIND2	–0.3	TVDD2+0.3	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 11)		Pd	-	1.1	W

Note 5. All voltages with respect to ground.
Note 6. VSS1, VSS2, VSS3, and VSS4 must be connected to the same analog ground plane.
Note 7. LIN, RIN, BEEP pins
Note 8. INTL1/2, INTR1/2, EXTL1/2, EXTR1/2, PRELN1/2, PRERN1/2 pins
Note 9. I2CN, MCKI, LRCK, BICK, SDTI pins
Note 10. PDN, CSN/CAD0, CCLK/SCL, CDTI/SDA, MUTE pins
Pull-up resistors at the SDA and SCL pins should be connected to (TVDD2+0.3)V or less voltage.
Note 11. In case of PCB wiring density is 200% or more. This power is the AK4691 internal dissipation that does not include power dissipation of externally connected speaker and headphone.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4 = 0V; Note 5)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 14)	Analog	AVDD	2.6	3.0	3.6	V
	LINE/HP (Note 12)	LVDD	2.6	3.0	5.5	V
	MIC (Note 13)	MVDD	2.6 or "AVDD – 0.1"	3.0	5.5	V
	Digital	DVDD	2.6	3.0	3.6	V
	Digital I/F 1	TVDD1	1.6	3.0	DVDD	V
	Digital I/F 2	TVDD2	1.6	3.0	DVDD	V
	SPK	SVDD	2.6	3.0	3.6	V
	Difference	AVDD – DVDD	-0.3	0	0.3	V

Note 5. All voltages with respect to ground.

Note 12. When the voltage of LVDD pin is low and a high level signal is output from LINEOUT, the output signal is clipped and the distortion of LINEOUT degrades. LVDD should be more than (0.6 x AVDD + 0.8)[V] at LVOL2-0 bits = "000" and be more than (0.76 x AVDD + 0.8)[V] at LVOL2-0 bits = "001" and be more than (1.19 x AVDD + 0.8)[V] at LVOL2-0 bits = "010" and be more than (1.36 x AVDD + 0.8)[V] at LVOL2-0 bits = "100"in order to avoid clipping.

Note 13. The Minimum value is higher value between 2.6V and "AVDD – 0.1"V.

Note 14. The power up sequence among AVDD, LVDD, MVDD, DVDD, TVDD1, TVDD2, and SVDD is not critical.

The AK4691 supports the following two cases of partial power ON/OFF. In these cases, the PDN pin must be "L".

1. TVDD1=TVDD2=ON: AVDD=DVDD=LVDD=MVDD=SVDD can be power ON/OFF.
2. TVDD2=ON: TVDD1=AVDD=DVDD=LVDD=MVDD=SVDD can be power ON/OFF.

When the power state is changed from OFF to ON in the above cases, the PDN pin should be changed from "L" to "H" after all power supply pins (TVDD1, TVDD2, AVDD, DVDD, MVDD, LVDD, and SVDD pins) are supplied. "L" time of 150ns or more is needed to reset the AK4691.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=MVDD=LVDD=SVDD=TVDD1=TVDD2=3.0V; VSS1=VSS2=VSS3=VSS4 = 0V; fs=48kHz; Input Frequency =1kHz; Measurement width=20Hz ~ 20kHz, unless otherwise specified)

Parameter		min	typ	max	Units
Pre-Amp Characteristics:					
Input Resistance: Positive Input Pin (Note 15)		70	100	130	kΩ
Negative Input Pin (Note 16)		1.54	2.2	2.86	kΩ
Gain	PRG12-10 bits = "000", FB bit = "1" PRG22-20 bits = "000", FB bit = "1"	-0.8	0	+17.2	dB
	PRG12-10 bits = "001", FB bit = "0" PRG22-20 bits = "001", FB bit = "0"	+17.2	+18	+18.8	dB
	PRG12-10 bits = "010", FB bit = "0" PRG22-20 bits = "010", FB bit = "0"	+19.2	+20	+20.8	dB
	PRG12-10 bits = "011", FB bit = "0" PRG22-20 bits = "011", FB bit = "0"	+23.2	+24	+24.8	dB
	PRG12-10 bits = "100", FB bit = "0" PRG22-20 bits = "100", FB bit = "0"	+27.2	+28	+28.8	dB
MIC Power Supply Voltage Characteristics: MPWR pin					
Output Voltage (Output current = 0mA) (Note 17)		1.7	1.9	2.1	V
Maximum Output Current		-	-	4	mA
ADC Analog Input Characteristics: ALC = OFF					
Resolution		-	-	16	bits
Input Resistance (LIN, RIN pins)		70	100	130	kΩ
Input Voltage (Note 18) (Note 19)		-4.5	-3.7	-2.9	dBV
(Note 18) (Note 20)		-57.9	-57.1	-56.3	dBV
S/(N+D) (-1dBFS) (Note 19)		75	85	-	dB
(Note 21)		72	82	-	dB
DR (-60dBFS, A-Weighted) (Note 19)		81	90	-	dB
(Note 20)		54	60	-	dB
S/N (A-Weighted) (Note 19)		81	90	-	dB
(Note 20)		54	60	-	dB
Interchannel Isolation (Note 19)		80	100	-	dB
(Note 20)		50	70	-	dB
Interchannel Gain Mismatch (Note 19)		-	-	0.5	dB
(Note 20)		-	-	0.5	dB

Note 15. INTL1/2, INTR1/2, EXTL1/2, EXTR1/2 pins

Note 16. PRELN1/2, PRERN1/2 pins. Gain=0dB, +20dB: 3.5kΩ ± 30%; Gain=+18dB: 4.4kΩ ± 30%, Gain=+24dB: 2.2kΩ ± 30%, Gain=+28dB: 1.4kΩ ± 30%

Note 17. When the output current is 0mA, the output voltage of MPWR pin is typically (MVDD – 1.1) V at MVDD=3.0V and typically (MVDD-1.4) V at MVDD=4.5V.
When the output current is 4mA, the output voltage of MPWR pin is typically (MVDD – 1.3) V at MVDD=3.0V and typically (MVDD-1.5) V at MVDD=4.5V.

Note 18. Input voltages are proportional to AVDD voltage.
LIN, RIN = typ. (0.62 x AVDD) Vpp
INTL1/2, INTR1/2, EXTL1/2, EXTR1/2 = typ. (0.0013 x AVDD) Vpp

Note 19. Input from LIN, RIN pins. FB = "1", IVOL=0dB.

Note 20. Input from INTL1/2, INTR1/2, EXTL1/2 or EXTR1/2 pins. Pre-Amp Gain = + 24dB, PRE bit = "1", FB bit = "0", IVOL = +29.625dB, MGL12-10 = MGR12-10 = MGL22-20 = MGR22-20 bits = "010" (0dB)

Note 21. Input from INTL1/2, INTR1/2, EXTL1/2 or EXTR1/2 pins. Pre-Amp Gain = + 24dB, PRE bit = "1", FB bit = "0", IVOL = +0dB, MGL12-10 = MGR12-10 = MGL22-20 = MGR22-20 bits = "010" (0dB)

*** 0dBV = 1Vrms = 2.83Vpp**

Parameter		min	typ	max	Units
DAC Analog Output characteristics: DAC → LOUT/ROUT, IVOL=DVOL=LVOL=+0dB, ALC=OFF, R_L= 10kΩ					
Resolution		-	-	16	bits
S/(N+D) (0dBFS)		76	85	-	dB
DR (-60dBFS, A-Weighted)		83	90	-	dB
S/N (A-Weighted)		83	90	-	dB
Output Voltage (Note 23)		-4.7	-3.9	-3.1	dBV
Interchannel Isolation		80	100	-	dB
Interchannel Gain Mismatch		-	-	0.5	dB
Load Resistance		10	-	-	kΩ
Load Capacitance (Note 22)		-	-	30	pF
Headphone-Amp Characteristics: DAC → HPL/HPR pins, ALC=OFF, IVOL=DVOL=0dB					
Output Voltage (Note 24)					
HPG bit = "0", 0dBFS, LVDD=3.0V, R_L=22.8Ω		-5.8	-3.9	-2	dBV
HPG bit = "1", 0dBFS, LVDD=3.3V, R_L=16Ω (Po=58mW)		-	-0.3	-	dBV
S/(N+D)					
HPG bit = "0", –3dBFS, LVDD=3.0V, R_L=22.8Ω		60	70	-	dBFS
HPG bit = "1", 0dBFS, LVDD=5.0V, R_L=100Ω		-	80	-	dBFS
HPG bit = "1", 0dBFS, LVDD=3.3V, R_L=16Ω (Po=58mW)		-	20	-	dBFS
S/N (A-weighted) (Note 25)		82	90	-	dB
Interchannel Isolation (Note 25)		65	75	-	dB
Interchannel Gain Mismatch (Note 25)		-	0.1	0.8	dB
Load Resistance		16	-	-	Ω
Load Capacitance	C1 in Figure 2	-	-	30	pF
	C2 in Figure 2	-	-	300	pF

Note 22. When the output pin drives some capacitive load, some resistor should be added in series between output pin and capacitive load.

Note 23. Output voltage is proportional to AVDD voltage. LOUT, ROUT = typ. (0.6 x AVDD) Vpp @LVOL = 0dB.

Note 24. Output voltage is proportional to AVDD voltage.
HPL, HPR = typ. (0.6 x AVDD) Vpp @ HPG bit = "0", typ. (0.91 x AVDD) Vpp @ HPG bit = "1".

Note 25. HPG bit = "0", LVDD=3.0V, R_L=22.8Ω.

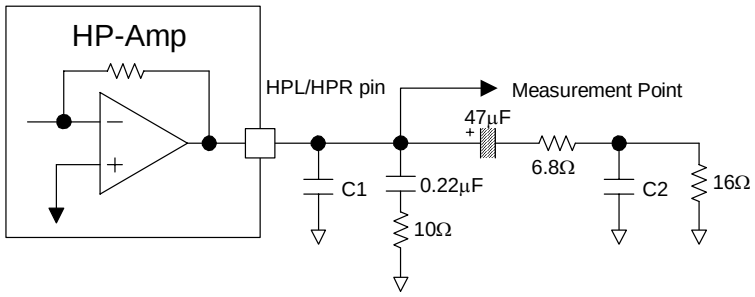


Figure 2. Headphone-Amp output circuit

*** 0dBV = 1Vrms = 2.83Vpp**

Parameter			min	typ	max	Units
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, IVOL=DVOL=0dB, R_L=8Ω, BTL, SVDD=3.0V (Note 27)						
Output Voltage (Note 26)						
	SPKG1-0 bits = "00", 0dBFS (Po=140mW)		-	0.5	-	dBV
	SPKG1-0 bits = "10", –3.75dBFS (Po=240mW)		1.4	3	4.6	dBV
	SPKG1-0 bits = "11", –3.75dBFS, SVDD=3.3V, (Po=400mW)		-	5	-	dBV
S/(N+D)						
	SPKG1-0 bits = "00", 0dBFS (Po=140mW)		-	60	-	dB
	SPKG1-0 bits = "10", –3.75dBFS (Po=240mW)		20	50	-	dB
	SPKG1-0 bits = "11", –3.75dBFS, SVDD=3.3V (Po=400mW)		-	20	-	dB
S/N (A-weighted)			80	90	-	dB
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	30	pF
Mono Input: BEEP pin (External Input Resistance=20kΩ)						
Maximum Input Voltage (Note 28)			-	1.8	-	Vpp
Gain (Note 29)						
	BEEP → LOUT/ROUT	LVOL2-0 bits = "000"	–4.5	0	+4.5	dB
	BEEP → HPL/HPR	HPG bit = "0"	–24.5	–20	–15.5	dB
	BEEP → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	–0.57	+4.43	+8.93	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+6.43	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+10.65	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+6.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+8.43	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+12.65	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+14.65	-	dB

Note 26. Output voltage is proportional to AVDD voltage. But actual speaker output level is clipped according to the supplied SVDD voltage.
Vout = typ. 1.0 x AVDD Vpp @ SPKG1-0 bits = "00" & 0dBFS, typ. 1.26 x AVDDVpp @ SPKG1-0 bits = "01" & 0dBFS, typ. 2.04 x AVDDVpp @ SPKG1-0 bits = "10" & 0dBFS, typ. 2.58 x AVDDVpp @ SPKG1-0 bits = "11" & 0dBFS at Full-differential.

Note 27. In case of measuring at the SPP and SPN pins.

Note 28. The Maximum voltage is in proportion to both AVDD and external input resistance (Rin). Vin = 0.6 x AVDD x Rin / 20kΩ (typ).

Note 29. The gain is in inverse proportion to external input resistance.

*** 0dBV = 1Vrms = 2.83Vpp**

Parameter			min	typ	max	Units
Power Supplies:						
Power-Up (PDN pin = "H")						
	All Circuit Power-up: (Note 30)					
		AVDD+DVDD+MVDD+TVDD1+TVDD2	-	28	42	mA
		LVDD: HP & LINEOUT-Amp Normal Operation (No Output)	-	6.4	9.6	mA
		SVDD: SPK-Amp Normal Operation (No Output)	-	8	24	mA
	MIC + ADC (4ch Mode):					
		AVDD+DVDD+TVDD1+TVDD2 (Note 31)	-	15.2	-	mA
		MVDD	-	7.5	-	mA
	DAC+LINEOUT:					
		AVDD+DVDD+MVDD+SVDD+TVDD1+TVDD2 (Note 32)	-	9.2	-	mA
		LVDD: LINEOUT-Amp Normal Operation	-	1.8	-	mA
Power-Down (PDN pin = "L") (Note 33)						
	AVDD+DVDD+MVDD+LVDD+SVDD+TVDD1+TVDD2		-	10	100	μA

Note 30. PLL Master Mode (MCKI=12.288MHz), PMMICL1=PMMICR1=PMMICL2=PMMICR2=PMADC1 = PMADC2 = PMDAC = PMLO = PMHPL = PMHPR = PMSPK = PMVCM = PMPLL = MCKO = PMBP = PMMP = M/S = SPPSN =HPMNT bits = "1" and LOPS bit = "0". The MPWR pin outputs 0mA. AVDD=14.5mA(typ), DVDD=4.1mA(typ), MVDD=7.5mA (typ.), TVDD1=2mA(typ), TVDD2=0mA(typ). EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=13.5mA(typ), DVDD=4.1mA(typ), TVDD1=TVDD2=0mA(typ)

Note 31. PLL Master Mode (MCKI=12.288MHz) and PMMICL1 = PMMICR1 = PMMICL2 = PMMICR2 = PMADC1 = PMADC2 = PMVCM=PMPLL=MCKO=PMMP = M/S bits = "1".

Note 32. PLL Master Mode (MCKI=12.288MHz), PMDAC = PMLO =PMVCM= PMPLL = MCKO = PMBP = M/S bits = "1", and LOPS bit = "0".

Note 33. All digital input pins are fixed to TVDD1, TVDD2 or VSS2. The PDN pin is held at "VSS2".

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=SVDD=2.6 ~ 3.6V; LVDD=MVDD= 2.6 ~ 5.5V; TVDD1=TVDD2=1.6 ~ 3.6V; fs=48kHz; DEM=OFF; FIL1=FIL3=EQ=OFF)

Parameter			Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):							
Passband (Note 34)	±0.16dB		PB	0	-	18.8	kHz
	–0.66dB			-	21.1	-	kHz
	–1.1dB			-	21.6	-	kHz
	–6.9dB			-	24.0	-	kHz
Stopband			SB	28.4	-	-	kHz
Passband Ripple			PR	-	-	±0.1	dB
Stopband Attenuation			SA	73	-	-	dB
Group Delay (Note 35)			GD	-	19	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
ADC Digital Filter (HPF): (Note 36)							
Frequency Response (Note 34)	–3.0dB		FR	-	1.0	-	Hz
	–0.5dB			-	2.9	-	Hz
	–0.1dB			-	6.5	-	Hz
DAC Digital Filter (LPF):							
Passband (Note 34)	±0.1dB		PB	0	-	21.3	kHz
	–0.7dB			-	21.8	-	kHz
	–6.0dB			-	24.0	-	kHz
Stopband			SB	25.2	-	-	kHz
Passband Ripple			PR	-	-	±0.01	dB
Stopband Attenuation			SA	59	-	-	dB
Group Delay (Note 35)			GD	-	26	-	1/fs
DAC Digital Filter (LPF) + SCF:							
Frequency Response: 0 ~ 20.0kHz			FR	-	±1.0	-	dB
DAC Digital Filter (HPF): (Note 36)							
Frequency Response (Note 34)	–3.0dB		FR	-	1.0	-	Hz
	–0.5dB			-	2.9	-	Hz
	–0.1dB			-	6.5	-	Hz
BOOST Filter: (Note 37)							
Frequency Response	MIN	20Hz	FR	-	6.27	-	dB
		100Hz		-	3.18	-	dB
		1kHz		-	0.02	-	dB
	MID	20Hz	FR	-	11.6	-	dB
		100Hz		-	7.44	-	dB
		1kHz		-	0.14	-	dB
	MAX	20Hz	FR	-	17.48	-	dB
		100Hz		-	11.47	-	dB
		1kHz		-	0.40	-	dB

Note 34. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.45 x fs (@-1.1dB). Each response refers to that of 1kHz.

Note 35. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16-bit data of both channels from the input register to the output of analog signal.
DAC group delay is at PMADC1 = PMADC2 bits = "0". When PMADC1 bit is "1" or PMADC2 bit is "1", it is typ. 19/fs.

Note 36. When PMADC1 bit = "1" or PMADC2 bit = "1", the HPF of ADC is enabled but the HPF of DAC is disabled. When PMADC1 = PMADC2 bits = "0" and PMDAC bit = "1", the HPF of DAC is enabled (@ HPFN bit = "0") but the HPF of ADC is disabled.

Note 37. These frequency responses scale with fs. If a high-level and low frequency signal is input, the analog output clips to the full-scale.

DC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=SVDD=2.6 ~ 3.6V; LVDD=MVDD= 2.6 ~ 5.5V; TVDD1=TVDD2=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	2.2V≤TVDD1≤3.6V	VIH1	70%TVDD1	-	-	V
(Note 38)	1.6V≤TVDD1<2.2V	VIH1	80%TVDD1	-	-	V
Low-Level Input Voltage	2.2V≤TVDD1≤3.6V	VIL1	-	-	30%TVDD1	V
(Note 38)	1.6V≤TVDD1<2.2V	VIL1	-	-	20%TVDD1	V
High-Level Output Voltage (Note 39) (Iout=–200μA)		VOH1	TVDD1–0.2	-	-	V
Low-Level Output Voltage (Note 39) (Iout=200μA)		VOL1	-	-	0.2	V
High-Level Input Voltage	2.2V≤TVDD2≤3.6V	VIH2	70%TVDD2	-	-	V
(Note 40)	1.6V≤TVDD2<2.2V	VIH2	80%TVDD2	-	-	V
Low-Level Input Voltage	2.2V≤TVDD2≤3.6V	VIL2	-	-	30%TVDD2	V
(Note 40)	1.6V≤TVDD2<2.2V	VIL2	-	-	20%TVDD2	V
Low-Level Output Voltage (SDA pin) (2.0V≤TVDD2≤3.6V: Iout=3mA)		VOL2	-	-	0.4	V
(1.6V≤TVDD2<2.0V: Iout=3mA)		VOL2	-	-	20%TVDD2	V
Input Leakage Current		Iin	-	-	±10	μA

Note 38. I2CN, MCKI, BICK, LRCK, SDTI pins
Note 39. MCKO, SDTO1, SDTO2 pins
Note 40. MUTE, PDN, CSN/CAD0, CCLK/SCK, CDTI pins

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=SVDD=2.6 ~ 3.6V; LVDD=MVDD= 2.6 ~ 5.5V; TVDD1=TVDD2=1.6 ~ 3.6V; C_L=20pF)

Parameter		Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Parameter		Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle (Except TDM mode)		Duty	45	-	55	%
"H" time in TDM mode		tLRCKH	1/(16fs)	-	1/(32fs)	ns
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
PLL Slave Mode (PLL Reference Clock = LRCK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle (Except TDM mode)		Duty	45	-	55	%
"H" time in TDM mode		tLRCKH	1/(16fs)	-	1/(32fs)	ns
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	240	-	-	ns
Pulse Width High		tBCKH	240	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle (Except TDM mode)		Duty	45	-	55	%
"H" time in TDM mode		tLRCKH	1/(16fs)	-	1/(32fs)	ns
BICK Input Timing						
Period	PLL3-0 bits = "0010"	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = "0011"	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode						
MCKI Input Timing						
Frequency	MCKI = 256fs	fCLK	1.8816	-	12.288	MHz
	MCKI = 512fs	fCLK	3.7632	-	24.576	MHz
	MCKI = 1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing						
Frequency	MCKI = 256fs	fs	7.35	-	48	kHz
	MCKI = 512fs	fs	7.35	-	48	kHz
	MCKI = 1024fs	fs	7.35	-	13	kHz
Duty Cycle (Except TDM mode)		Duty	45	-	55	%
"H" time in TDM mode		tLRCKH	1/(16fs)	-	1/(32fs)	ns
BICK Input Timing						
Period		tBCK	312.5	-	-	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 42)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 42)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 42)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 43)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 43)	tCSH	50	-	-	ns
Control Interface Timing (I²C Bus mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 44)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 45)	tPD	150	-	-	ns
PMADC1 or PMADC2 "↑" to SDTO valid (Note 46)	tPDV	-	1059	-	1/fs

Note 41. I²C is a registered trademark of Philips Semiconductors.
Note 42. BICK rising edge must not occur at the same time as LRCK edge.
Note 43. CCLK rising edge must not occur at the same time as CSN edge.
Note 44. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 45. The AK4691 can be reset by the PDN pin = "L".
Note 46. This is the count of LRCK "↑" from the PMADC1 or PMADC2 bit = "1".

■ Timing Diagram

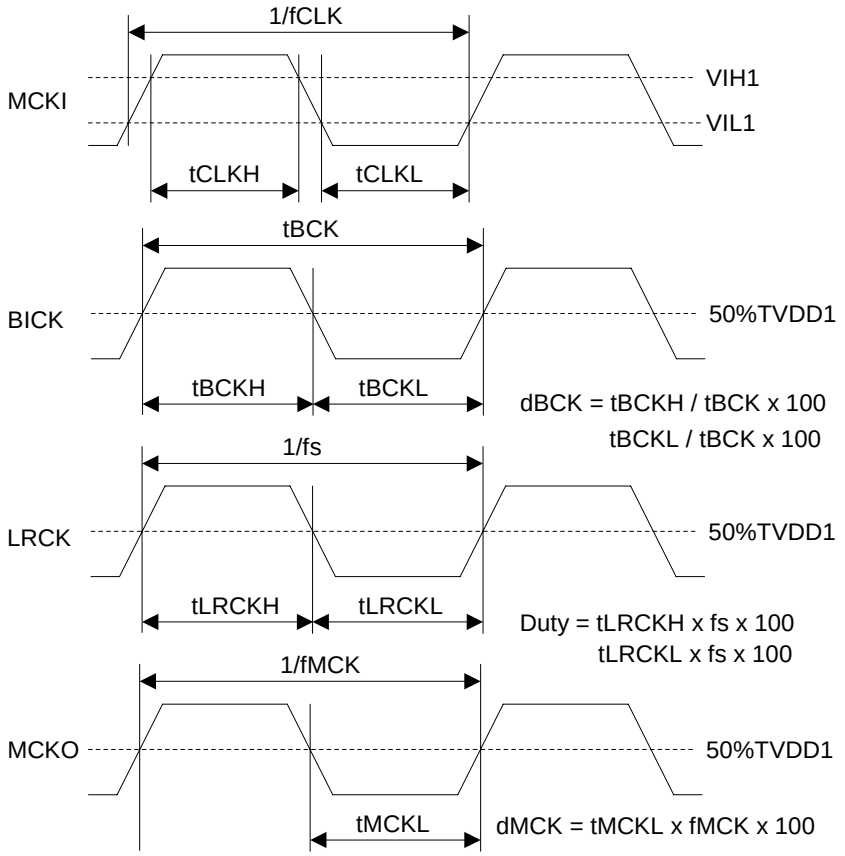


Figure 3. Clock Timing (PLL Master mode)

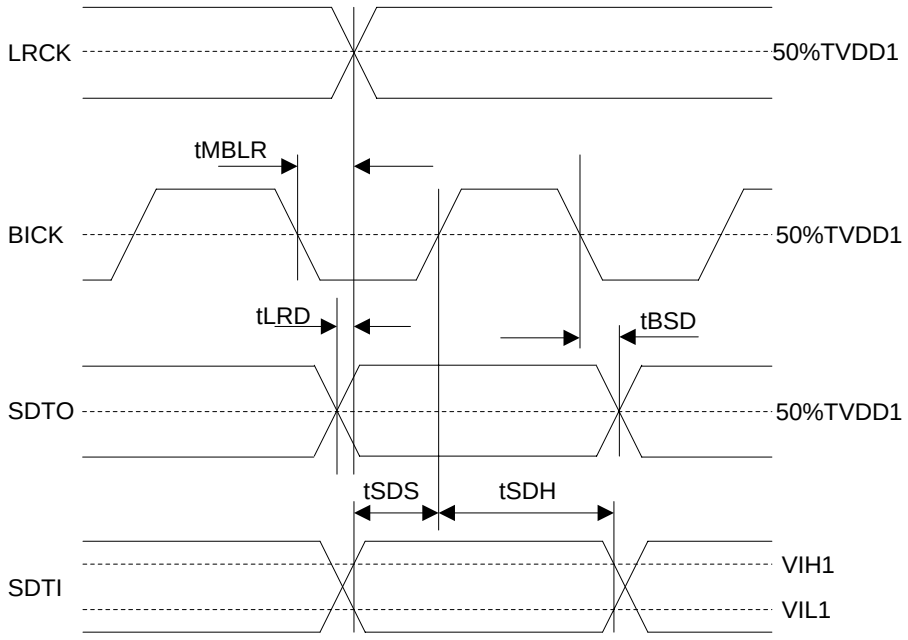


Figure 4. Audio Interface Timing (PLL Master mode)

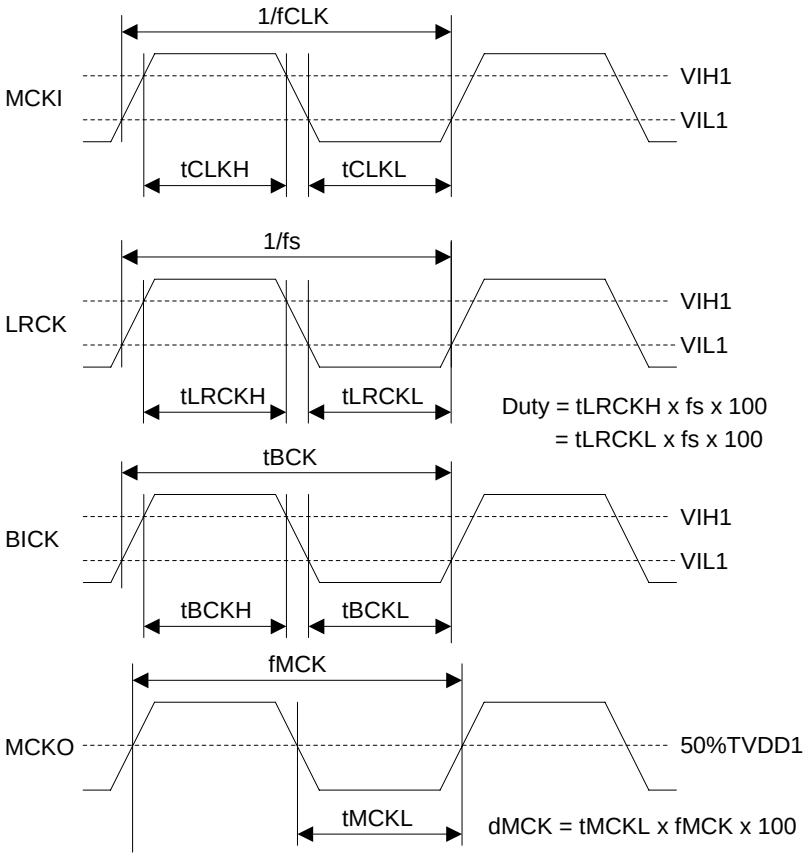


Figure 5. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

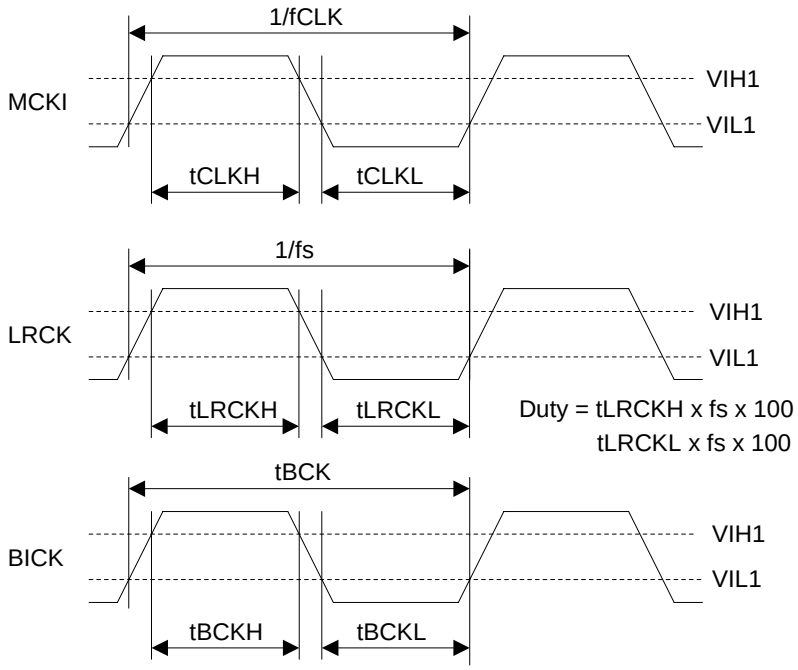


Figure 6. Clock Timing (EXT Slave mode)

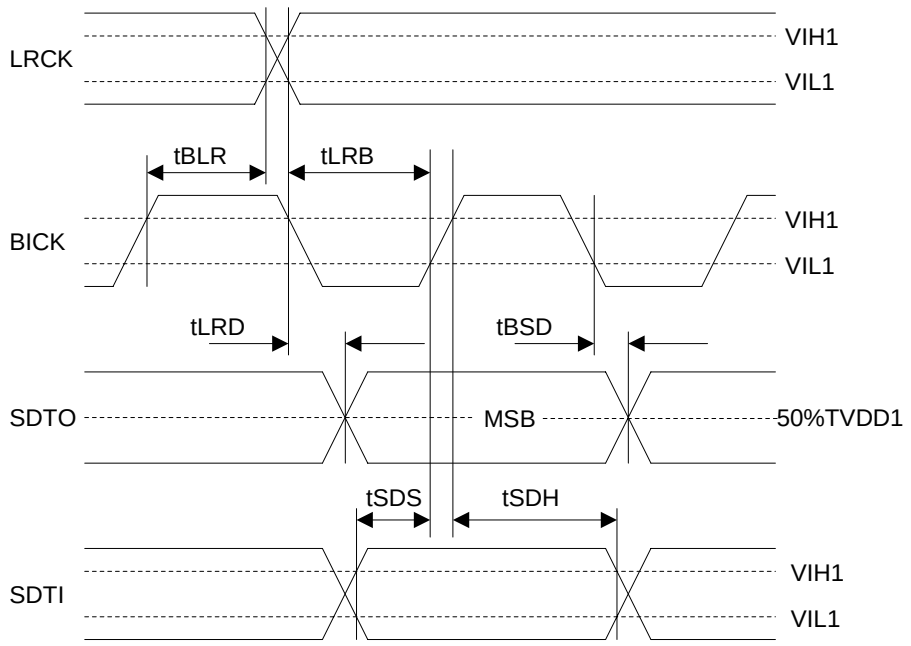


Figure 7. Audio Interface Timing (PLL/EXT Slave mode)

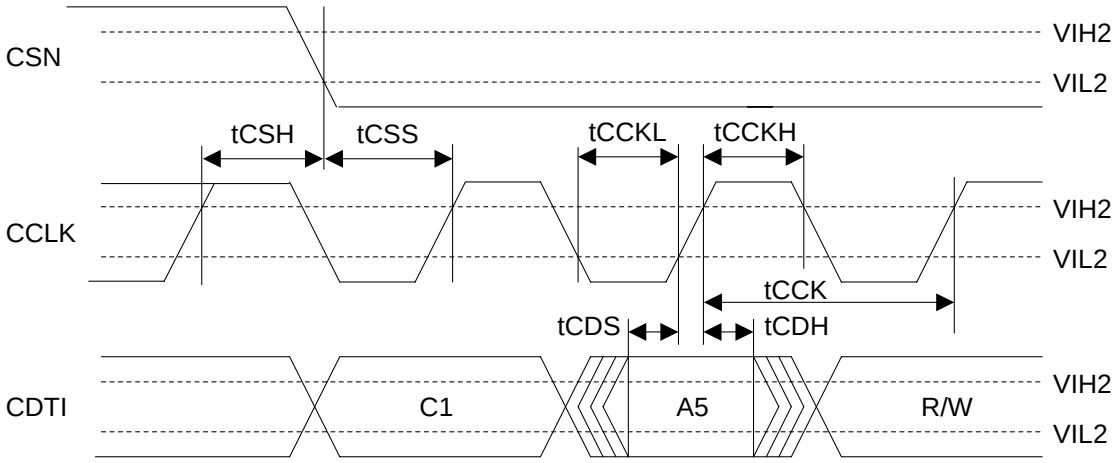


Figure 8. WRITE Command Input Timing

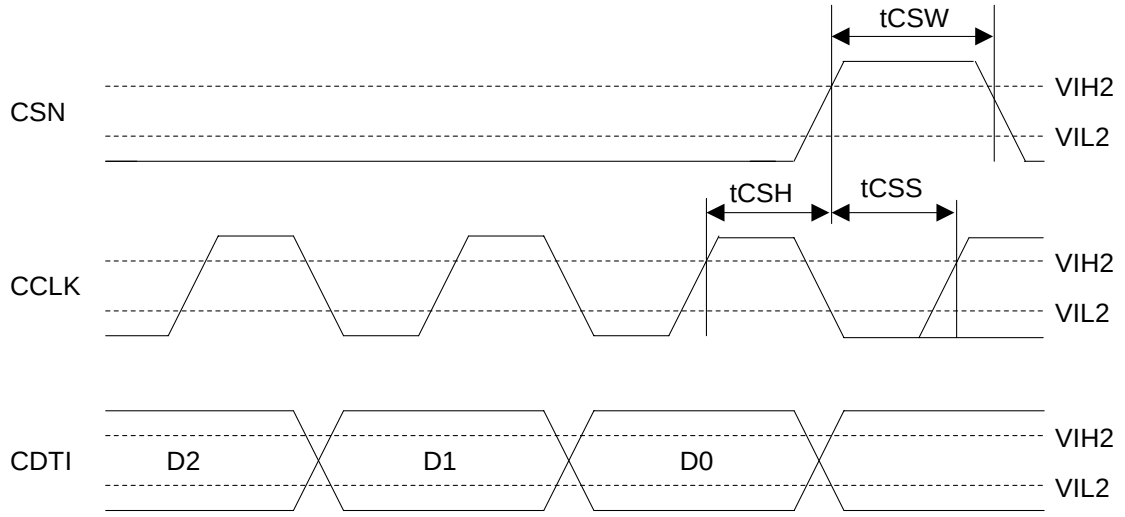


Figure 9. WRITE Data Input Timing

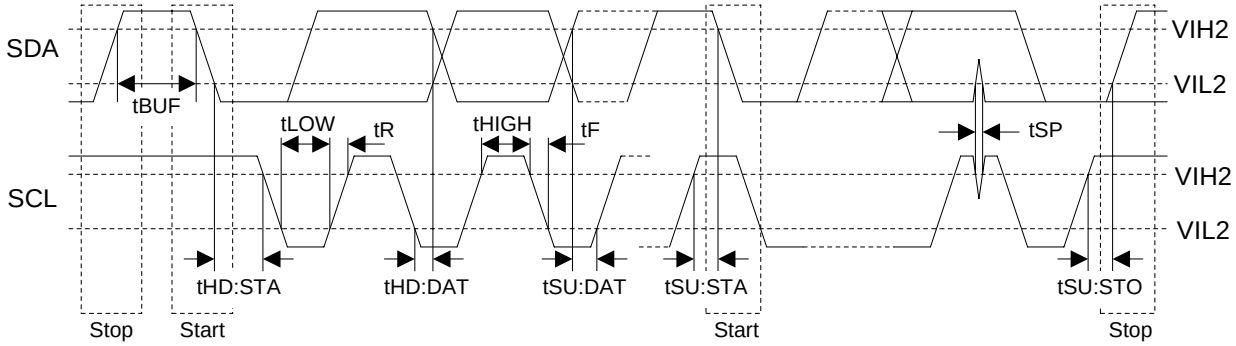


Figure 10. I^{2}C Bus Mode Timing

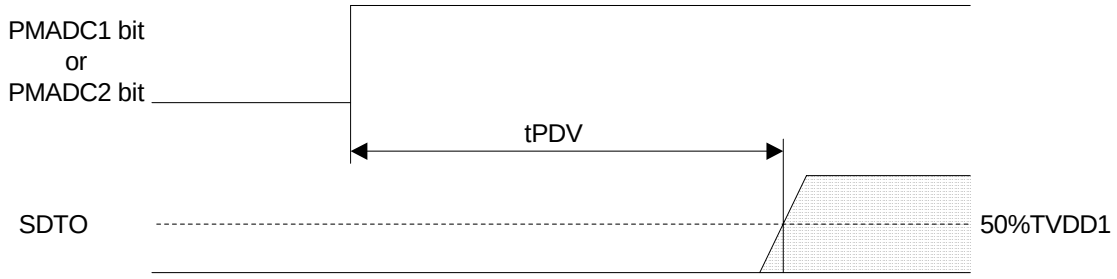


Figure 11. Power Down & Reset Timing 1

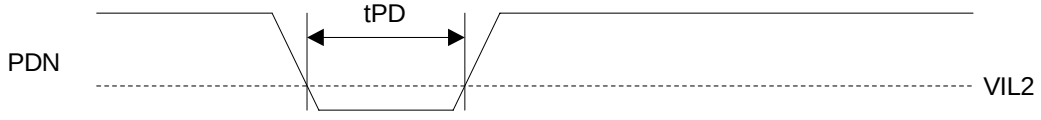


Figure 12. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following four clock modes to interface with external devices (Table 1, Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	Table 4	Figure 13
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 14
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 4	Figure 15
EXT Slave Mode	0	0	x	Figure 16
Don't Care (Note 47)	0	1	x	-

Note 47. If this mode is selected, the invalid clocks are output from the MCKO pin when MCKO bit is "1".

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	0	L	GND	Output (Selected by BCKO bit)	Input (1fs)
EXT Slave Mode	0	L	Selected by FS3-0 bits	Input (≥ 32fs)	Input (1fs)

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4691 is power-down mode (PDN pin = "L") and exits reset state, the AK4691 is slave mode. After exiting reset state, the AK4691 is set to master mode by changing M/S bit = "1".

When the AK4691 is used by master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4691 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, when the AK4691 is supplied stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	LRCK pin	1fs	6.8k	220n	160ms	(default)
1	0	0	0	1	N/A	-	-	-	-	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
							10k	10n	4ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
							10k	10n	4ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms	
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	40ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	40ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
Others	Others				N/A					

Table 4. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not available)

2) Setting of sampling frequency in PLL Mode
When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	(default)
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz	
5	0	1	0	1	11.025kHz	
6	0	1	1	0	14.7kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz	
15	1	1	1	1	44.1kHz	
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1" (N/A: Not available)

When PLL2 bit is "0" (PLL reference clock input is LRCK or BICK pin), the sampling frequency is selected by FS3 and FS1-0 bits (Table 6). **FS2 bit is "don't care".**

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	x	0	0	7.35kHz ≤ fs ≤ 8kHz	(default)
1	0	x	0	1	8kHz < fs ≤ 12kHz	
2	0	x	1	0	12kHz < fs ≤ 16kHz	
3	0	x	1	1	16kHz < fs ≤ 24kHz	
6	1	x	1	0	24kHz < fs ≤ 32kHz	
7	1	x	1	1	32kHz < fs ≤ 48kHz	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1" (x: Don't care)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK and BICK pins change to "L" and irregular frequency clock is output from the MCKO pin at MCKO bit is "1" before the PLL sets to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin changes to "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, the BICK and LRCK pins do not output irregular frequency clocks but change to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After after PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except above case)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 9	Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL sets to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal can be muted by writing "0" to DACL, DACH and DACS bits.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

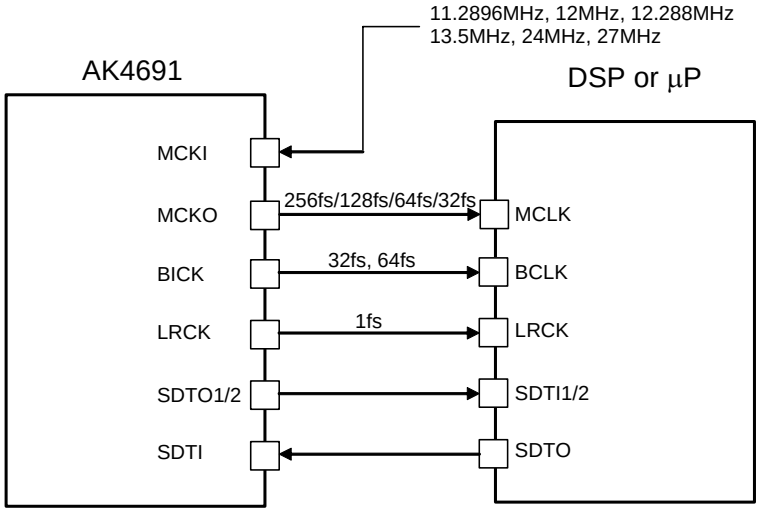


Figure 13. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pin. The required clock to the AK4691 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

The BICK and LRCK inputs should be synchronized with the MCKO output. The phase between MCKO and LRCK dose not matter. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

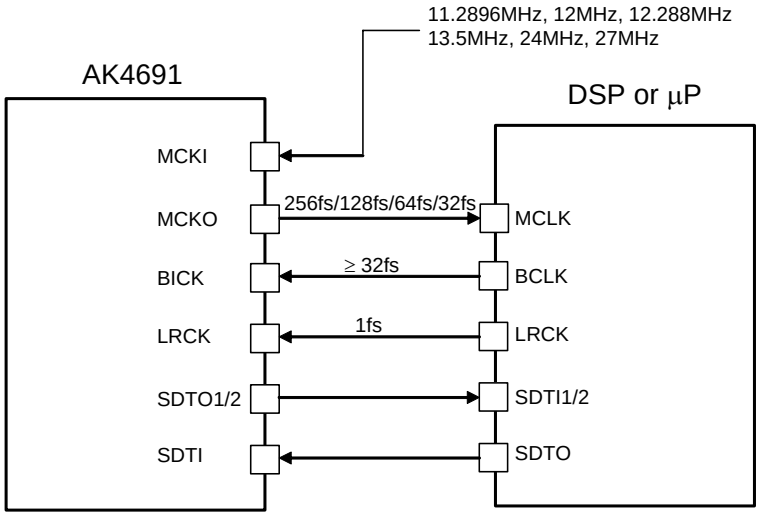


Figure 14. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK or LRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (Table 6).

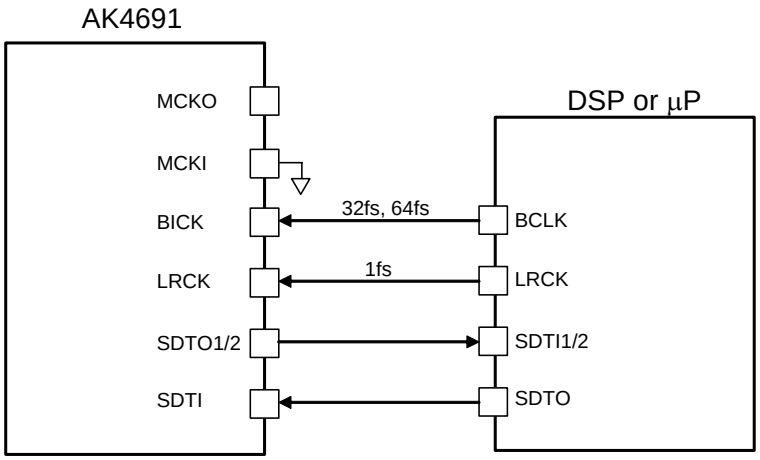


Figure 15. PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADC1 bit = "1", PMADC2 bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4691 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADC1=PMADC2=PMDAC bits = "0").

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4691 becomes EXT mode. Master clock is input directly from MCKI pin without the internal PLL circuit. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits (Table 11).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 48kHz	
3	x	1	1	512fs	7.35kHz ~ 26kHz	
Others	Others			N/A	N/A	

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0"), (N/A: Not available, x: Don't care)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through the LOUT/ROUT pins at fs=8kHz is shown in Table 12.

Mode	MCKI	S/N (fs=8kHz, 20kHzLPF + A-weighted)
0	256fs	80dB
2	512fs	
3	512fs	90dB
1	1024fs	90dB

Table 12. Relationship between MCKI and S/N of LOUT/ROUT pins

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADC1 bit = "1", PMADC2 bit = "1" or PMDAC bit = "1"). If these clocks are not provided, the AK4691 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADC1=PMADC2=PMDAC bits = "0").

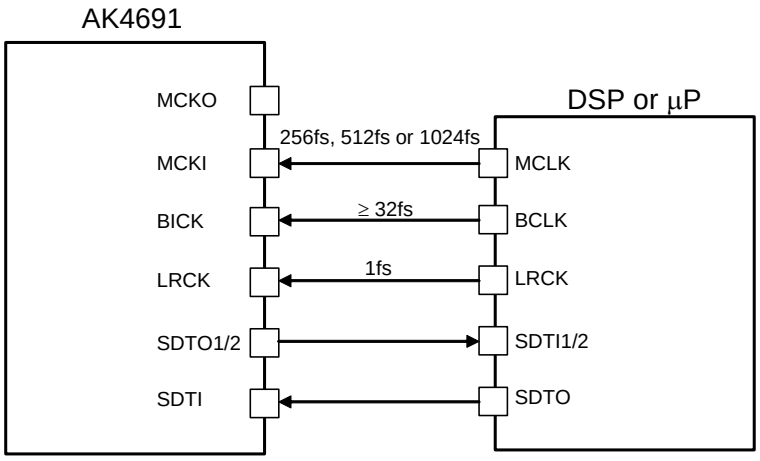


Figure 16. EXT Slave Mode

■ System Reset

When power-up, the AK4691 should be reset by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle when the PMADC1 or PMADC2 bit is changed from "0" to "1" at PMDAC bit = "0". The initialization cycle time is 1059/fs=22ms@fs=48kHz. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's complement, "0". The ADC output reflects the analog input signal after the initialization cycle is complete.

The DAC enters an initialization cycle when the PMDAC bit is changed from "0" to "1" at PMADC1 = PMADC2 = INITDA bits = "0". The initialization cycle time is 1059/fs=22ms@fs=48kHz. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2's complement, "0". The DAC output reflects the digital input data after the initialization cycle is complete and group delay of DAC (26/fs = 0.54ms @ fs=48kHz) is passed. When INITDA bits = "1", the DAC does not do initialization cycle. When PMADC1 or PMADC 2 bit is "1", INITDA bit should be set to "0". When PMDAC bit is "0", INITDA bit should be changed.

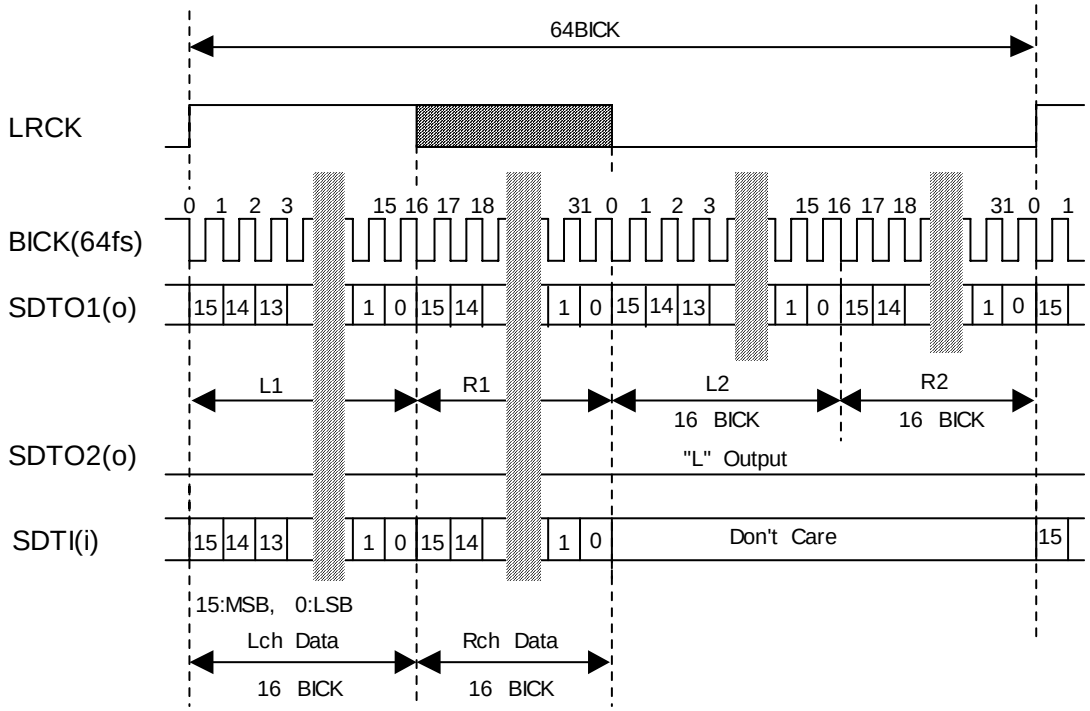
■ Audio Interface Format

Four types of data formats are available and are selected by setting the DIF1-0 bits (Table 13). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4691 in master mode, but must be input to the AK4691 in slave mode. The SDTO is clocked out on the falling edge ("↓") of BICK and the SDTI is latched on the rising edge ("↑"). **SDTO1's Audio interface format is the same as SDTO2's.**

Mode	DIF1 bit	DIF0 bit	SDTO1 (ADC1) SDTO2 (ADC2)	SDTI (DAC)	BICK	Figure	
0	0	0	TDM Mode	TDM Mode	64fs	Figure 17	
1	0	1	MSB justified	LSB justified	≥ 32fs	Figure 18	
2	1	0	MSB justified	MSB justified	≥ 32fs	Figure 19	(default)
3	1	1	I^2S compatible	I^2S compatible	≥ 32fs	Figure 20	

Table 13. Audio Interface Format

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "–1" at 16bit data is converted to "–1" at 8-bit data. And when the DAC playbacks this 8-bit data, "–1" at 8-bit data will be converted to "–256" at 16-bit data which is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.



Note 48. When PMADC1 bit is "0", SDTO1 is output to "0" data during the period of L1 and R1. When PMADC2 bit is "0", SDTO2 is output to "0" data during the period of L2 and R2.

Figure 17. Mode 0 Timing (TDM Mode)

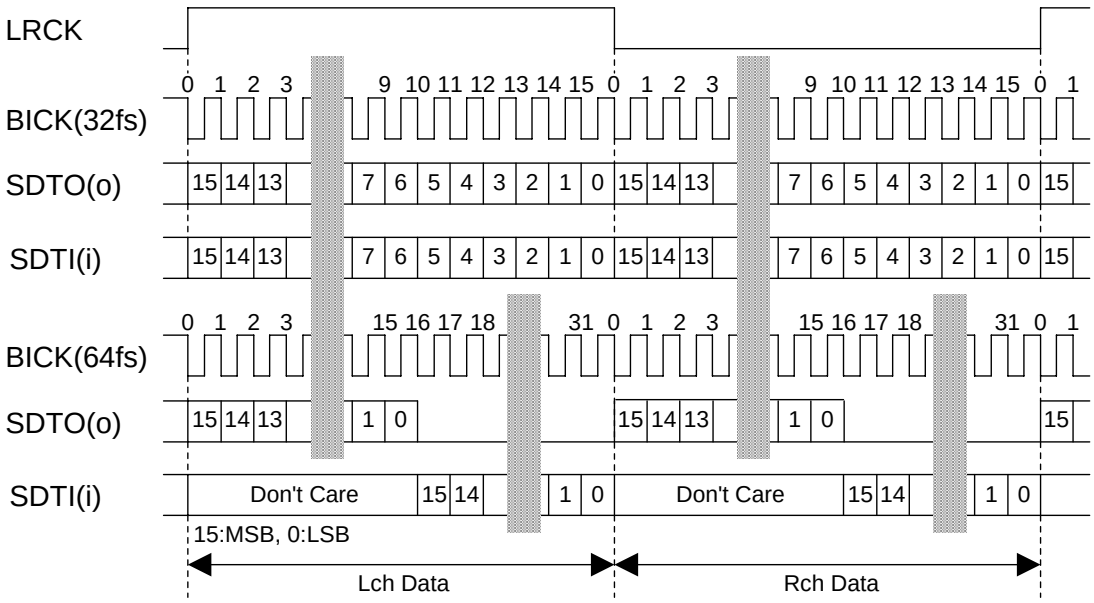


Figure 18. Mode 1 Timing

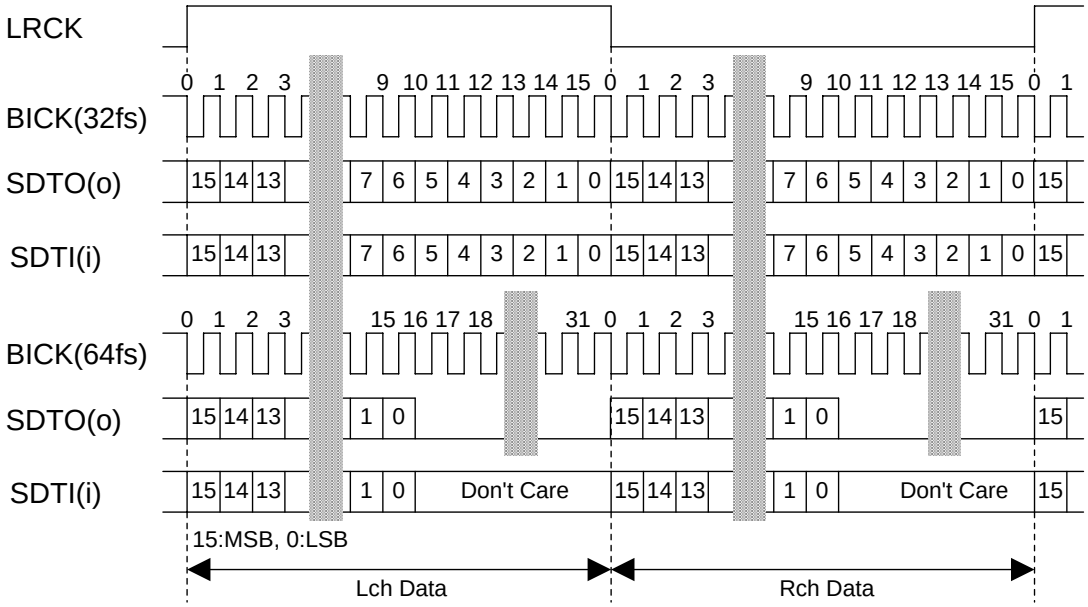


Figure 19. Mode 2 Timing

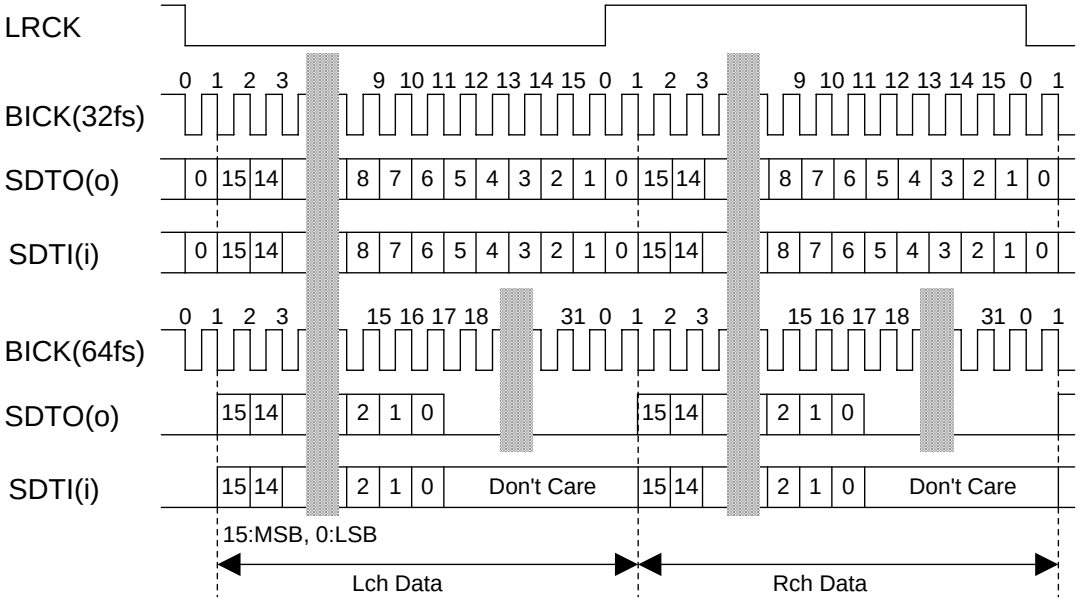


Figure 20. Mode 3 Timing

■ MIC BLOCK

1. Pre- Amp

Pre-Amp includes a selector, Internal MIC or External MIC Mode can be selected by PRSL2-1 and PRSR2-1 bits. The Pre-Amp is non-inverting amplifier and internally biased to VCOM voltage with 100kΩ (typ.). The gain from Pre-Amp #1 to MIXL/R-Amp is set by PRG12-10, and the gain from Pre-Amp #2 to MIXL/R-Amp is set by PRG22-20 bits (Table 15).

PRSL1 bit	Lch Pre-Amp #1 Input Signal Source
0	INTL1 pin
1	EXTL1 pin

PRSR1 bit	Rch Pre-Amp #1 Input Signal Source
0	INTR1 pin
1	EXTR1 pin

PRSL2 bit	Lch Pre-Amp #2 Input Signal Source
0	INTL2 pin
1	EXTL2 pin

PRSR2 bit	Rch Pre-Amp #2 Input Signal Source
0	INTR2 pin
1	EXTR2 pin

Table 14. Pre-Amp Input Signal Source Select

An external capacitor (C1) is needed to cancel DC gain. The cut-off frequency is determined by an external capacitor (C1) and internal feedback resistor (Rn). The internal feedback resistor (Rn) depends on Pre-Amp Gain and is typ ± 30%.

PRG12 bit PRG22 bit	PRG11 bit PRG21 bit	PRG10 bit PRG20 bit	Gain		Rn(typ)
			FB bit = "0"	FB bit = "1"	
0	0	0	-4.4dB (Note 49)	0dB (Note 49)	3.5kΩ
0	0	1	+18dB	+22.4dB	4.4 kΩ
0	1	0	+20dB	+24.4dB	3.5kΩ
0	1	1	+24dB (default)	+28.4dB	2.2kΩ
1	0	0	+28dB	+32.4dB	1.4kΩ
1	0	1	N/A		
1	1	0			
1	1	1			

Note 49. Input signal is bypassed to Pre-Amp and is inputted to MIX-Amp. The cut-off frequency is determined by input impedance (typ. 100kΩ) and external capacitors (C2, C3).

Table 15. Relationship between Pre-Amp Gain and Feedback resistor (N/A: Not available)

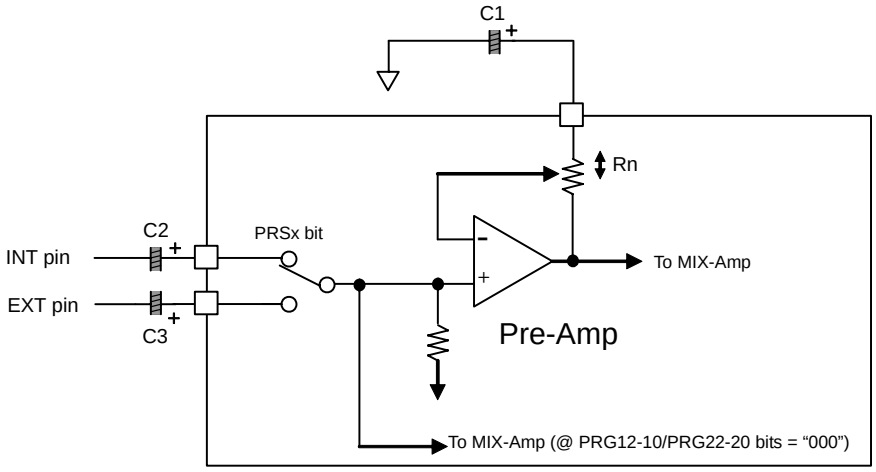


Figure 21. Pre-Amp

2. Power Supply for MIC

The Power Supply for microphone device is supplied from the MPWR pin. The MPWR pin can supply the current up to 4mA. When the output current is 0mA, the output voltage is typically (MVDD – 1.1) V at MVDD=3.0V and typically (MVDD – 1.4) V at MVDD=4.5V. When the output current is 4mA, the output voltage is typically (MVDD – 1.3) V at MVDD=3.0V and typically (MVDD – 1.5) V at MVDD=4.5V. When PMMP bit is "0", the output current is not supplied.

PMMP bit	MPWR pin	
0	Pull-down to VSS1 with 5.3kΩ(typ.)	(default)
1	Output	

Table 16. MIC Power

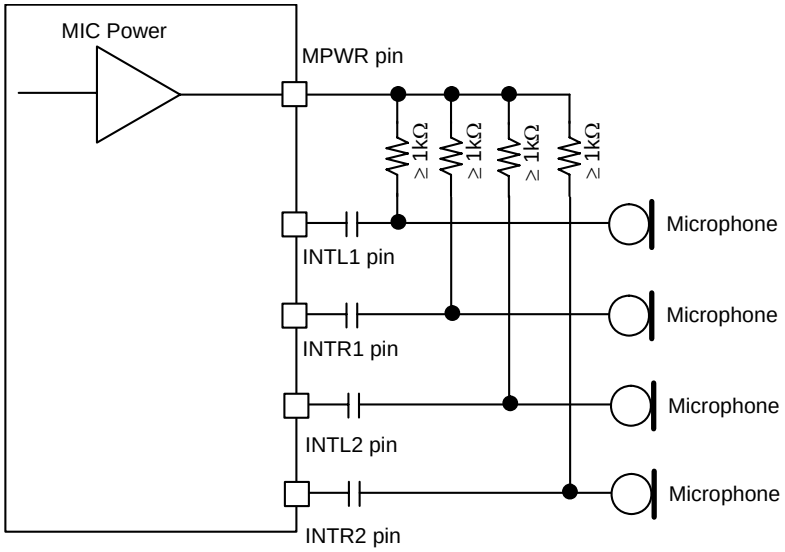


Figure 22. MIC Block Circuit example

■ MIC Sensitivity Compensation

The AK4691 has MIC sensitivity (Interchannel gain mismatch) compensation function. The gain of each channel for compensation is set by the resister as shown in Table 17. This function is enabled when Pre-Amp gain is from +18dB to +32.4dB. It is ignored when Pre-Amp gain is 0dB or -4.4dB.

Register	Input pin
MGL12-10 bits	INTL1/EXTL1
MGR12-10 bits	INTR1/EXTR1
MGL22-20 bits	INTL2/EXTL2
MGR22-20 bits	INTR2/EXTR2

Table 17. Relationship between register and input pin

MGL12 bit MGR12 bit MGL22 bit MGR22 bit	MGL11 bit MGR11 bit MGL21 bit MGR21 bit	MGL10 bit MGR10 bit MGL20 bit MGR20 bit	Gain	
0	0	0	+2dB	
0	0	1	+1dB	
0	1	0	0dB	(default)
0	1	1	-1dB	
1	0	0	-2dB	
1	0	1	N/A	
1	1	0		
1	1	1		

Table 18. MIC Sensitivity Compensation function (N/A: Not available)

■ Analog Mixing Circuit for Recording Block

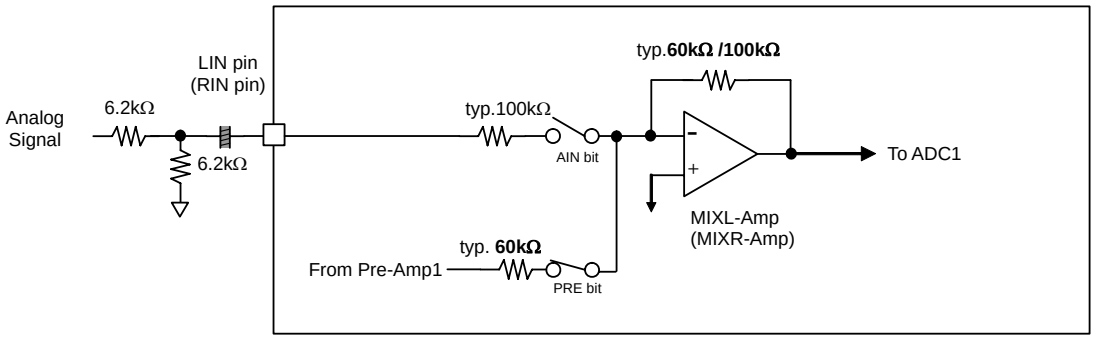


Figure 23. Analog Mixing Circuit for Recording Block

1. LINE Input

Input resistance of LIN and RIN pins are typically 100kΩ and centered around the VCOM voltage. When the input voltage exceeds +2dBV, the input signals should be attenuated down to –3.7dBV at AVDD=3.0V by external resistor divider.

When AIN bit is "1", LIN and RIN pins are selected. The MIX-Amp gain is changed by FB bit.

FB bit	Gain	
0	-4.4dB	(default)
1	0dB	

Table 19. MIX-Amp gain at LINE Input

2. MIX-Amp

MIX1-Amp is powered-up when PMADC1 bit = "1". MIX-Amp mixes the MIC input and the line input. Mixing ratio is "1:0.6" at FB bit = "0" and "1.67:1" at FB bit = "1".

3. Polarity

INTL1/INTR1, INTL2/INTR2, EXTL1/EXTR1, EXTL2/EXTR2, and LIN/RIN pins output non-inverted input signals from ADC.

Signal Path	Polarity
INTL1/INTR1 → ADC1 INTL2/INTR2 → ADC2	Non-inverted
EXTL2/EXTR2 → ADC1 EXTL2/EXTR2 → ADC2	Non-inverted
LIN/RIN → ADC1	Non-inverted

Table 20. Polarity of Recording Block

4. Mono Analog Loopback Selector

When Pre-Amp gain is +18dB, +20dB, +24dB or +28dB, signal from Lch Pre-Amp #1 (MICL1 bit), Rch Pre-Amp #1 (MICR1 bit), and Lch Pre-Amp #2 (MICL2 bit) can be output from the LOUT pin. This path does not pass through the block of MIC sensitivity compensation. MICL1 bit is enabled at PMMICL1 = PMLO bits = "1". MICR1 bit is enabled at PMMICR1 = PMLO bits = "1". MICL2 bit is enabled at PMMICL2 = PMLO bits = "1".

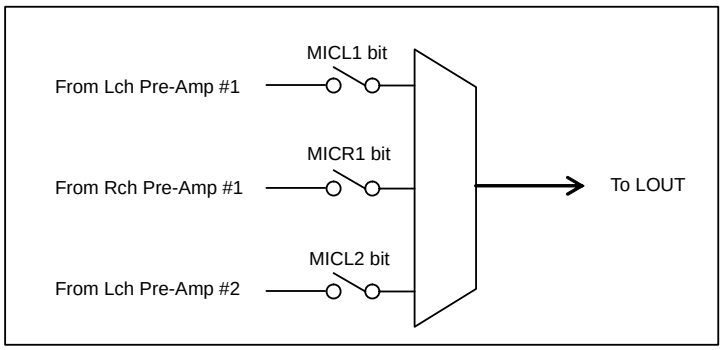


Figure 24. Mono Analog Loopback Selector

5. MONO Mode

ADC1 and ADC2 support mono data output. The both output mode of ADC1 and ADC2 are selected by ADM1-0 bits. This conversion to mono data from stereo data is done before window noise reduction circuit (Figure 25).

ADM1 bit	ADM0 bit	ADC output		
		Lch	Rch	
0	0	Lch Data	Rch Data	(default)
0	1	Lch Data	Lch Data	
1	0	Rch Data	Rch Data	
1	1	(L+R)/2	(L+R)/2	

Table 21. ADC output data

After setting ADM1-0 bits, ADC should be power-up by setting PMADC1 bit = "1" or PMADC2 bit = "1". When changing ADM1-0 bits during ADC is working, the pop noise may occur.

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@ fs = 48kHz) and scales with sampling rate (fs). ADC1 and DAC use common HPF. When ADC side is powered-up (PMADC1 bit = "1" or PMADC2 bit = "1"), the HPF of ADC1 is enabled but the HPF of DAC is disabled. When ADC side is powered-down (PMADC1 = PMADC2 bits = "0") and DAC is powered-up (PMDAC bit = "1"), the HPF of DAC is enabled (@ HPFN bit = "0"). When the HPF of DAC is enabled, ON/OFF of the HPF can be selected by HPFN bit. When changing HPFN bit, DAC should be powered-down. When ADC side is powered-up, HPFN bit must be set to "0".

PMADC2-1 bits	PMDAC bit	HPFN bit	HPF
01, 10 or 11	x	1	ADC
00	0	x	OFF
	1	0	DAC
		1	OFF

Table 22. HPF ON/OFF (x: Don't care)

■ Digital EQ/HPF/LPF

The AK4691 has wind-noise reduction filter (FIL1), stereo separation emphasis (FIL3), gain compensation (EQ) and ALC (Automatic Level Control) in digital domain for A/D converted data (Figure 25). ADC1 and ADC2 have FIL1, FIL3, and EQ blocks independently. ALC block is common to ADC1 and ADC2. FIL1, FIL3, and EQ blocks are IIR filters of 1st order. The filter coefficient of FIL3, EQ and FIL1 blocks can be set to any value. Refer to the section of "ALC operation" about ALC.

When only DAC is powered-up, digital EQ/HPF/LPF circuit in ADC1 operates at playback path. When only ADC is powered-up or both ADC and DAC are powered-up, digital EQ/HPF/LPF circuit in ADC1 operates at recording path. Even if the path is switched from recording to playback, the register setting of filter coefficient at recording remains. Therefore, FIL3A, EQA, FIL1A, GN1A, GN0A bits should be set to "0" if digital EQ/HPF/LPF in ADC1 is not used for playback path.

When digital EQ/HPF/LPF blocks change from recording path to playback path, ADC1, ADC2 and DAC (PMADC1=PMADC2=PMDAC bits = "0") should be powered-down.

PMADC2 -1 bits	PMDAC bit	LOOP1-0 bits (Note 50)	Status	Digital EQ/HPF/LPF	
00	0	x	Power-down	Power-down	(default)
	1	x	Playback	Playback path	
01, 10 or 11	0	x	Recording	Recording path	
	1	00	Recording & Playback	Recording path	
01	1	01, 11	Recording Monitor Playback (ADC1 → DAC)	Recording path	
		10	Recording & Playback	Recording path	
10	1	01	Recording & Playback	Recording path	
		10, 11	Recording Monitor Playback (ADC2 → DAC)	Recording path	
				Recording path	
11	1	01, 11	Recording (ADC2) Recording Monitor Playback (ADC1 → DAC)	Recording path	
		10	Recording (ADC1) Recording Monitor Playback (ADC2 → DAC)	Recording path	

Note 50. When LOOP1-0 bits = "10", TDM mode (DIF1-0 bits = "00") is not supported.
Note 51. Stereo emphasis circuit in ADC1 and ADC2 is effective only at stereo operation.

Table 23. Digital EQ/HPF/LPF Circuit Setting (x: Don't care)

When the below recording channels (PMADC2-1 bits = "01" ➔ PMADC2-1 bits = "10" or PMADC2-1 bits = "10" ➔ PMADC2-1 bits = "01") are changed at PMDAC bit = "1, PMADC1 = PMADC2 bits = "11" should be set more than 2/fs.

<Example of Sequence>

a. PMADC2-1 bits = "01" ("10")
b. PMADC2-1 bits = "11"
c. Delay (≥ 2/fs)
d. PMADC2-1 bits = "10" ("01")

FIL3A, EQA, FIL1A, GN1A, and GN0A bits are for ADC1.
FIL3B, EQB, FIL1B, GN1B, and GN0B bits are for ADC2.

FIL3A(FIL3B) coefficient also sets the attenuation of the stereo separation emphasis.

The combination of GN1-0A(GN1-0B) bits (Table 24) and EQA(EQB) coefficient set the compensation gain.

FIL1A(FIL1B) and FIL3A(FIL3B) blocks become HPF when F1ASA(F1ASB) and F3ASA(F3ASB) bits are "0" and become LPF when F1ASA(F1ASB) and F3ASA(F3ASB) bits are "1", respectively.

When EQA(EQB) and FIL1A(FIL1B) bits are "0", EQA(EQB) and FIL1A(FIL1B) blocks become "through" (0dB). When FIL3A(FIL3B) bit is "0", FIL3A(FIL3B) block become "MUTE". When each filter coefficient is changed, each filter should be set to "through" ("MUTE" in case of FIL3A (FIL3B)).

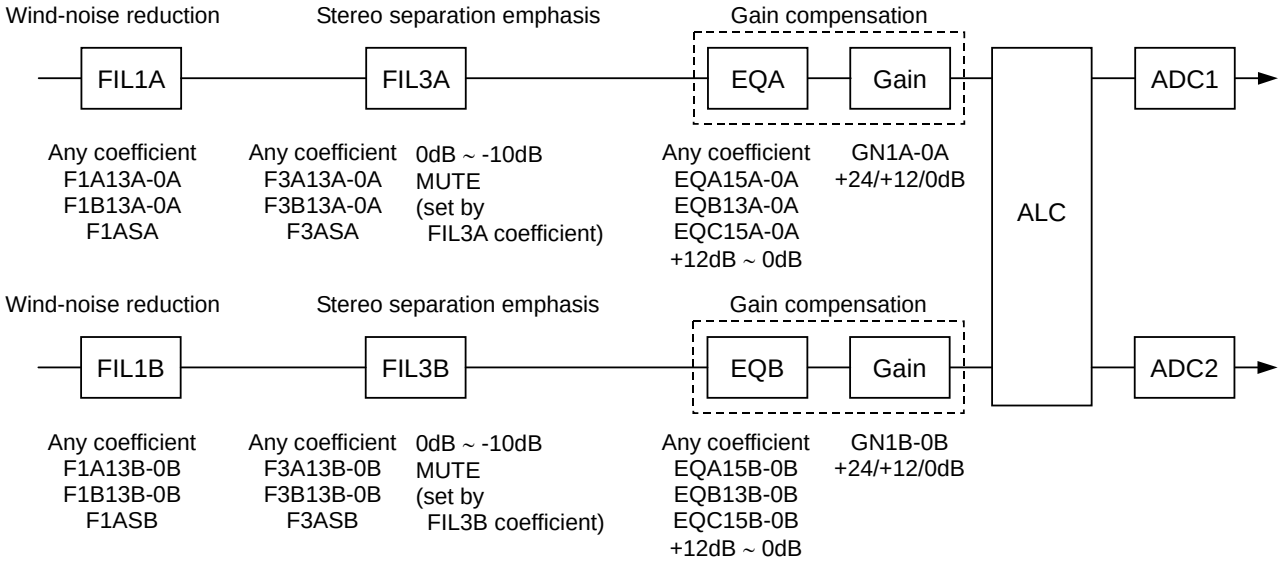


Figure 25. Digital EQ/HPF/LPF

GN1A bit GN1B bit	GN0A bit GN0B bit	Gain	
0	0	0dB	(default)
0	1	+12dB	
1	x	+24dB	

Table 24. Gain select of gain block (x: Don't care)

[Filter Coefficient Setting]

1) When FIL1A(FIL1B) and FIL3A(FIL3B) are set to "HPF"

fs: Sampling frequency
fc: Cut-off frequency
f: Input signal frequency
K: Filter gain [dB] (Filter gain of FIL1A(FIL1B) should be set to 0dB.)

Register setting for ADC1
FIL1A: F1ASA bit = "0", F1A[13:0]A bits =A, F1B[13:0]A bits =B
FIL3A: F3ASA bit = "0", F3A[13:0]A bits =A, F3B[13:0]A bits =B
(MSB=F1A13A, F1B13A, F3A13A, F3B13A; LSB=F1A0A, F1B0A, F3A0A, F3B0A)

Register setting for ADC2
FIL1B: F1ASB bit = "0", F1A[13:0]B bits =A, F1B[13:0]B bits =B
FIL3B: F3ASB bit = "0", F3A[13:0]B bits =A, F3B[13:0]B bits =B
(MSB=F1A13B, F1B13B, F3A13B, F3B13B; LSB=F1A0B, F1B0B, F3A0B, F3B0B)

$$A = 10^{K/20} \times \frac{1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function	Amplitude	Phase
$H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$	$M(f) = A \sqrt{\frac{2 - 2\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$	$\theta(f) = \tan^{-1} \frac{(B+1)\sin(2\pi f/fs)}{1 - B + (B-1)\cos(2\pi f/fs)}$

2) When FIL1A(FIL1B) and FIL3A(FIL3B) are set to "LPF"

fs: Sampling frequency
fc: Cut-off frequency
f: Input signal frequency
K: Filter gain [dB] (Filter gain of FIL1A (FIL1B) should be set to 0dB.)

Register setting for ADC1
FIL1A: F1ASA bit = "0", F1A[13:0]A bits =A, F1B[13:0]A bits =B
FIL3A: F3ASA bit = "0", F3A[13:0]A bits =A, F3B[13:0]A bits =B
(MSB=F1A13A, F1B13A, F3A13A, F3B13A; LSB=F1A0A, F1B0A, F3A0A, F3B0A)

Register setting for ADC2
FIL1B: F1ASB bit = "0", F1A[13:0]B bits =A, F1B[13:0]B bits =B
FIL3B: F3ASB bit = "0", F3A[13:0]B bits =A, F3B[13:0]B bits =B
(MSB=F1A13B, F1B13B, F3A13B, F3B13B; LSB=F1A0B, F1B0B, F3A0B, F3B0B)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan(\pi fc/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc/fs)}{1 + 1 / \tan(\pi fc/fs)}$$

Transfer function	Amplitude	Phase
$H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$	$M(f) = A \sqrt{\frac{2 + 2\cos(2\pi f/fs)}{1 + B^2 + 2B\cos(2\pi f/fs)}}$	$\theta(f) = \tan^{-1} \frac{(B-1)\sin(2\pi f/fs)}{1 + B + (B+1)\cos(2\pi f/fs)}$

3) EQ

fs: Sampling frequency
fc_1: Pole frequency
fc_2: Zero-point frequency
f: Input signal frequency
K: Filter gain [dB] (Maximum +12dB)

Register setting for ADC1
EQA[15:0]A bits =A, EQB[13:0]A bits =B, EQC[15:0]A bits =C
(MSB=EQA15A, EQB13A, EQC15A; LSB=EQA0A, EQB0A, EQC0A)

Register setting for ADC2
EQA[15:0]B bits =A, EQB[13:0]A bits =B, EQC[15:0]B bits =C
(MSB=EQA15B, EQB13B, EQC15B; LSB=EQA0B, EQB0B, EQC0B)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad B = \frac{1 - 1 / \tan(\pi fc_1/fs)}{1 + 1 / \tan(\pi fc_1/fs)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi fc_2/fs)}{1 + 1 / \tan(\pi fc_1/fs)}$$

Transfer function	Amplitude	Phase
$H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$	$M(f) = \sqrt{\frac{A^2 + C^2 + 2ACcos(2\pi f/fs)}{1 + B^2 + 2Bcos(2\pi f/fs)}}$	$\theta(f) = \tan^{-1}\frac{(AB-C)sin(2\pi f/fs)}{A + BC + (AB+C)cos(2\pi f/fs)}$

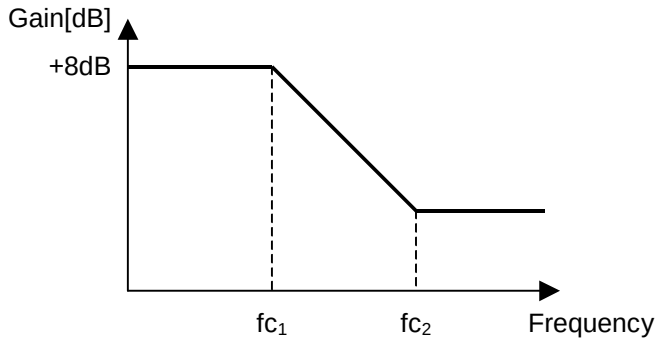
[Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]
X = (Real number of filter coefficient calculated by the equations above) x 2^{13}

X should be rounded to integer, and then should be translated to binary code (2's complement).
MSB of each filter coefficient setting register is sine bit.

[Filter Coefficient Setting Example]

1) FIL1Ablock
Example: HPF, fs=44.1kHz, fc=100Hz
F1ASAbit = "0"
F1A[13:0]A bits = 01 1111 1100 0110
F1B[13:0]A bits = 10 0000 0111 0100

2) EQA block
Example: fs=44.1kHz, fc_1=300Hz, fc_2=3000Hz, Gain=+8dB



EQA[15:0]A bits = 0000 1001 0110 1110
EQB[13:0]A bits = 10 0001 0101 1001
EQC[15:0]A bits = 1111 1001 1110 1111

■ ALC Operation

The ALC (Automatic Level Control) is operated by ALC block when ALC bit is "1". The ALC block is common to ADC1 and ADC2. When only DAC is powered-up, ALC circuit operates at playback path. When only ADC1 or ADC2 is powered-up or ADC1, ADC2, and DAC are powered-up, ALC circuit operates at recording path.

PMADC2 -1 bits	PMDAC bit	LOOP1-0 bits (Note 52)	Status	ALC	
00	0	x	Power-down	Power-down	(default)
	1	x	Playback	Playback path	
01, 10 or 11	0	x	Recording	Recording path	
	1	00	Recording & Playback	Recording path	
01	1	01, 11	Recording Monitor Playback (ADC1 → DAC)	Recording path	
		10	Recording & Playback	Recording path	
10	1	01	Recording & Playback	Recording path	
		10, 11	Recording Monitor Playback (ADC2 → DAC)	Recording path	
				Recording path	
11	1	01, 11	Recording (ADC2) Recording Monitor Playback (ADC1 → DAC)	Recording path	
		10	Recording (ADC1) Recording Monitor Playback (ADC2 → DAC)	Recording path	

Note 52. When LOOP1-0 bits = "10", TDM mode (DIF1-0 bits = "00") is not supported.
Table 25. ALC Setting (x: Don't care)

1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch in ADC1 and ADC2 exceeds the ALC limiter detection level (Table 26), the IVL and IVR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (Table 27). The IVL and IVR are then set to the same value for both channels.

When ZELMN bit = "0" (zero cross detection is enabled), the IVL and IVR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 28). When ALC output level exceeds full-scale at LFST bit = "1", IVL and IVR values are immediately (Period: 1/fs) changed. When ALC output level is less than full-scale, IVL and IVR values are changed at the individual zero crossing point of each channels or at the zero crossing timeout. When LFST bit = "1", the attenuation level is fixed to 1 step regardless of the setting of LMAT1-0 bits.

When ZELMN bit = "1" (zero cross detection is disabled), IVL and IVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuate operation is executed continuously until the input signal level becomes ALC limiter detection level (Table 26) or less. After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

The ALC operation corresponds to the impulse noise. When the impulse noise is input at ZELNN bit = "0", the ALC limiter operation becomes faster than the setting of ZTM1-0 bits (fast limiter operation). The speed of fast limiter operation is set by RFST1-0 bits (Table 32).

LMTH1 bit	LMTH0 bit	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ −2.5dBFS	−2.5dBFS > ALC Output ≥ −4.1dBFS	(default)
0	1	ALC Output ≥ −4.1dBFS	−4.1dBFS > ALC Output ≥ −6.0dBFS	
1	0	ALC Output ≥ −6.0dBFS	−6.0dBFS > ALC Output ≥ −8.5dBFS	
1	1	ALC Output ≥ −8.5dBFS	−8.5dBFS > ALC Output ≥ −12dBFS	

Table 26. ALC Limiter Detection Level / Recovery Counter Reset Level

ZELMN bit	LMAT1 bit	LMAT0 bit	ALC Limiter ATT Step				
			ALC Output ≥ LMTH	ALC Output ≥ FS	ALC Output ≥ FS + 6dB	ALC Output ≥ FS + 12dB	
0	0	0	1step (0.375dB)	1step (0.375dB)	1step (0.375dB)	1step (0.375dB)	(default)
	0	1	2 step (0.75dB)	2 step (0.75dB)	2 step (0.75dB)	2 step (0.75dB)	
	1	0	2 step (0.75dB)	4 step (1.5dB)	4 step (1.5dB)	8 step (3.0dB)	
	1	1	1step (0.375dB)	2 step (0.75dB)	4 step (1.5dB)	8 step (3.0dB)	
1	x	x	1 step (0.375dB)	1 step (0.375dB)	1 step (0.375dB)	1 step (0.375dB)	

Table 27. ALC Limiter ATT Step (x: Don't care)

ZTM1 bit	ZTM0 bit		Zero Crossing Timeout Period			
			8kHz	32kHz	48kHz	
0	0	128/fs	16ms	4ms	2.7ms	(default)
0	1	256/fs	32ms	8ms	5.3ms	
1	0	512/fs	64ms	16ms	10.7ms	
1	1	1024/fs	128ms	32ms	21.3ms	

Table 28. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits (Table 29) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 26) during the wait time, the ALC recovery operation is executed. The IVL and IVR values are automatically incremented by RGAIN1-0 bits (Table 30) up to the set reference level (Table 31) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 28). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation period is set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, the ALC recovery operation waits until WTM2-0 period and the next recovery operation is executed.

For example, when the current IVOL value is 30H and RGAIN1-0 bits are set to "01", IVOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVOL value exceeds the reference level (REF7-0 bits), the IVOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation (Fast Recovery Operation). When large noise is input to microphone instantaneously, the quality of small signal level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 32).

WTM2 bit	WTM1 bit	WTM0 bit		ALC Recovery Operation Waiting Period			
				8kHz	32kHz	48kHz	
0	0	0	128/fs	16ms	4ms	2.7ms	
0	0	1	256/fs	32ms	8ms	5.3ms	
0	1	0	512/fs	64ms	16ms	10.7ms	
0	1	1	1024/fs	128ms	32ms	21.3ms	
1	0	0	2048/fs	256ms	64ms	42.7ms	(default)
1	0	1	4096/fs	512ms	128ms	85.3ms	
1	1	0	8192/fs	1024ms	256ms	170.7ms	
1	1	1	16384/fs	2048ms	512ms	341.3ms	

Table 29. ALC Recovery Operation Waiting Period

RGAIN1 bit	RGAIN0 bit	GAIN STEP		
0	0	1 step	0.375dB	(default)
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 30. ALC Recovery GAIN Step

REF7-0 bits	GAIN(dB)		
	MIC (GSEL bit = "0")	LINE (GSEL bit = "1")	
F1H	+36.0	+6.0	
F0H	+35.625	+5.625	
EFH	+35.25	+5.25	
:	:	:	
E2H	+30.375	+0.375	
E1H	+30.0	0	(default)
E0H	+29.625	-0.375	
DFH	+29.25	-0.75	
:	:	:	
04H	-52.875	-82.875	
03H	-53.25	-83.25	
02H	-53.625	-83.625	
01H	-54.0	-84.0	
00H	MUTE	MUTE	

Table 31. Reference Level at ALC Recovery operation (0.375dB step)

RFST1 bit	RFST0 bit	Limiter / Recovery Speed	
0	0	4 times	(default)
0	1	8 times	
1	0	16 times	
1	1	N/A	

Table 32. Fast Limiter / Recovery Speed Setting (N/A: Not Available)

3. Example of ALC Operation

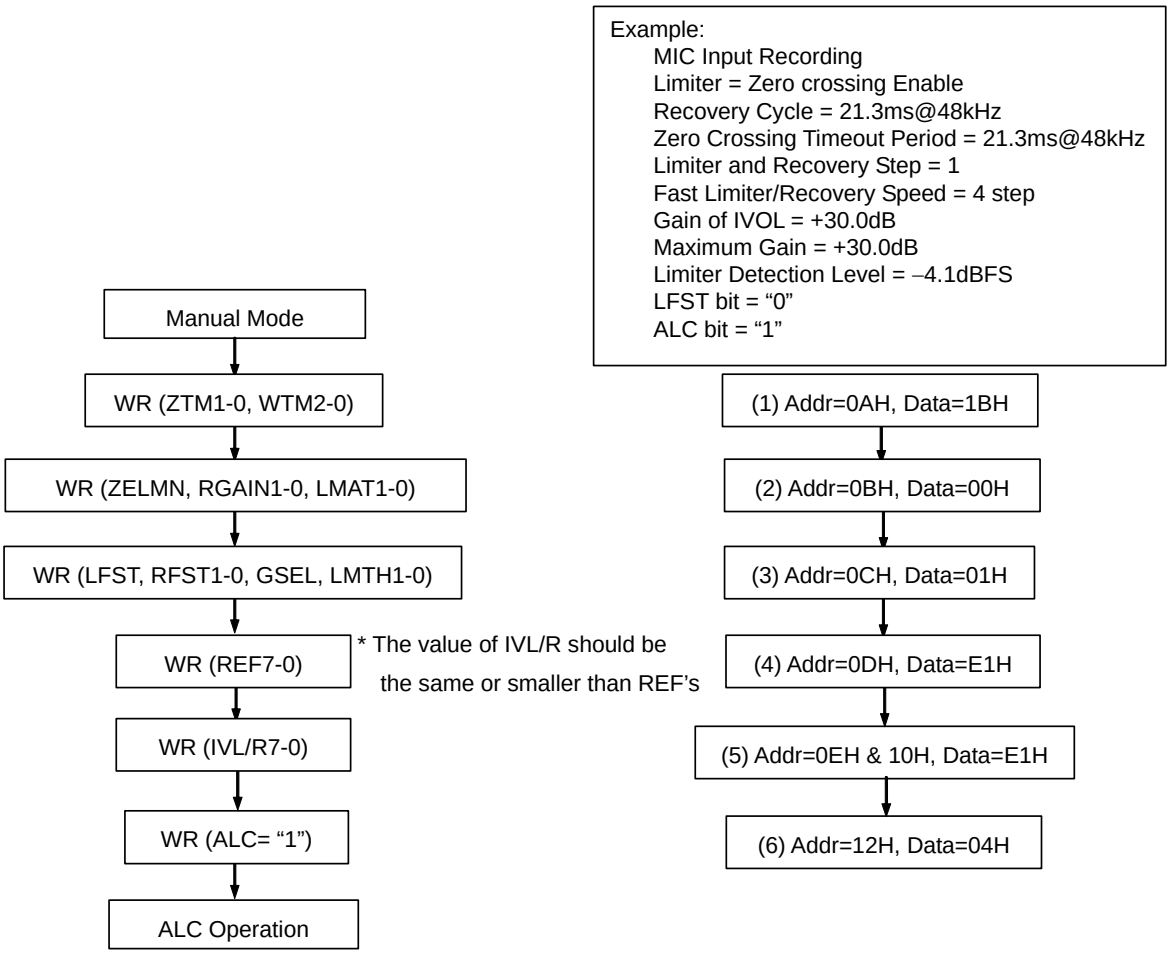
Table 33 shows the examples of the ALC setting for MIC recording.

Register Name	Comment	fs=8kHz		fs=48kHz	
		Data	Operation	Data	Operation
LMTH1-0	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	01	32ms	11	21.3ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same or larger data to ZTM1-0 bits	001	32ms	011	21.3ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0, IVR7-0	Gain of IVOL	E1H	+30dB	E1H	+30dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
ALC	ALC enable	1	Enable	1	Enable

Table 33. Example of the ALC setting

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0" or PMADC1=PMADC2 = PMDAC bits = "0".

- **LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN, GSEL, RFST1-0, LFST bits**



Note : WR : Write

Figure 26. Registers set-up sequence at ALC operation

■ FADEIN Mode

In FADEIN Mode, the IVL/R values increase gradually by the step set by FDATT1-0 bits when FDIN bit changes from "0" to "1". The FADEIN period is set by REF7-0, FDATT1-0 (Table 35) and FDTM1-0 (Table 34) bits. The FADEIN operation is executed by the zero crossing detection. The operation stops when the IVL/R values become the REF value or the limiter detection level (LMTH1-0). If the limiter operation is executed during FADAIN period, the FADEIN operation stops and the ALC operation starts.

NOTE: When FDIN and FDOUT bits are set to "1" at the same time, FADEOUT operation is prior to FADEIN operation.

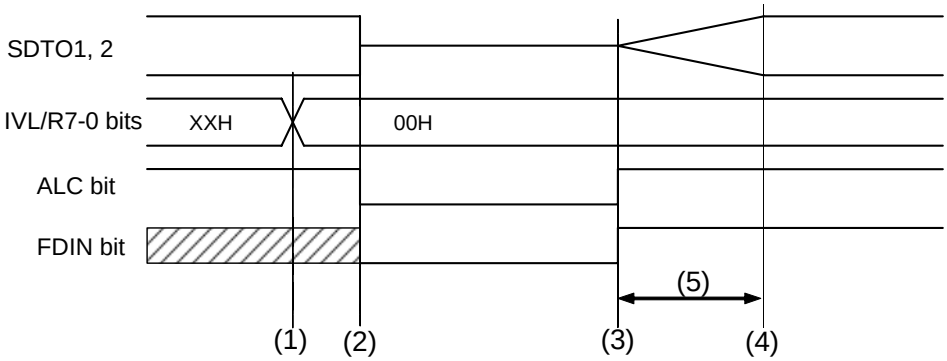


Figure 27. Example for controlling sequence in FADEIN operation

(1) WR(IVL/R7-0 bits = 00H) : IVL/R are changed to "MUTE".
(2) WR (ALC bit = FDIN bit = "0"): The ALC operation is disabled. To start the FADEIN operation, FDIN bit is written in "0".
(3) WR (ALC bit = FDIN bit = "1"): The FADEIN operation starts. The IVL/R is fade-in from MUTE state.
(4) The FADEIN operation is repeated until the limiter detection level (LMTH1-0 bits) or the reference level (REF7-0 bits). After completing the FADEIN operation, the ALC operation starts.
(5) FADEIN time is set by REF7-0, FDTM1-0, and FDATT bits
e.g. REF7-0 = E1H(225 dec), FDTM1-0 = "01" (= 42.7ms @ fs = 48kHz), FDATT1-0 = 2 step
(225 x FDTM1-0) / FDATT1-0 = 225 x 42.7ms /2 = 4.8s

FDTM1 bit	FDTM0 bit		FADEIN/OUT Period			
			8kHz	32kHz	48kHz	
0	0	1024/fs	128ms	32ms	21.3ms	
0	1	2048/fs	256ms	64ms	42.7ms	(default)
1	0	2304/fs	288ms	72ms	48ms	
1	1	2560/fs	320ms	80ms	53.3ms	

Table 34. FADEIN/OUT Period

FDATT1 bit	FDATT0 bit	ATT STEP	
0	0	1	(default)
0	1	2	
1	0	3	
1	1	4	

Table 35. FADEIN/OUT ATT Step Setting

■ FADEOUT Mode

In FADEOUT mode, the present IVL/R values decrease gradually down to the MUTE state when FDOUT bit changes from "0" to "1". The operation is executed by the zero crossing detection. If the large signal is supplied to the ALC circuit during the FADEOUT operation, the ALC limiter operation starts. However, the total time of the FADEOUT operation is the same time, even if the limiter operation is executed. The period of FADEOUT is set by FDTM1-0 bits (Table 34), the number of step is set by FDATT1-0 bits (Table 35). When FDOUT bit changes into "0" during the FADEOUT operation, the ALC operation starts from the present IVL/R values. When FDOUT and ALC bits change into "0" at the same time, the FADEOUT operation stops and the IVL/R keeps the value at that time.

NOTE: When FDIN and FDOUT bits are set to "1" at the same time, FADEOUT operation is prior to FADEIN operation.

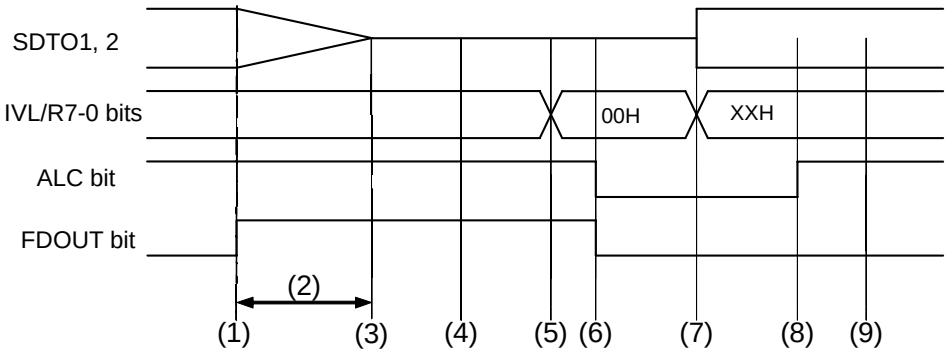


Figure 28. Example for controlling sequence in FADEOUT operation

(1) WR (FDOUT bit = "1"): The FADEOUT operation starts. Then ALC bit should be always "1".
(2) FADEOUT time is set by REF7-0, FDTM1-0 and FDATT bits.
e.g. REF7-0 = E1H(225 dec), FDTM1-0 = "01" (= 42.7ms @ fs = 48kHz), FDATT1-0 = 2 step
(225 x FDTM1-0) / FDATT1-0 = 225 x 42.7ms / 2 = 4.8s
(3) The FADEOUT operation is completed. The IVL/R values are the MUTE state. If FDOUT bit keeps "1", the IVL/R values keep the MUTE state.
(4) Analog and digital outputs are muted externally. Then the IVL/R values are MUTE state.
(5) WR (IVL/R7-0 bits = 00H) : IVL/R are changed to "MUTE".
(6) WR (ALC bit = FDOUT bit = "0"): Exit the ALC and FADEOUT operations
(7) WR (IVL/R7-0 bits = XXH): The IVL/R value should be set to the same or smaller than REF's.
(8) WR (ALC bit = "1", FDOUT bit = "0"): The ALC operation restarts. But the ALC bit should be written until completing zero crossing detection operation of IVL/R.
(9) Release an external mute function for analog and digital outputs.

■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode when ALC bit is "0". This mode is for the case shown below. The volume setting is common to ADC1 and ADC2 and has two tables that are LINE and MIC.

1. After exiting reset state, when setting up the registers for the ALC operation (ZTM1-0, LMTH1-0 and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.
3. When IVOL is used as a manual volume.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 36). The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits. If IVL7-0 or IVR7-0 bits are written during PMADC1 = PMADC2 = PMDAC bits = "0", IVOL operation starts with the written values at the end of the ADC/DAC initialization cycle after PMADC1, PMADC2, or PMDAC bit is changed to "1".

Even if the path is switched from recording to playback, the register setting of IVL/R remains. Therefore, IVL7-0 and IVR7-0 bits should be set to "91H" (0dB) at GSEL bit = "0".

IVL7-0 bits IVR7-0 bits	GAIN(dB)		
	MIC (GSEL bit = "0")	LINE (GSEL bit = "1")	
F1H	+36.0	+6.0	
F0H	+35.625	+5.625	
EFH	+35.25	+5.25	
:	:	:	
E2H	+30.375	+0.375	
E1H	+30.0	0	(default)
E0H	+29.625	-0.375	
DFH	+29.25	-0.75	
:	:	:	
04H	-52.875	-82.875	
03H	-53.25	-83.25	
02H	-53.625	-83.625	
01H	-54.0	-84.0	
00H	MUTE	MUTE	

Table 36. Input Digital Volume Setting

When writing to the IVL7-0 and IVR7-0 bits continuously, the control register should be written in an interval more than zero crossing timeout. If not, IVL and IVR are not changed since zero-crossing counter is reset at every write operation. If the same register value as the previous write operation is written to IVL and IVR, this write operation is ignored and zero-crossing counter is not reset. Therefore, IVL and IVR can be written in an interval less than zero crossing timeout.

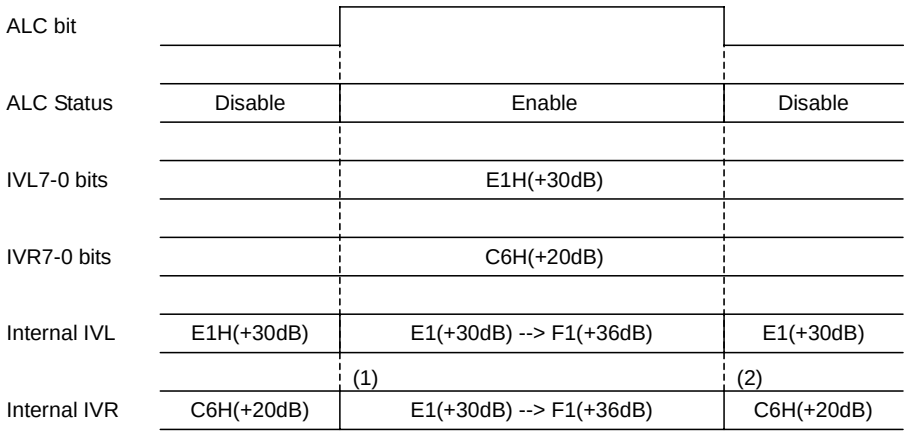


Figure 29. IVOL value during ALC operation (GSEL bit = "0")

(1) The IVL value becomes the start value if the IVL and IVR are different when the ALC starts.
(2) Writing to IVL and IVR registers (0EH, 10H) is ignored during ALC operation. After ALC is disabled, the IVOL changes to the last written data by zero crossing or timeout. When ALC is enabled again, ALC bit should be set to "1" with an interval more than zero crossing timeout period after ALC bit = "0".

■ De-emphasis Filter

The AK4691 includes the digital de-emphasis filter (tc = 50/15μs) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 37).

DEM1 bit	DEM0 bit	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 37. De-emphasis Control

■ Bass Boost Function

The BST1-0 bits control the amount of low frequency boost applied to the DAC output signal (Table 38). If the BST1-0 bits are set to "01" (MIN Level), use a 47µF capacitor for AC-coupling. If the boosted signal exceeds full scale, the analog output clips to the full scale. Figure 30 shows the boost frequency response at –20dB signal input.

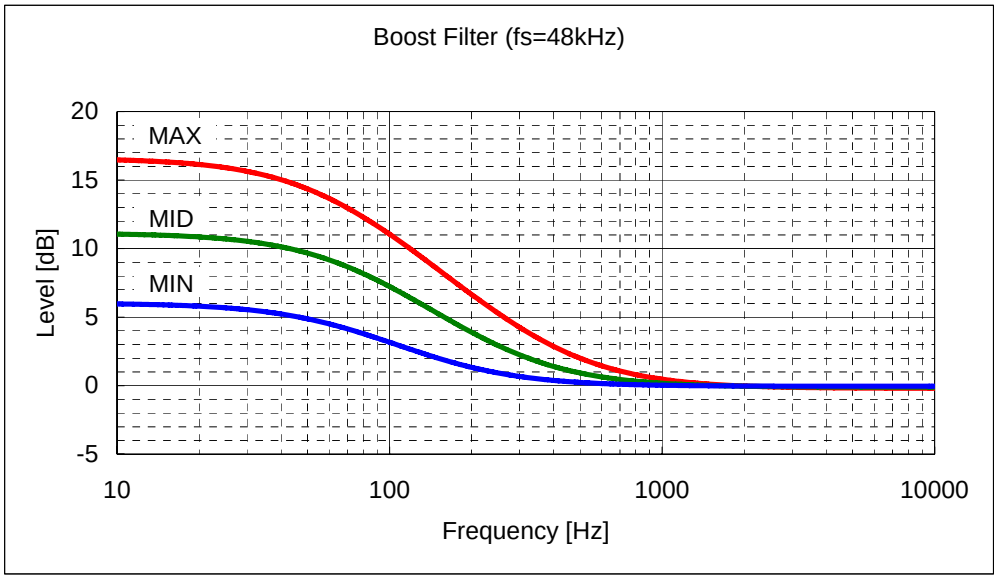


Figure 30. Bass Boost Frequency Response (fs = 48kHz)

BST1 bit	BST0 bit	Mode	
0	0	OFF	(default)
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 38. Bass Boost Control

■ Digital Output Volume

The AK4691 has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the DVL7-0 and DVR7-0 bits. The volume is placed in front of a DAC block. The input data of DAC is changed from +12 to –115dB or MUTE. When the DVOLC bit = "1", the DVL7-0 bits control both Lch and Rch attenuation levels. When the DVOLC bit = "0", the DVL7-0 bits control Lch level and DVR7-0 bits control Rch level. This volume has a soft transit function. The DVTM bit sets the transition time between set values of DVL/R7-0 bits as either 1061/fs or 256/fs (Table 40). When DVTM bit = "0", a soft transition between the set values occurs (1062 levels). It takes 1061/fs (=22.1ms@fs=48kHz) from 00H (+12dB) to FFH (MUTE).

DVL/R7-0 bits	Gain	
00H	+12.0dB	
01H	+11.5dB	
02H	+11.0dB	
:	:	
18H	0dB	(default)
:	:	
FDH	–114.5dB	
FEH	–115.0dB	
FFH	MUTE (–∞)	

Table 39. Digital Volume Code Table

DVTM bit	Transition time between DVL/R7-0 bits = 00H and FFH			
	Setting	fs=8kHz	fs=48kHz	
0	1061/fs	133ms	22.1ms	(default)
1	256/fs	32ms	5.3ms	

Table 40. Transition Time Setting of Digital Output Volume

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit is changed to "1", the output signal is attenuated by –∞ ("0") during the cycle set by the DVTM bit. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the value set by the DVL/R7-0 bits during the cycle set of the DVTM bit. If the soft mute is cancelled within the cycle set by the DVTM bit after starting the operation, the attenuation is discontinued and returned to the value set by the DVL/R7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transmission (Figure 31).

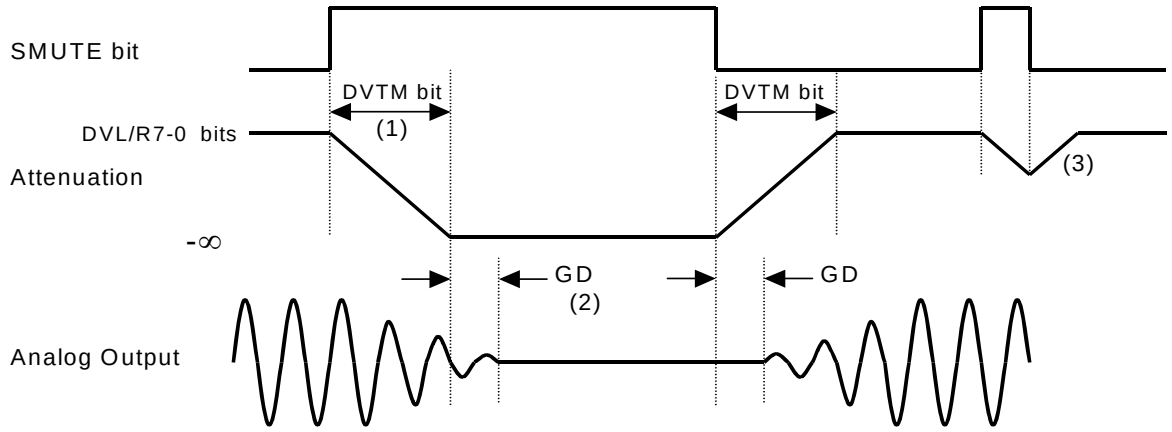


Figure 31. Soft Mute Function

(1) The output signal is attenuated until –∞ ("0") by the cycle set by the DVTM bit.
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within the cycle set by the DVTM bit, the attenuation is discounted and returned to the value set by the DVL/R7-0 bits.

■ Analog Mixing: Mono Input

When the PMBP bit is set to "1", the mono input is powered-up. When the BEEPS bit is set to "1", the input signal from the BEEP pin is output to Speaker-Amp. When the BEEPH bit is set to "1", the input signal from the BEEP pin is output to Headphone-Amp. When the BEEPL bit is set to "1", the input signal from the BEEP pin is output to the stereo line output amplifier. The external resister Ri adjusts the signal level of BEEP input. Table 41, Table 42 and Table 43 show the typical gain example at R_i = 20kΩ. This gain is in inverse proportion to R_i.

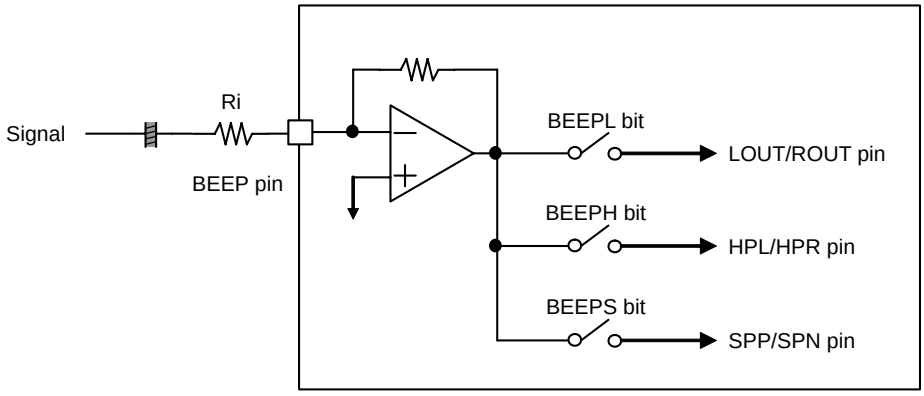


Figure 32. Block Diagram of BEEP pin

LVOL2 bit	LVOL1 bit	LVOL0 bit	BEEP → LOUT/ROUT	
0	0	0	0dB	(default)
0	0	1	+2dB	
0	1	0	+5.9dB	
0	1	1	+6.5dB	
1	0	0	+7.1dB	
1	0	1	N/A	
1	1	x	N/A	

Table 41. BEEP Input → LOUT/ROUT Output Gain (typ) at R_i = 20kΩ (N/A: Not available)

HPG bit	BEEP → HPL/HPR	
0	–20dB	(default)
1	–16.4dB	

Table 42. BEEP Input → Headphone-Amp Output Gain (typ) at R_i = 20kΩ

SPKG1-0 bits	BEEP → SPP/SPN		
	ALC bit = "0"	ALC bit = "1"	
00	+4.43dB	+6.43dB	(default)
01	+6.43dB	+8.43dB	
10	+10.65dB	+12.65dB	
11	+12.65dB	+14.65dB	

Table 43. BEEP Input → Speaker-Amp Output Gain (typ) at R_i = 20kΩ

■ Stereo Line Output (LOUT/ROUT pins)

When DACL bit is "1", Lch/Rch signal of DAC is output from the LOUT/ROUT pins which is single-ended. When DACL bit is "0", output signal is muted and LOUT/ROUT pins output LVCM voltage. The load impedance is 10kΩ (min.). LVOL2-0 bits set the gain of stereo line output. The Power supply voltage for LINEOUT-Amp is supplied from LVDD pin. The output level of LINEOUT is constant regardless of LVDD voltage. When the output voltage of LVDD pin is low, the distortion of LINEOUT degrades. Stereo LINEOUT has two kinds of power-save mode in order to support a common connector of LINEIN/OUT.

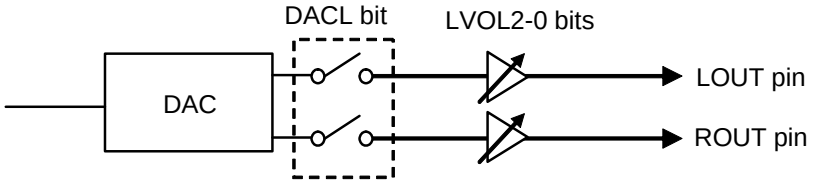


Figure 33. Stereo Line Output

LVOL2 bit	LVOL1 bit	LVOL0 bit	Gain	AVDD voltage	LINEOUT	
0	0	0	0dB	3.0V	-3.9dBV	(default)
0	0	1	+2dB	3.0V	-1.9dBV	
0	1	0	+5.9dB	3.0V	+2dBV	
0	1	1	+6.5dB	2.8V	+2dBV	
1	0	0	+7.1dB	2.6V	+2dBV	
1	0	1	N/A			
1	1	x				

Table 44. Stereo Line Output Volume Setting (x: Don't care, N/A: Not Available)

1. LMODE bit = "1" (When Line input and Line output are not used as a common connector.)

When the PMLO bit = LOPS bit = "0", the stereo line output enters power-down mode and the output is pulled-down to VSS4 by 100kΩ (typ). When the LOPS bit is "1", stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit at LOPS bit = "1". In this case, output signal line should be pulled-down to VSS4 by 20kΩ after AC coupled as Figure 34. Rise/Fall time is 300ms (max) at C=1μF. When PMLO bit = "1" and LOPS bit = "0", stereo line output is in normal operation.

LOPS bit	PMLO bit	Mode	LOUT/ROUT pins	
0	0	Power-down	Pull-down to VSS4	(default)
	1	Normal Operation	Normal Operation	
1	0	Power-save	Fall down to VSS4	
	1	Power-save	Rise up to LVCM	

Table 45. Stereo Line Output Mode Select @ LMODE bit = "1"

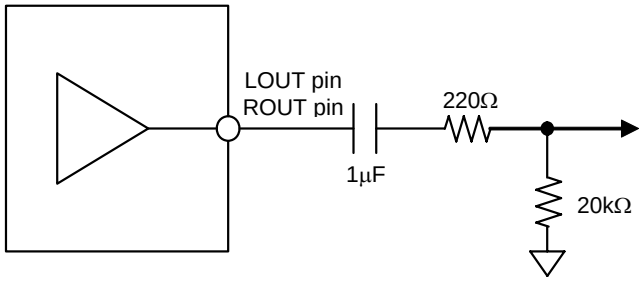


Figure 34. External Circuit for Stereo Line Output (in case of using Pop Reduction Circuit)

LVDD	Rising Time (Note 53)		Falling Time (Note 54)	
	typ.	max	typ.	max.
3.6V	200ms	300ms	200ms	300ms
5.5V	220ms	400ms	260ms	440ms

Note 53. Rising time of stereo line output (0.9 x LVCM)

Note 54. Falling time of stereo line output (This time is until the voltage between 220Ω and 20kΩ resistors as shown in Figure 34 becomes less than 50mV.)

Table 46. Rising / Falling time of stereo line output

[Stereo Line Output Control Sequence (in case of using Pop Reduction Circuit)]

E.g. In case of LVDD = 3.6V

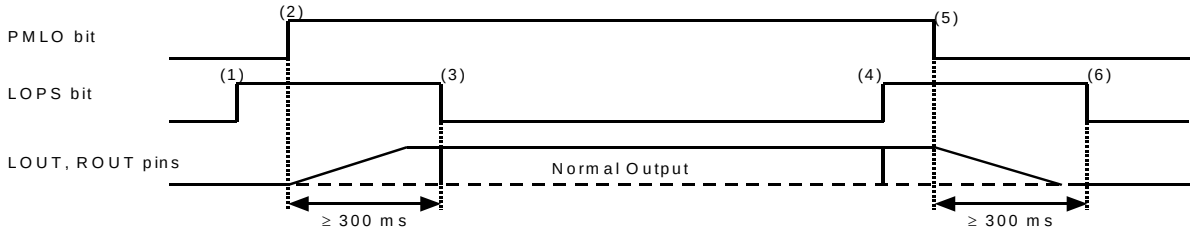


Figure 35. Stereo Line Output Control Sequence (in case of using Pop Reduction Circuit)

(1) Set LOPS bit = "1". Stereo line output enters the power-save mode.
(2) Set PMLO bit = "1". Stereo line output exits the power-down mode.
LOUT and ROUT pins rise up to LVCM voltage. Rise time is 200ms (max 300ms) at C=1μF.
(3) Set LOPS bit = "0" after LOUT and ROUT pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
(4) Set LOPS bit = "1". Stereo line output enters power-save mode.
(5) Set PMLO bit = "1". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to VSS4. Fall time is 200ms (max 300ms) at C=1μF.
(6) Set LOPS bit = "0" after LOUT and ROUT pins fall down. Stereo line output exits the power-save mode.

2. LMODE bit = "0" (When Line input and Line output are used as a common connector.)

When PMLO bit bit = "0", the stereo line output enters power-down mode and the output becomes Hi-Z status. When the LOPS bit is "1", stereo line output (LOUT/ROUT pins) enters power-save mode and outputs LVCM voltage via an internal resistor (typ. 200kΩ). In power-save mode, the signal path of stereo line output (DACL, BEEPL, MICL1, MICL2, and MICR1 bits) is OFF. Pop noise can be decreased by using power-save mode. When using line input, the AK4691 should be in the power-save mode.

PMLO bit	LOPS bit	Mode	LOUT/ROUT pins	
0	x	Power-down	Hi-Z	(default)
1	1	Power-save	LVCM	
	0	Normal Operation	Normal Operation	

Table 47. External Circuit for Stereo Line Output @ LMODE bit = "0" (x: Don't care)

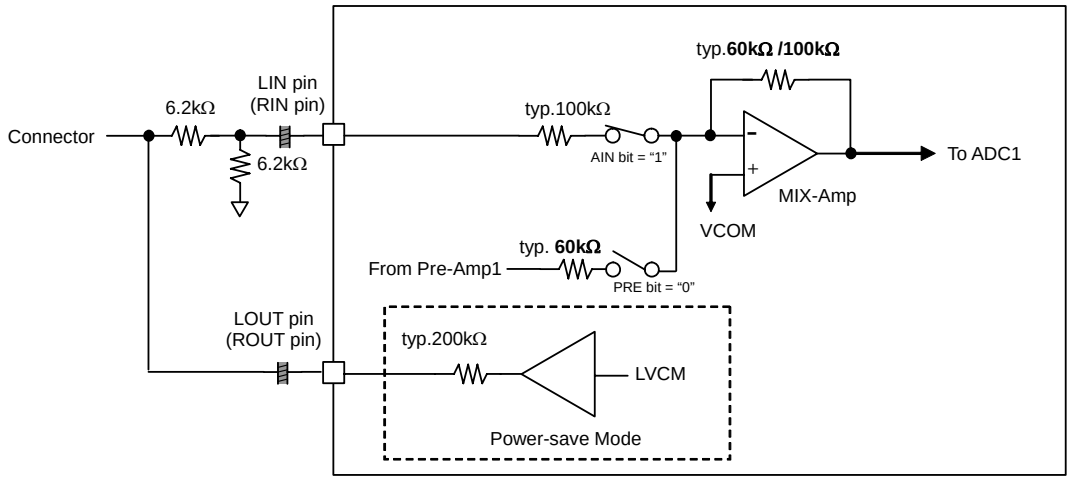


Figure 36. Connection Example (When Line input and Line output are used as a common connector.)

■ Headphone Output

Power supply voltage for the Headphone-Amp is supplied from the LVDD pin and centered on the LVDD/2 voltage. The load resistance is 16Ω (min). HPG bit selects the output voltage (Table 48).

HPG bit	0	1
Output Voltage [Vpp]	0.6 x AVDD	0.91 x AVDD

Table 48. Headphone-Amp Output Voltage

When the HPMTN bit is "0", the common voltage of Headphone-Amp falls and the outputs (HPL and HPR pins) become to "L" (VSS4). When HPMTN bit is "1", the common voltage rises to LVDD/2. A capacitor between the MUTET pin and ground reduces pop noise at power-up. Rise/Fall time constant is in proportional to LVDD voltage and the capacitor at the MUTET pin.

LVDD	Capacitor value of MUTET pin	HPMTN bit= "0" → "1" (Note 55)		HPMTN bit = "1" → "0" (Note 56)	
		typ.	max	typ.	max.
3.6V	1μF±30%	120ms	210ms	140ms	260ms
5.5V		160ms	270ms	170ms	300ms
3.6V	2.2μF±30%	260ms	460ms	310ms	560ms
5.5V		340ms	590ms	370ms	600ms

Note 55. Rising time of HP-Amp (0.8 x LVDD/2)
Note 56. Time until the common voltage settles to VSS4

Table 49. Relationship between capacitor value of MUTET pin and MUTE ON/OFF time (HPG bit = "0")

When PMHPL and PMHPR bits are "0", the Headphone-Amp is powered-down, and the outputs (HPL and HPR pins) become to "L" (VSS4).

PMHPL/R bits	HPMTN bit	Mode	HPL pin	HPR pin	
0	x	Power-down	"L"(VSS4)	"L"(VSS4)	(default)
1	0	Fall down to common voltage	"L"(VSS4)	"L"(VSS4)	
	1	Rise up to common voltage	Normal operation	Normal operation	

Table 50. Headphone-Amp Mode Setting (x: Don't care)

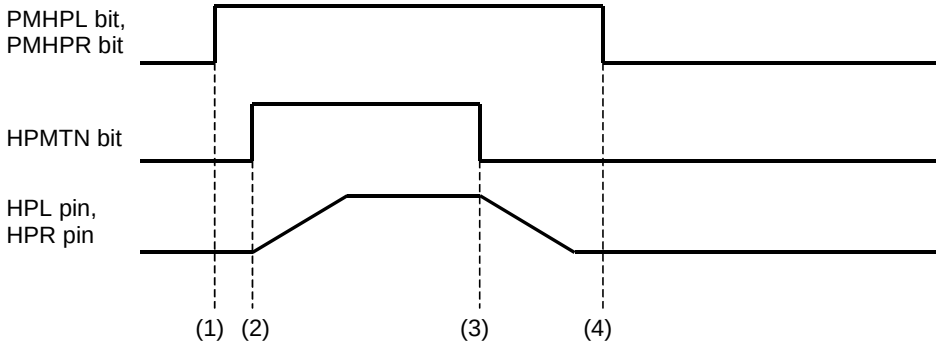


Figure 37. Power-up/Power-down Timing for Headphone-Amp

(1) Headphone-Amp power-up (PMHPL, PMHPR bit = "1"). The outputs are still VSS4.
(2) Headphone-Amp common voltage rises up (HPMTN bit = "1"). Common voltage of Headphone-Amp is rising.
(3) Headphone-Amp common voltage falls down (HPMTN bit = "0"). Common voltage of Headphone-Amp is falling.
(4) Headphone-Amp power-down (PMHPL, PMHPR bit = "0"). The outputs are VSS4. If the power supply is switched off or Headphone-Amp is powered-down before the common voltage settles to VSS4, some POP noise occurs.

When BOOST=OFF, the cut-off frequency (fc) of Headphone-Amp depends on the external resistor and capacitor. This fc can be shifted to lower frequency by using bass boost function. Table 51 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at AVDD = LVDD = 2.7, 3.0 and 3.3V. The output voltage of headphone is 0.6 x AVDD (Vpp)@HPG bit = "0", 0.91 x AVDD(Vpp)@HPG bit = "1".

When an external resistor R is smaller than 12Ω, put an oscillation prevention circuit (0.22μF±20% capacitor and 10Ω±20% resistor) because there is a possibility that Headphone-Amp oscillates.

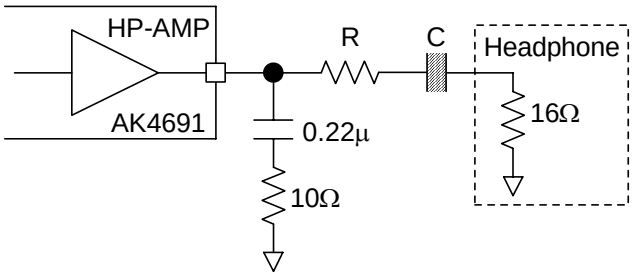


Figure 38. External Circuit Example of Headphone

HPG bit	R [Ω]	C [μF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MIN @fs=44.1kHz	Output Power [mW]@0dBFS		
					2.7V	3.0V	3.3V
0	6.8	100	70	28	10.1	12.5	15.1
		47	149	78			
	16	100	50	19	5.1	6.3	7.7
		47	106	47			
1	0	220	45	17	33	41	50
		100	100	43			
	100	22	62	25	0.9	1.1	1.3
		10	137	69			

Table 51. External Circuit Example

■ Speaker Output

When DACS bit is set to "1", the DAC output signal is input to the Speaker-amp as [(L+R)/2]. The Speaker-amp is mono and BTL output. The gain is set by SPKG1-0 bits. Output level depends on AVDD voltage and SPKG1-0 bits.

SPKG1-0 bits	Gain		
	ALC bit = "0"	ALC bit = "1"	
00	+4.43dB	+6.43dB	(default)
01	+6.43dB	+8.43dB	
10	+10.65dB	+12.65dB	
11	+12.65dB	+14.65dB	

Table 52. SPK-Amp Gain

AVDD	SVDD	SPKG1-0 bits	SPK-Amp Output (DAC Input = 0dBFS)	
			ALC bit = "0"	ALC bit = "1" (LMTH1-0 bits = "00";-2.5dBFS)
3.0V	3.0V	00	3.0Vpp	2.83Vpp
		01	3.77Vpp	3.56Vpp
		10	4.0Vpp (Note 57)	4.0Vpp (Note 57)
		11	4.0Vpp (Note 57)	4.0Vpp (Note 57)
	3.3V	00	3.0Vpp	2.83Vpp
		01	3.77Vpp	3.56Vpp
		10	4.6Vpp (Note 57)	4.6Vpp (Note 57)
		11	4.6Vpp (Note 57)	4.6Vpp (Note 57)

Note 57. The output level is calculated on the assumption that output signal is not clipped. In actual case, output signal may be clipped when DAC outputs 0dBFS signal. DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is 4.0Vpp (@ SVDD = 3.0V), 4.6Vpp (@ SVDD = 3.3V) or less and output signal is not clipped.

Table 53. SPK-Amp Output Level

<ALC Operation Example of Speaker Playback>

Register Name	Comment	fs=48kHz	
		Data	Operation
LMTH1-0	Limiter detection Level	00	–2.5dBFS
ZELMN	Limiter zero crossing detection	0	Enable
ZTM1-0	Zero crossing timeout period	10	10.7ms
WTM2-0	Recovery waiting period *WTM2-0 bits should be the same or larger data to ZTM1-0 bits	011	21.3ms
REF7-0	Maximum gain at recovery operation	C1H	+18dB
IVL7-0, IVR7-0	Gain of IVOL	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step
ALC	ALC enable	1	Enable

Table 54. ALC Operation Example of Speaker Playback

<Speaker-Amp Control Sequence>

Speaker-Amp is powered-up/down by PMSPK bit. When PMSPK bit is "0", both SPP and SPN pin are in Hi-Z state. When PMSPK bit is "1" and SPPSN bit is "0", the Speaker-Amp enters power-save mode. In this mode, the SPP pin is placed in Hi-Z state and the SPN pin outputs SVDD/2 voltage. Power-save mode can reduce pop noise at power-up and power-down.

PMSPK bit	SPPSN bit	Mode	SPP pin	SPN pin	
0	x	Power-down	Hi-Z	Hi-Z	(default)
1	0	Power-save	Hi-Z	SVDD/2	
	1	Normal Operation	Normal Operation	Normal Operation	

Table 55. Speaker-Amp Mode Setting (x: Don't care)

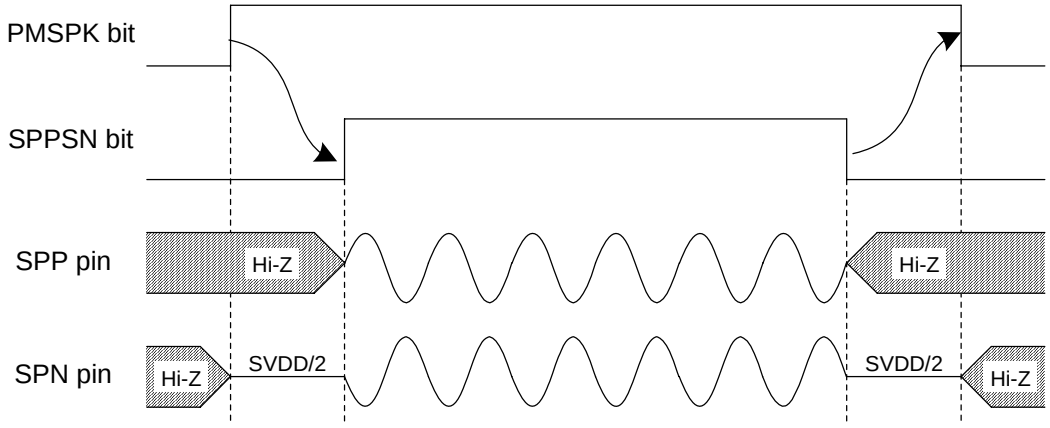


Figure 39. Power-up/Power-down Timing for Speaker-Amp

■ MUTE Function

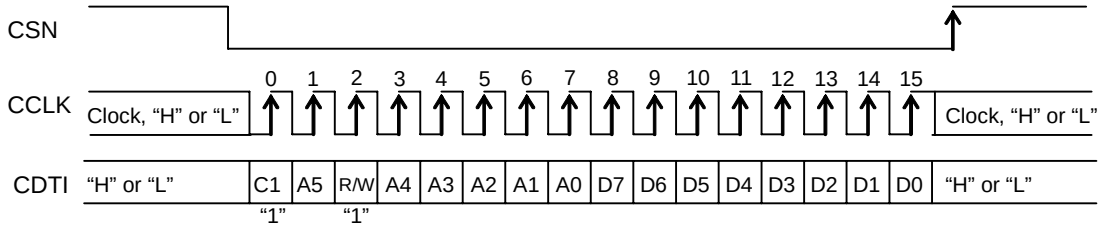
When the MUTE pin is "H", the output signals of LINEOUT, Headphone-Amp, and Speaker-Amp are muted, and become VCOM or LVCM voltage. LINEOUT and Speaker-Amp become Power-save mode, HP-Amp is in mute state. And switches of DACL, DACS, DACH, BEEPL, BEEPS, BEEPH, MICL1, MICR1, and MICL2 become "OFF" at the same time.

■ Serial Control Interface

(1) 3-wire Serial Control Mode (I2CN pin = “H”)

(1)-1. Specific address WRITE Mode

Internal registers may be written by using the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 1-bit Chip address (Fixed to “1”), Read/Write (Fixed to “1”), Register address (MSB first, 6bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge (“↑”) of CCLK. Writing data becomes effective between the 16th CCLK rising edge (“↑”) and CSN rising edge (“↑”) after CSN falling edge(“↓”). CSN should be set to “H” every one command. Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by the PDN pin = “L”.



C1: Chip Address; Fixed to “1”
R/W: READ/WRITE (“1”: WRITE, “0”: READ); Fixed to “1”
A5-A0: Register Address
D7-D0: Control data

Figure 40. Serial Control I/F Timing 1

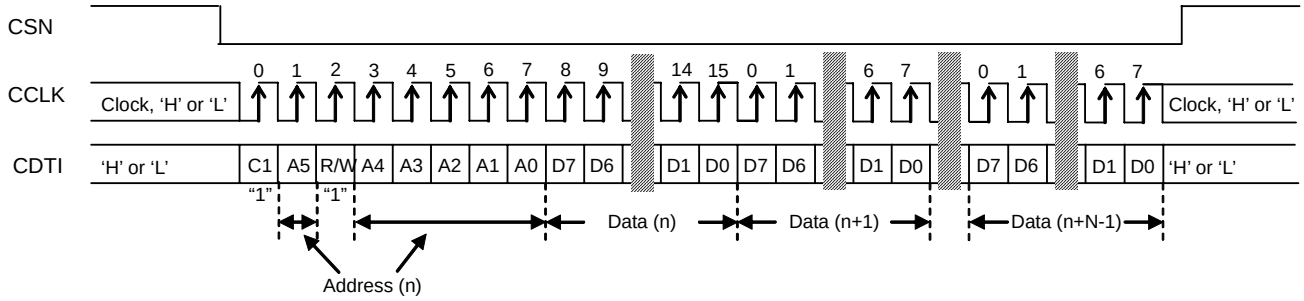
(1)-2. Continuous Data WRITE Mode

In this mode, data can be written continuously and address counter is incremented automatically.

Internal registers may be written by the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 1-bit Chip address (Fixed to "1"), Read/Write (Fixed to "1"), Register address (MSB first, 6bits) and Control data (MSB first, 8bits x N). Each bit is clocked in on the rising edge ("↑") of CCLK. Writing data becomes effective between the 16th CCLK rising edge ("↑") and falling edge ("↓"). When the µP continues sending CDTI and CCLK in CSN = "L", address counter is incremented automatically, and writing data becomes effective between the 8th CCLK rising edge ("↑") and falling edge ("↓"). For the last address (33H), writing data becomes effective between the 8th CCLK rising edge ("↑") and CSN rising edge ("↑").

When data is written to an arbitrary address before the last address, WRITE operation can be finished by setting CSN = "H".

Note 58. When CSN is set to "H" while data is written, the data is ignored.
Note 59. After data in the last address (33H) becomes effective, CSN should be set to "H". If the uP continues sending CCLK and CDTI in CSN = "L", data is rewritten in address 33H.



C1: Chip Address (C1= "1"); Fixed to "1"
R/W: READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A5-A0: Register Address
D7-D0: Control data

Figure 41. Control Data Timing 2

(2) I²C-bus Control Mode (I2CN pin = "L")

The AK4691 supports the fast-mode I²C-bus (max: 400kHz). Pull-up resistors at the SCL and SDA pins should be connected to (TVDD2 + 0.3)V or less voltage.

(2)-1. WRITE Operations

Figure 42 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 48). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as "001001". The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets these device address bits (Figure 43). If the slave address matches that of the AK4691, the AK4691 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 49). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4691. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 44). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 45). The AK4691 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 48).

The AK4691 can perform more than one byte write operation per sequence. After receiving the third byte the AK4691 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 50) except for the START and STOP conditions.

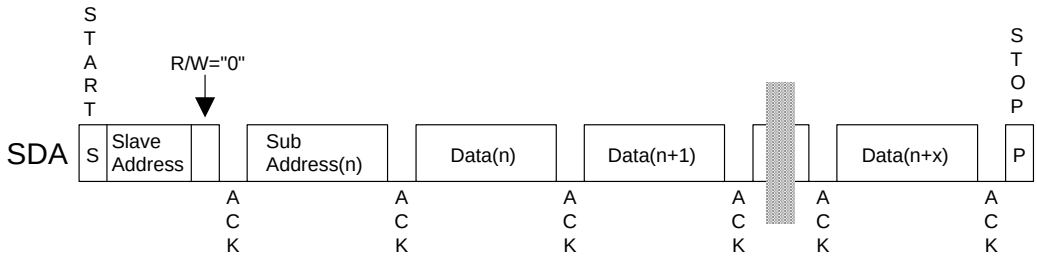


Figure 42. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	1	CAD0	R/W

(The CAD0 should match with CAD0 pin)

Figure 43. The First Byte

0	0	A5	A4	A3	A2	A1	A0

Figure 44. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 45. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4691. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after receiving the first data word. After receiving each data packet the internal 5-bit address counter is incremented, and the next data is automatically taken into the next address. If the address exceeds 33H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4691 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4691 contains an internal address counter. The "current address read" operation reads the data appointed by the counter. The counter is incremented by one from the address number of the last word accessed. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receiving the slave address with R/W bit "1", the AK4691 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but instead generates a stop condition, the AK4691 ceases transmission.

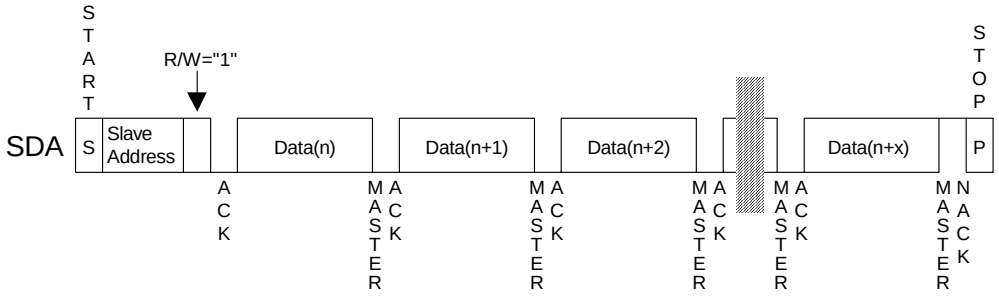


Figure 46. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4691 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but instead generates a stop condition, the AK4691 ceases transmission.

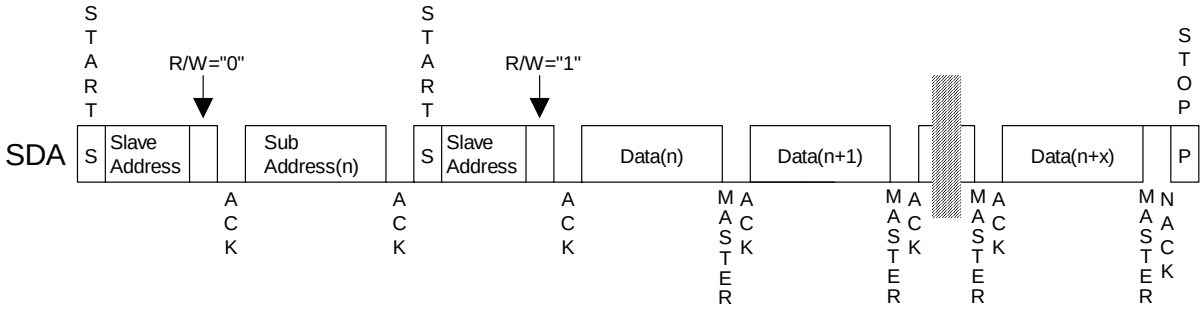


Figure 47. RANDOM ADDRESS READ

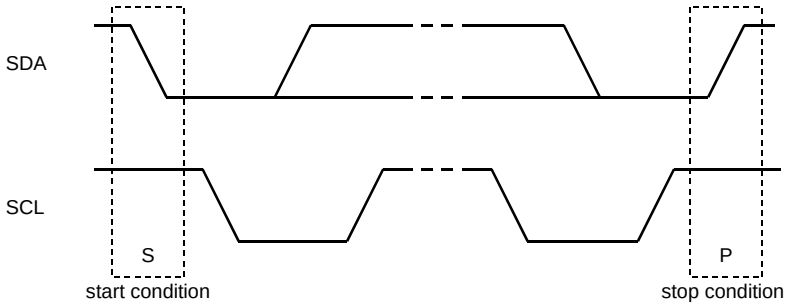


Figure 48. START and STOP Conditions

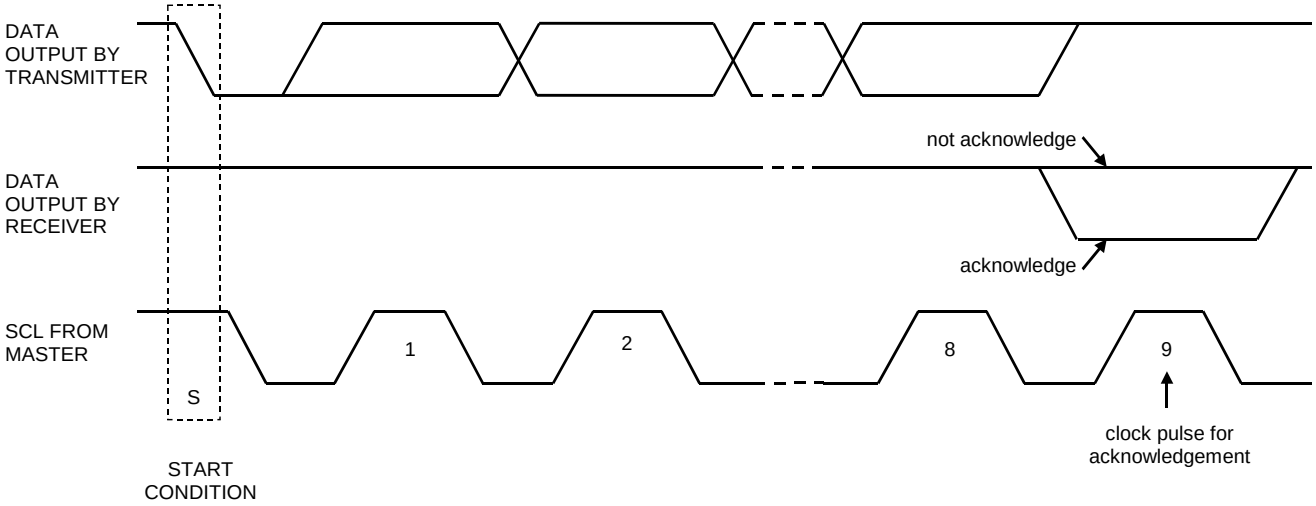


Figure 49. Acknowledge on the I^2C-Bus

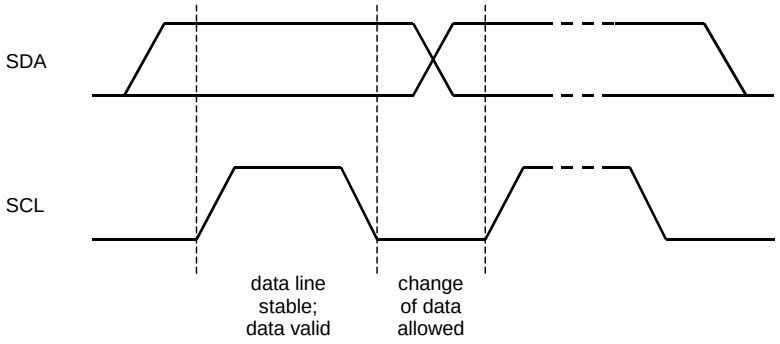


Figure 50. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMMP	PMMICR2	PMMICL2	PMMICR1	PMMICL1	PMADC2	PMADC1	PMVCM
01H	Power Management 2	0	HPMTN	PMHPR	PMHPL	PMSPK	PMLO	PMDAC	PMBP
02H	Mode Control 1	0	0	BCKO	M/S	PS1	PS0	MCKO	PMPLL
03H	Mode Control 2	PLL3	PLL2	PLL1	PLL0	FS3	FS2	FS1	FS0
04H	Mode Control 3	ADM1	ADM0	0	INITDA	LMODE	HPFN	DIF1	DIF0
05H	Pre-Amp Gain Select	0	0	PRG22	PRG21	PRG20	PRG12	PRG11	PRG10
06H	Signal Select 1	0	FB	AIN	PRE	PRSR2	PRSL2	PRSR1	PRSL1
07H	Signal Select 2	SPPSN	BEEPS	DACS	BEEPL	DACL	HPM	BEEPH	DACH
08H	HP/SPK Gain Select	0	0	MICL2	MICR1	MICL1	HPG	SPKG1	SPKG0
09H	Mode Control 4	LVOL2	LVOL1	LVOL0	LOPS	0	0	DVOLC	IVOLC
0AH	Timer Select	FDTM1	FDTM0	0	ZTM1	ZTM0	WTM2	WTM1	WTM0
0BH	ALC Mode Control 1	0	ZELMN	FDATT1	FDATT0	RGAIN1	RGAIN0	LMAT1	LMAT0
0CH	ALC Mode Control 2	0	0	LFST	RFST1	RFST0	GSEL	LMTH1	LMTH0
0DH	ALC Mode Control 3	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
0EH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
0FH	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
10H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
11H	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
12H	ALC Mode Control 4	0	0	0	0	0	ALC	FDOUT	FDIN
13H	Mode Control 5	LOOP1	LOOP0	SMUTE	DVTM	BST1	BST0	DEM1	DEM0
14H	Mode Control 6	0	0	MGR12	MGR11	MGR10	MGL12	MGL11	MGL10
15H	Mode Control 7	0	0	MGR22	MGR21	MGR20	MGL22	MGL21	MGL20
16H	Digital Filter Select 1	GN1A	GN0A	0	FIL1A	EQA	FIL3A	0	0
17H	FIL3A Co-efficient 0	F3A7A	F3A6A	F3A5A	F3A4A	F3A3A	F3A2A	F3A1A	F3A0A
18H	FIL3A Co-efficient 1	F3ASA	0	F3A13A	F3A12A	F3A11A	F3A10A	F3A9A	F3A8A
19H	FIL3A Co-efficient 2	F3B7A	F3B6A	F3B5A	F3B4A	F3B3A	F3B2A	F3B1A	F3B0A
1AH	FIL3A Co-efficient 3	0	0	F3B13A	F3B12A	F3B11A	F3B10A	F3B9A	F3B8A
1BH	EQA Co-efficient 0	EQA7A	EQA6A	EQA5A	EQA4A	EQA3A	EQA2A	EQA1A	EQA0A
1CH	EQA Co-efficient 1	EQA15A	EQA14A	EQA13A	EQA12A	EQA11A	EQA10A	EQA9A	EQA8A
1DH	EQA Co-efficient 2	EQB7A	EQB6A	EQB5A	EQB4A	EQB3A	EQB2A	EQB1A	EQB0A
1EH	EQA Co-efficient 3	0	0	EQB13A	EQB12A	EQB11A	EQB10A	EQB9A	EQB8A
1FH	EQA Co-efficient 4	EQC7A	EQC6A	EQC5A	EQC4A	EQC3A	EQC2A	EQC1A	EQC0A
20H	EQA Co-efficient 5	EQC15A	EQC14A	EQC13A	EQC12A	EQC11A	EQC10A	EQC9A	EQC8A
21H	FIL1A Co-efficient 0	F1A7A	F1A6A	F1A5A	F1A4A	F1A3A	F1A2A	F1A1A	F1A0A
22H	FIL1A Co-efficient 1	F1ASA	0	F1A13A	F1A12A	F1A11A	F1A10A	F1A9A	F1A8A
23H	FIL1A Co-efficient 2	F1B7A	F1B6A	F1B5A	F1B4A	F1B3A	F1B2A	F1B1A	F1B0A
24H	FIL1A Co-efficient 3	0	0	F1B13A	F1B12A	F1B11A	F1B10A	F1B9A	F1B8A
25H	Digital Filter Select 2	GN1B	GN0B	0	FIL1B	EQB	FIL3B	0	0
26H	FIL3B Co-efficient 0	F3A7B	F3A6B	F3A5B	F3A4B	F3A3B	F3A2B	F3A1B	F3A0B
27H	FIL3B Co-efficient 1	F3ASB	0	F3A13B	F3A12B	F3A11B	F3A10B	F3A9B	F3A8B
28H	FIL3B Co-efficient 2	F3B7B	F3B6B	F3B5B	F3B4B	F3B3B	F3B2B	F3B1B	F3B0B
29H	FIL3B Co-efficient 3	0	0	F3B13B	F3B12B	F3B11B	F3B10B	F3B9B	F3B8B
2AH	EQB Co-efficient 0	EQA7B	EQA6B	EQA5B	EQA4B	EQA3B	EQA2B	EQA1B	EQA0B
2BH	EQB Co-efficient 1	EQA15B	EQA14B	EQA13B	EQA12B	EQA11B	EQA10B	EQA9B	EQA8B
2CH	EQB Co-efficient 2	EQB7B	EQB6B	EQB5B	EQB4B	EQB3B	EQB2B	EQB1B	EQB0B
2DH	EQB Co-efficient 3	0	0	EQB13B	EQB12B	EQB11B	EQB10B	EQB9B	EQB8B
2EH	EQB Co-efficient 4	EQC7B	EQC6B	EQC5B	EQC4B	EQC3B	EQC2B	EQC1B	EQC0B
2FH	EQB Co-efficient 5	EQC15B	EQC14B	EQC13B	EQC12B	EQC11B	EQC10B	EQC9B	EQC8B
30H	FIL1B Co-efficient 0	F1A7B	F1A6B	F1A5B	F1A4B	F1A3B	F1A2B	F1A1B	F1A0B
31H	FIL1B Co-efficient 1	F1ASB	0	F1A13B	F1A12B	F1A11B	F1A10B	F1A9B	F1A8B
32H	FIL1B Co-efficient 2	F1B7B	F1B6B	F1B5B	F1B4B	F1B3B	F1B2B	F1B1B	F1B0B
33H	FIL1B Co-efficient 3	0	0	F1B13B	F1B12B	F1B11B	F1B10B	F1B9B	F1B8B

Note 60. PDN pin = "L" resets the registers to their default values.
Note 61. Write "0" data to the bits named "0".

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMMP	PMMICR2	PMMICL2	PMMICR1	PMMICL1	PMADC2	PMADC1	PMVCM
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCM: VCOM and LVCM Power Management
0: Power-down (default)
1: Power-up
When any blocks are powered-up, the PMVCM bit must be set to "1". PMVCM bit can be set to "0" only when all power management bits of 00H and 01H, PMPLL and MCKO bits are "0".

PMADC1: ADC1 Power Management
0: Power-down (default)
1: Power-up

PMADC2: ADC2 Power Management
0: Power-down (default)
1: Power-up
When the PMADC1 or PMADC2 bit is changed from "0" to "1", the initialization cycle (1059/fs=22.1ms @48kHz) starts. After initializing, digital data of the ADC is output.

PMMICL1: Lch Pre-Amp #1 Power Management
0: Power-down (default)
1: Power-up

PMMICR1: Rch Pre-Amp #1 Power Management
0: Power-down (default)
1: Power-up

PMMICL2: Lch Pre-Amp #2 Power Management
0: Power-down (default)
1: Power-up

PMMICR2: Rch Pre-Amp #2 Power Management
0: Power-down (default)
1: Power-up

PMMP: MPWR pin Power Management
0: Power-down. Pull-down to VSS1 with 5.3kΩ (typ.) (default)
1: Power-up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	HPMTN	PMHPR	PMHPL	PMSPK	PMLO	PMDAC	PMBP
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMBP: BEEP Input Power Management
0: Power-down (default)
1: Power-up
Both PMDAC and PMBP bits should be set to "1" when DAC is powered-up for playback. After that, BEEPL, BEEPH, BEEPS, MICL1, MICR1, or MICL2 bit is used to control each path when BEEP input is used.

PMDAC: DAC Power Management
0: Power-down (default)
1: Power-up

PMLO: Stereo Lineout Power Management
0: Power-down (default)
1: Power-up

PMSPK: Speaker-Amp Power Management
0: Power-down (default)
1: Power-up

PMHPL: Headphone-Amp Lch Power Management
0: Power-down (default)
1: Power-up

PMHPR: Headphone-Amp Rch Power Management
0: Power-down (default)
1: Power-up

HPMTN: Headphone-Amp Mute Control
0: Mute (default)
1: Normal operation

Each block can be powered-down respectively by writing "0" to each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When all power management bits are "0" in the 00H and 01H addresses, PMPLL bit and MCKO bit is "0", all blocks are powered-down. The register values remain unchanged.

When neither ADC nor DAC are used, external clocks may not be present. When ADC or DAC is used, external clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Mode Control 1	0	0	BCKO	M/S	PS1	PS0	MCKO	PMPLL
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power-Down (default)
1: PLL Mode and Power-up

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (default)
1: Enable: Output frequency is selected by PS1-0 bits.

PS1-0: MCKO Output Frequency Select (Table 9)
Default: "00" (256fs)

M/S: Master / Slave Mode Select
0: Slave Mode (default)
1: Master Mode

BCKO: BICK Output Frequency Select at Master Mode (Table 10)
Default: "0" (32fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 2	PLL3	PLL2	PLL1	PLL0	FS3	FS2	FS1	FS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency Select (Table 5, Table 6.) and MCKI Frequency Select (Table 11)
FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

PLL3-0: PLL Reference Clock Select (Table 4)
Default: "0000"(LRCK pin)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Mode Control 3	ADM1	ADM0	0	INITDA	LMODE	HPFN	DIF1	DIF0
R/W		R/W	R/W	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

DIF1-0: Audio Interface Format (Table 13)
Default: "10" (Left justified)

HPFN: HPF Control on DAC
0: Enable (default)
1: Disable

LMODE: Select power-save mode of stereo line output (Table 45, Table 47)

INITDA: DAC Initialization Cycle Enable
0: Enable (Initialization Cycle= 1059/fs) (default)
1: Disable

ADM1-0: ADC Mono Mode (Table 21)
Default: "00" (Stereo Output)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Pre-Amp Gain Select	0	0	PRG22	PRG21	PRG20	PRG12	PRG11	PRG10
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	1	1

PRG12-10: Pre-Amp #1 Gain Setting (Table 15)
Default: "011" (+24dB)

PRG22-20: Pre-Amp #2 Gain Setting (Table 15)
Default: "011" (+24dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Signal Select 1	0	FB	AIN	PRE	PRSR2	PRSL2	PRSR1	PRSL1
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	0

PRSL1: Select input signal of Lch Pre-Amp #1
0: INTL1 pin (default)
1: EXTL1 pin

PRSR1: Select input signal of Rch Pre-Amp #1
0: INTR1 pin (default)
1: EXTR1 pin

PRSL2: Select input signal of Lch Pre-Amp #2
0: INTL2 pin (default)
1: EXTL2 pin

PRSR2: Select input signal of Rch Pre-Amp #2
0: INTR2 pin (default)
1: EXTR2 pin

PRE: Enable input signal from Pre-Amp 1 to ADC1
0: OFF
1: ON (default)

AIN: Enable input signal from LIN/RIN pin to ADC1
0: OFF (default)
1: ON

FB: Select MIX-Amp feedback resistor
0: 60kΩ (typ) (default)
1: 100kΩ (typ)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Signal Select 2	SPPSN	BEEPS	DACS	BEEPL	DACL	HPM	BEEPH	DACH
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACH: Switch Control from DAC to Headphone-Amp
0: OFF (default)
1: ON

BEEPH: Switch Control from the BEEP pin to Headphone-Amp
0: OFF (default)
1: ON

HPM: Headphone-Amp Mono Output Select
0: Stereo (default)
1: Mono
When the HPM bit = "1", (L+R)/2 signals are output to Lch and Rch of the Headphone-Amp. Both PMHPL and PMHPR bits should be "1" when HPM bit is "1".

DACL: Switch Control from DAC to Stereo Line Output
0: OFF (default)
1: ON
When PMLO bit is "1", DACL bit is enabled.

BEEPL: Switch Control from the BEEP pin to Stereo Line Output
0: OFF (default)
1: ON
When PMLO bit is "1", BEEPL bit is enabled.

DACS: Switch Control from DAC to Speaker-Amp
0: OFF (default)
1: ON
When DACS bit is "1", DAC output signal is input to Speaker-Amp.

BEEPS: Switch Control from BEEP pin to Speaker-Amp
0: OFF (default)
1: ON
When BEEPS bit is "1", mono signal is input to Speaker-Amp.

SPPSN: Speaker-Amp Power-Save Mode
0: Power-Save Mode (default)
1: Normal Operation
When SPPSN bit is "0", Speaker-Amp is in power-save mode. In this mode, the SPP pin changes to Hi-Z and the SPN pin outputs SVDD/2 voltage. When PMSPK bit = "1", SPPSN bit is enabled. After the PDN pin is set to "H", Speaker-Amp is in power-down mode since PMSPK bit is "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	HP/SPK Gain	0	0	MICL2	MICR1	MICL1	HPG	SPKG1	SPKG0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SPKG1-0: Speaker-Amp Output Gain Select (Table 52)

HPG: Headphone-Amp Gain Select (Table 48)
0: 0dB (default)
1: +3.6dB

MICL1: Select path from Lch Pre-Amp #1 to LOUT pin.
0: OFF (default)
1: ON
When PMMICL1 = PMLO bits = "1", MICL1 bit is enabled.

MICR1: Select path from Rch Pre-Amp #1 to LOUT pin
0: OFF (default)
1: ON
When PMMICR1 = PMLO bits = "1", MICR1 bit is enabled.

MICL2: Select path from Lch Pre-Amp #2 to LOUT pin
0: OFF (default)
1: ON
When PMMICL2 = PMLO bits = "1", MICL2 bit is enabled.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Mode Control 4	LVOL2	LVOL1	LVOL0	LOPS	0	0	DVOLC	IVOLC
R/W		R/W	R/W	R/W	R/W	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	1	1

IVOLC: Input Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

DVOLC: Output Digital Volume Control Mode Select
0: Independent
1: Dependent (default)
When DVOLC bit = "1", DVL7-0 bits control both Lch and Rch volume level, while register values of DVL7-0 bits are not written to DVR7-0 bits. When DVOLC bit = "0", DVL7-0 bits control Lch level and DVR7-0 bits control Rch level, respectively.

LOPS: Stereo Line Output Power-Save Mode
0: Normal Operation (default)
1: Power-Save Mode

LVOL2-0: Stereo Line Output Gain Select (Table 44)
Default: "000" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Timer Select	FDTM1	FDTM0	0	ZTM1	ZTM0	WTM2	WTM1	WTM0
R/W		R/W	R/W	RD	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	1	0	0

WTM2-0: ALC Recovery Waiting Period (Table 29)
Default: "100" (2048/fs)

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (Table 28.)
Default: "00" (128/fs)

FDTM1-0: FADEIN/OUT Cycle Setting (Table 34)
Default: "01" (2048/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ALC Mode Control 1	0	ZELMN	FDATT1	FDATT0	RGAIN1	RGAIN0	LMAT1	LMAT0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMAT1-0: ALC Limiter ATT Step (Table 27)
Default: "00"

RGAIN1-0: ALC Recovery GAIN Step (Table 30)
Default: "00"

FDATT1-0: FADEIN/OUT ATT Step Setting (Table 35)
Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
0: Enable (default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	ALC Mode Control 2	0	0	LFST	RFST1	RFST0	GSEL	LMTH1	LMTH0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 26)
Default: "00"

GSEL: Select IVOL Gain
0: MIC (default)
1: LINE

RFST1-0: ALC First limiter/recovery Speed (Table 32)
Default: "00" (4 times)

LFST: Setting of Limiter operation when input signal exceeds full-scale level
0: IVL/R values are changed at zero-crossing detection or zero-crossing timeout. (default)
1: IVL/R values are immediately (period: 1/fs) attenuated by 1step when ALC output signal exceeds full-scale level.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	ALC Mode Control 3	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 31)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Lch Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
10H	Rch Input Volume Control	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	0	0	0	0	1

IVL7-0, IVR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 36)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Lch Digital Volume Control	DVL7	DVL6	DVL5	DVL4	DVL3	DVL2	DVL1	DVL0
11H	Rch Digital Volume Control	DVR7	DVR6	DVR5	DVR4	DVR3	DVR2	DVR1	DVR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

DVL7-0, DVR7-0: Output Digital Volume (Table 39)
Default: "18H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	ALC Mode Control 4	0	0	0	0	0	ALC	FDOUT	FDIN
R/W		RD	RD	RD	RD	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ALC: ALC Enable
0: ALC Disable (default)
1: ALC Enable

FDOUT: FADEOUT Enable
0: Disable (default)
1: Enable

FDIN: FADEIN Enable
0: Disable (default)
1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Mode Control 5	LOOP1	LOOP0	SMUTE	DVTM	BST1	BST0	DEM1	DEM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis Frequency Select (Table 37)
Default: "01" (OFF)

BST1-0: Bass Boost Function Select (Table 38)
Default: "00" (OFF)

DVTM: Digital Volume Transition Time Setting (Table 40)
0: 1061/fs (default)
1: 256/fs
This is the transition time between DVL/R7-0 bits = 00H and FFH.

SMUTE: Soft Mute Control
0: Normal Operation (default)
1: DAC outputs soft-muted

LOOP1-0: Digital Internal Loopback (Table 23, Table 25)
00: SDTI → DAC (default)
01: SDTO1 → DAC
10: SDTO2 → DAC
11: SDTO1 → DAC
When LOOP1-0 bits = "10" (SDTO2 → DAC), TDM mode (DIF1-0 bits = "00") is not supported.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	Mode Control 6	0	0	MGR12	MGR11	MGR10	MGL12	MGL11	MGL10
15H	Mode Control 6	0	0	MGR22	MGR21	MGR20	MGL22	MGL21	MGL20
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	1	0

MGL12-10: MIC sensitivity compensation for INTL1/EXTL1 input
MGR12-10: MIC sensitivity compensation for INTR1/EXTR1 input
MGL22-20: MIC sensitivity compensation for INTL2/EXTL2 input
MGR22-20: MIC sensitivity compensation for INTR2/EXTR2 input
Default: "010" (0dB) (Table 17, Table 18)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Digital Filter Select 1	GN1A	GN0A	0	FIL1A	EQA	FIL3A	0	0
R/W		R/W	R/W	RD	R/W	R/W	R/W	RD	RD
Default		0	0	0	0	0	0	0	0

FIL3A: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL3A bit is "1", the settings of F3A13A-0A and F3B13A-0A bits are enabled. When FIL3A bit is "0", FIL3A block is OFF (MUTE).

EQA: EQA (Gain Compensation Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQA bit is "1", the settings of EQA15A-0A, EQB13A-0A and EQC15A-0A bits are enabled. When EQA bit is "0", EQA block is through (0dB).

FIL1A: FIL1A (Wind-noise Reduction Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL1A bit is "1", the settings of F1A13A-0A and F1B13A-0A bits are enabled. When FIL1A bit is "0", FIL1A block is through (0dB).

GN1A-0A: Gain Select at GAIN block in ADC1 (Table 24)
Default: "00" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
17H	FIL3A Co-efficient 0	F3A7A	F3A6A	F3A5A	F3A4A	F3A3A	F3A2A	F3A1A	F3A0A
18H	FIL3A Co-efficient 1	F3ASA	0	F3A13A	F3A12A	F3A11A	F3A10A	F3A9A	F3A8A
19H	FIL3A Co-efficient 2	F3B7A	F3B6A	F3B5A	F3B4A	F3B3A	F3B2A	F3B1A	F3B0A
1AH	FIL3A Co-efficient 3	0	0	F3B13A	F3B12A	F3B11A	F3B10A	F3B9A	F3B8A
1BH	EQA Co-efficient 0	EQA7A	EQA6A	EQA5A	EQA4A	EQA3A	EQA2A	EQA1A	EQA0A
1CH	EQA Co-efficient 1	EQA15A	EQA14A	EQA13A	EQA12A	EQA11A	EQA10A	EQA9A	EQA8A
1DH	EQA Co-efficient 2	EQB7A	EQB6A	EQB5A	EQB4A	EQB3A	EQB2A	EQB1A	EQB0A
1EH	EQA Co-efficient 3	0	0	EQB13A	EQB12A	EQB11A	EQB10A	EQB9A	EQB8A
1FH	EQA Co-efficient 4	EQC7A	EQC6A	EQC5A	EQC4A	EQC3A	EQC2A	EQC1A	EQC0A
20H	EQA Co-efficient 5	EQC15A	EQC14A	EQC13A	EQC12A	EQC11A	EQC10A	EQC9A	EQC8A
21H	FIL1A Co-efficient 0	F1A7A	F1A6A	F1A5A	F1A4A	F1A3A	F1A2A	F1A1A	F1A0A
22H	FIL1A Co-efficient 1	F1ASA	0	F1A13A	F1A12A	F1A11A	F1A10A	F1A9A	F1A8A
23H	FIL1A Co-efficient 2	F1B7A	F1B6A	F1B5A	F1B4A	F1B3A	F1B2A	F1B1A	F1B0A
24H	FIL1A Co-efficient 3	0	0	F1B13A	F1B12A	F1B11A	F1B10A	F1B9A	F1B8A
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F3A13A-0A, F3B13A-0A: FIL3A (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: “0000H”

F3ASA: FIL3A (Stereo Separation Emphasis Filter) Select
0: HPF (default)
1: LPF

EQA15A-0A, EQB13A-0A, EQC15A-C0A: EQA (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)
Default: “0000H”

F1A13A-0A, F1B13A-B0A: FIL1A (Wind-noise Reduction Filter) Coefficient (14bit x 2)
Default: “0000H”

F1ASA: FIL1A (Wind-noise Reduction Filter) Select
0: HPF (default)
1: LPF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
25H	Digital Filter Select 2	GN1B	GN0B	0	FIL1B	EQB	FIL3B	0	0
R/W		R/W	R/W	RD	R/W	R/W	R/W	RD	RD
Default		0	0	0	0	0	0	0	0

FIL3B: FIL3B (Stereo Separation Emphasis Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL3B bit is "1", the settings of F3A13B-0B and F3B13B-0B bits are enabled. When FIL3B bit is "0", FIL3B block is OFF (MUTE).

EQB: EQB (Gain Compensation Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When EQB bit is "1", the settings of EQA15B-0B, EQB13B-0B and EQC15B-0B bits are enabled. When EQB bit is "0", EQB block is through (0dB).

FIL1B: FIL1B (Wind-noise Reduction Filter) Coefficient Setting Enable
0: Disable (default)
1: Enable
When FIL1B bit is "1", the settings of F1A13B-0B and F1B13B-0B bits are enabled. When FIL1B bit is "0", FIL1B block is through (0dB).

GN1B-0B: Gain Select at GAIN block in ADC2 (Table 24)
Default: "00" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
26H	FIL3B Co-efficient 0	F3A7B	F3A6B	F3A5B	F3A4B	F3A3B	F3A2B	F3A1B	F3A0B
27H	FIL3B Co-efficient 1	F3ASB	0	F3A13B	F3A12B	F3A11B	F3A10B	F3A9B	F3A8B
28H	FIL3B Co-efficient 2	F3B7B	F3B6B	F3B5B	F3B4B	F3B3B	F3B2B	F3B1B	F3B0B
29H	FIL3B Co-efficient 3	0	0	F3B13B	F3B12B	F3B11B	F3B10B	F3B9B	F3B8B
2AH	EQB Co-efficient 0	EQA7B	EQA6B	EQA5B	EQA4B	EQA3B	EQA2B	EQA1B	EQA0B
2BH	EQB Co-efficient 1	EQA15B	EQA14B	EQA13B	EQA12B	EQA11B	EQA10B	EQA9B	EQA8B
2CH	EQB Co-efficient 2	EQB7B	EQB6B	EQB5B	EQB4B	EQB3B	EQB2B	EQB1B	EQB0B
2DH	EQB Co-efficient 3	0	0	EQB13B	EQB12B	EQB11B	EQB10B	EQB9B	EQB8B
2EH	EQB Co-efficient 4	EQC7B	EQC6B	EQC5B	EQC4B	EQC3B	EQC2B	EQC1B	EQC0B
2FH	EQB Co-efficient 5	EQC15B	EQC14B	EQC13B	EQC12B	EQC11B	EQC10B	EQC9B	EQC8B
30H	FIL1B Co-efficient 0	F1A7B	F1A6B	F1A5B	F1A4B	F1A3B	F1A2B	F1A1B	F1A0B
31H	FIL1B Co-efficient 1	F1ASB	0	F1A13B	F1A12B	F1A11B	F1A10B	F1A9B	F1A8B
32H	FIL1B Co-efficient 2	F1B7B	F1B6B	F1B5B	F1B4B	F1B3B	F1B2B	F1B1B	F1B0B
33H	FIL1B Co-efficient 3	0	0	F1B13B	F1B12B	F1B11B	F1B10B	F1B9B	F1B8B
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

F3A13B-0B, F3B13B-0B: FIL3B (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)
Default: “0000H”

F3ASB: FIL3B (Stereo Separation Emphasis Filter) Select
0: HPF (default)
1: LPF

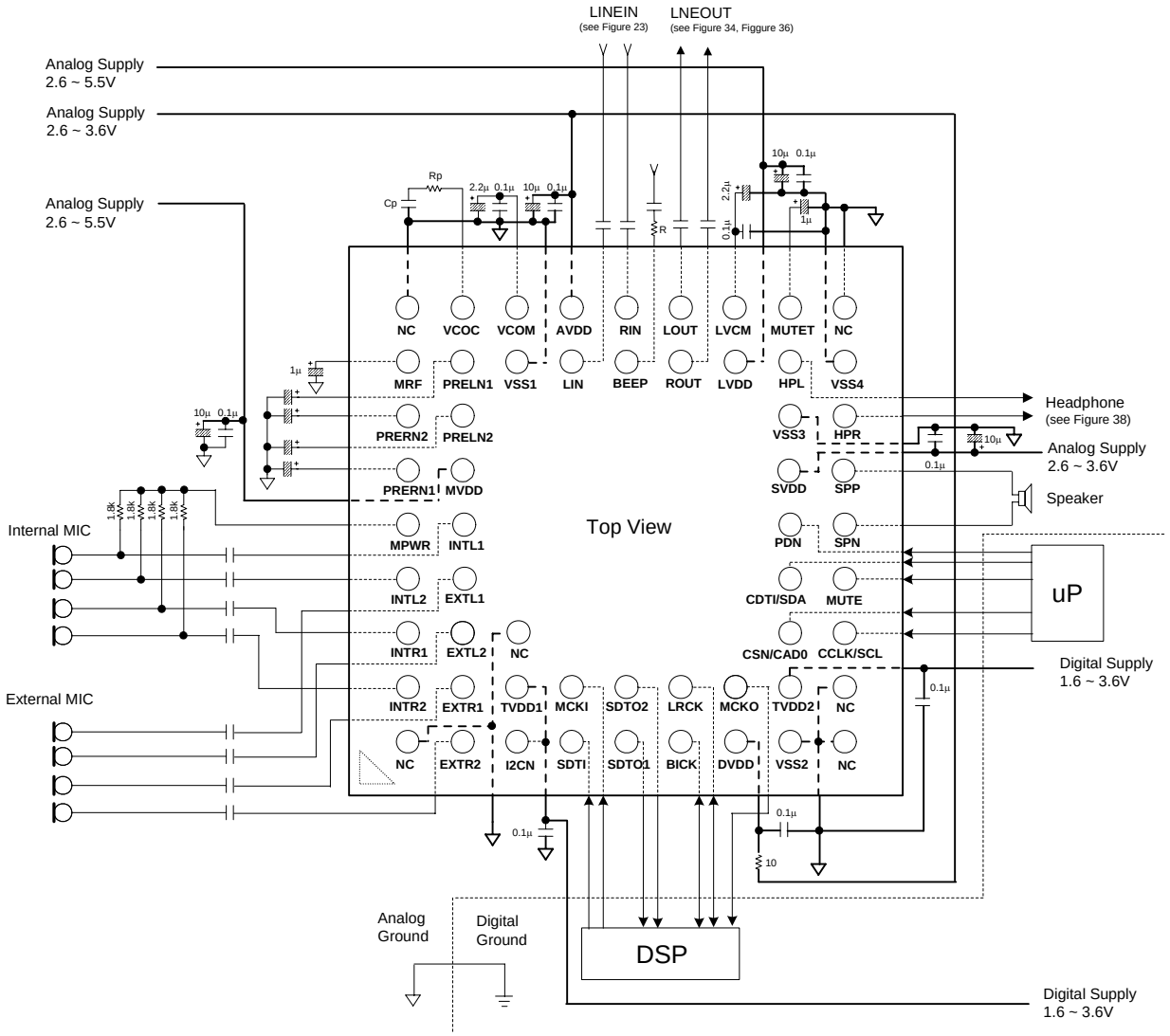
EQA15B-0B, EQB13B-0B, EQC15B-C0B: EQB (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)
Default: “0000H”

F1A13B-0B, F1B13B-B0B: FIL1B (Wind-noise Reduction Filter) Coefficient (14bit x 2)
Default: “0000H”

F1ASB: FIL1B (Wind-noise Reduction Filter) Select
0: HPF (default)
1: LPF

SYSTEM DESIGN

Figure 51 shows the system connection diagram for the AK4691. The evaluation board [AKD4691] demonstrates the optimum layout, power supply arrangements and measurement results.



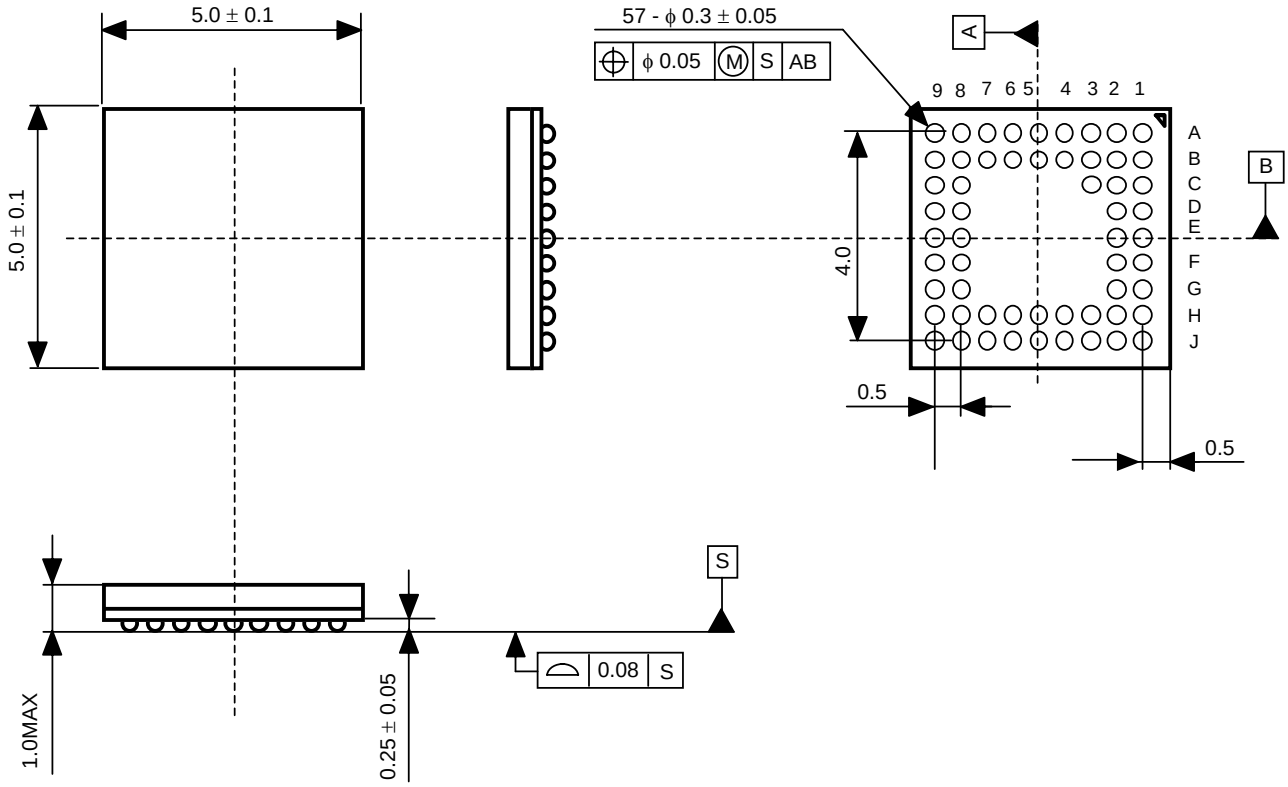
Notes:

- VSS1, VSS2, VSS3 and VSS4 of the AK4691 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK4691 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of the VCOC pin is not needed.
- When the AK4691 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of the VCOC pin is shown in Table 4.
- When the AK4691 is used in master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor should be connected to LRCK and BICK pins of the AK4691.

Figure 51. Typical Connection Diagram (I2CN pin = "H", 3-wire Mode)

PACKAGE

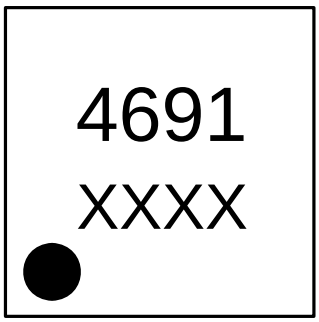
57pin BGA (Unit: mm)



■ Material & Lead finish

Package molding compound:	Epoxy
Interposer material:	BT resin
Solder ball material:	SnAgCu

MARKING



XXXX: Date code (4 digits)
Pin #1 indication

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
07/11/02	00	First Edition		