



## Low-Jitter Configurable HCSL Oscillator

### General Description

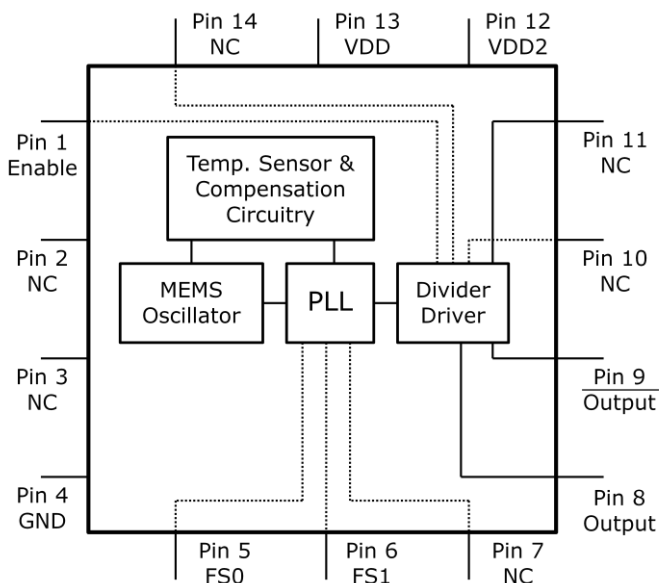
The DSC2040 series of high performance dual output oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. The two outputs are controlled by separate supply voltages to allow for high output isolation. The frequencies of the outputs can be identical or independently derived from a common PLL frequency source. The DSC2040 has provision for up to eight user-defined pre-programmed, pin-selectable output frequency combinations.

DSC2040 is packaged in a 14-pin 3.2x2.5 mm QFN package and available in temperature grades from Ext. Commercial to Industrial.

### Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability:  $\pm 10$ ,  $\pm 25$ ,  $\pm 50$  ppm**
- **Wide Temperature Range**
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Two Independent HCSL Outputs**
- **4 Pin-Selectable Output Frequencies**
- **Wide Freq. Range:**
  - HCSL Output: 2.3 to 460 MHz
- **Miniature Footprint of 3.2x2.5mm**
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**

### Block Diagram



### Applications

- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**

## Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	Leave unconnected or grounded
4	GND	Power	Ground
5	FS0	I	Least significant bit for frequency selection
6	FS1	I	Most significant bit for frequency selection
7	NC	NA	Leave unconnected or grounded
8	Output+	O	Positive HCSL Output
9	Output-	O	Negative HCSL Output
10	NC	NA	Leave unconnected or grounded
11	NC	NA	Leave unconnected or grounded
12	VDD2	Power	Power Supply
13	VDD	Power	Power Supply
14	NC	NA	Leave unconnected or grounded

## Operational Description

The DSC2040 is a HCSL oscillator consisting of a MEMS resonator and a support PLL IC. The HCSL output is generated through independent 8-bit programmable dividers from the output of the internal PLL.

The actual frequency output by the DSC2040 is controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to four

different frequencies. Two control pins (FS0 – FS1) select the output frequency. Discera supports customer defined versions of the DSC2040. Standard frequency options are described in the following sections.

When Enable (pin 1) is floated or connected to VDD, the DSC2040 is in operational mode. Driving Enable to ground will tri-state output driver (hi-impedance mode).

## Output Clock Frequencies

Table 1 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 1. Pre-programmed pin-selectable output frequency combinations

Ordering Info	Freq (MHz)	Freq Select Bits [FS1, FS0] – <b>Default is [11]</b>			
		00	01	10	<b>11</b>
D0001	$f_{OUT}$	125	156.25	200	<b>100</b>
D000X	$f_{OUT}$	Contact factory for additional configurations.			

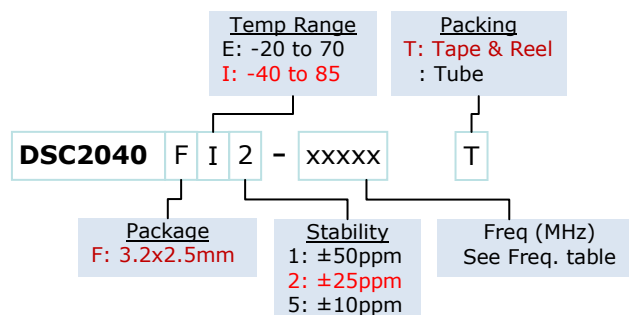
Frequency select bit are weakly tied high so if left unconnected the default setting will be [11] and the device will output the associated frequency highlighted in **Bold**.

## Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	$V_{DD}+0.3$	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Note: 1000+ years of data retention on internal memory

## Ordering Code



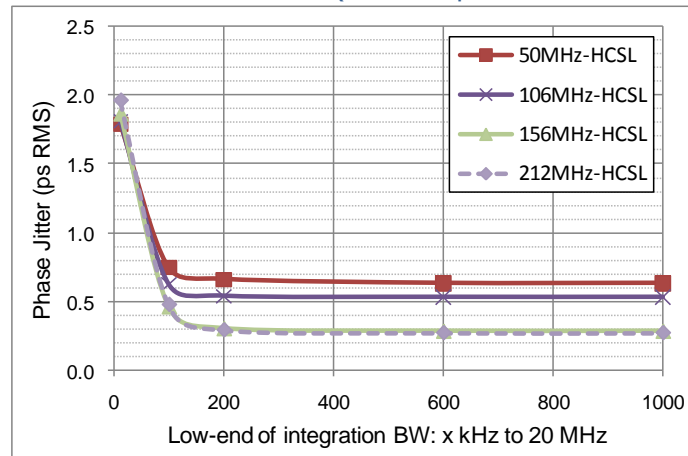
## Specifications (Unless specified otherwise: T=25° C)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage <sup>1</sup>	$V_{DD}$		2.25		3.6	V
Supply Current	$I_{DD}$	EN pin low – outputs are disabled		21	23	mA
Supply Current <sup>2</sup>	$I_{DD}$	EN pin high – outputs are enabled $R_L=50\ \Omega$ , $F_0=156.25\ \text{MHz}$		40	42	mA
Frequency Stability	$\Delta f$	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	$\Delta f$	1 year @25°C			±5	ppm
Startup Time <sup>3</sup>	$t_{SU}$	T=25°C			5	ms
Input Logic Levels						
Input logic high	$V_{IH}$		0.75x $V_{DD}$		-	V
Input logic low	$V_{IL}$		-		0.25x $V_{DD}$	
Output Disable Time <sup>4</sup>	$t_{DA}$				5	ns
Output Enable Time	$t_{EN}$				20	ns
Pull-Up Resistor <sup>2</sup>		Pull-up exists on all digital IO		40		k $\Omega$
<b>HCSL Outputs</b>						
Output Logic Levels						
Output logic high	$V_{OH}$	$R_L=50\ \Omega$	0.725		-	V
Output logic low	$V_{OL}$		-		0.1	
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time <sup>4</sup>						
Rise Time	$t_R$	20% to 80% $R_L=50\ \Omega$ , $C_L=2\ \text{pF}$	200		400	ps
Fall Time	$t_F$					
Frequency	$f_0$	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter <sup>5</sup>	$J_{PER}$	$F_0=156.25\ \text{MHz}$		2.8		ps <sub>RMS</sub>
Integrated Phase Noise	$J_{PH}$	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.37 1.7	2	ps <sub>RMS</sub>

### Notes:

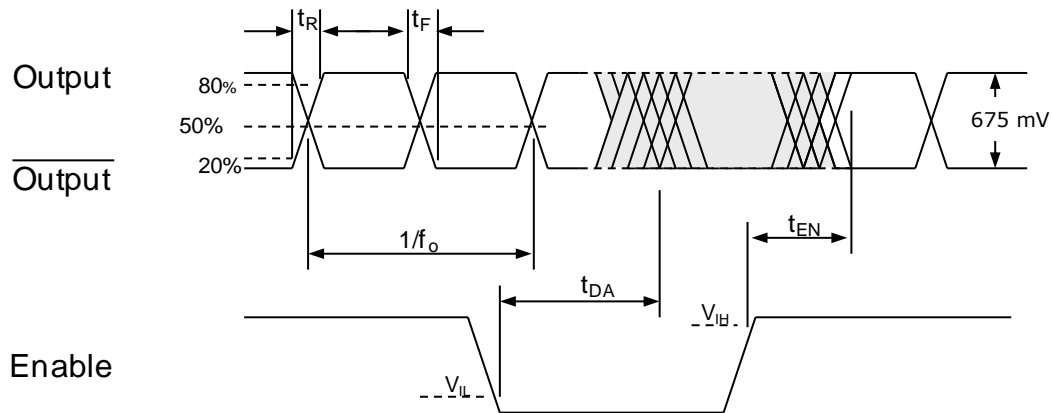
- Pin 4  $V_{DD}$  should be filtered with 0.01uF capacitor.
- Output is enabled if Enable pad is floated or not connected.
- $t_{SU}$  is time to 100PPM stable output frequency after  $V_{DD}$  is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Period Jitter includes crosstalk from adjacent output.

## Nominal Performance Parameters (Unless specified otherwise: $T=25^{\circ}\text{C}$ , $V_{DD}=3.3\text{V}$ )

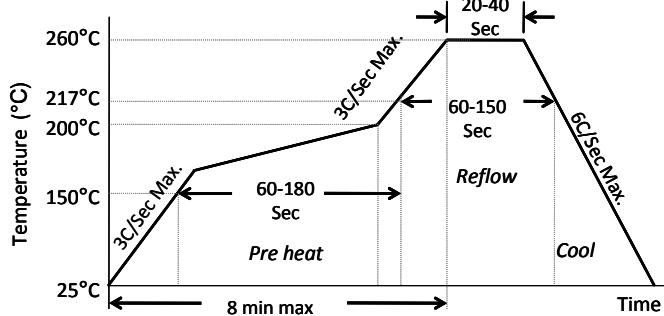


HCSL Phase jitter (integrated phase noise)

## Output Waveform: HCSL



## Solder Reflow Profile



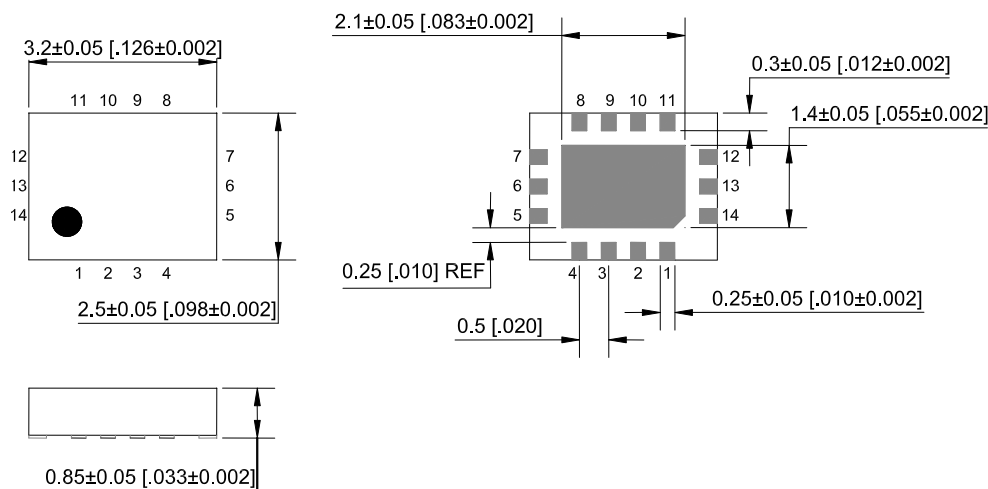
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

## Package Dimensions

### 3.2 x 2.5 mm 14 Lead Plastic Package

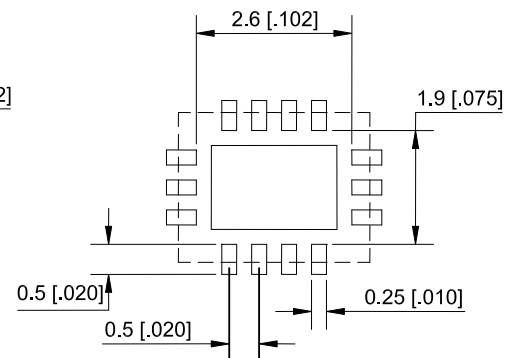
#### External Dimensions

units: mm[inch]



#### Recommended Solder Pad Layout

units: mm[inch]



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