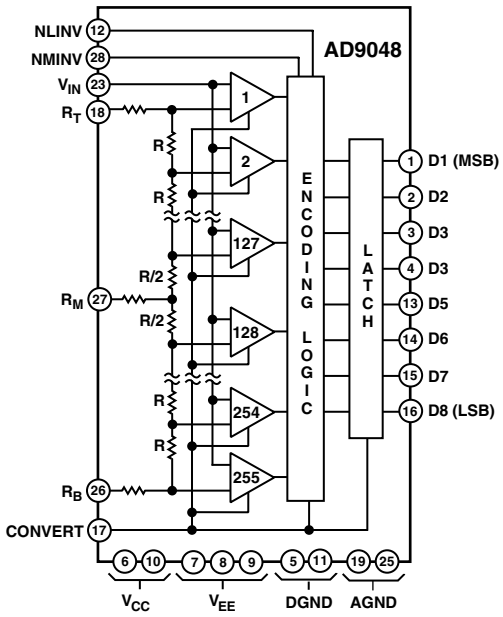
Monolithic 8-Bit Video A/D Converter

AD9048

FEATURES
35 MSPS Encode Rate
16 pF Input Capacitance
550 mW Power Dissipation
Industry-Standard Pinouts
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Professional Video Systems
Special Effects Generators
Electro-Optics
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9048 is an 8-bit, 35 MSPS flash converter, made on a high speed bipolar process, which is an alternate source for the TDC1048 unit, offers enhancements over its predecessor. Lower power dissipation makes the AD9048 attractive for a variety of system designs.

Because of its wide bandwidth, it is an ideal choice for real-time conversion of video signals. Input bandwidth is flat with no missing codes.

Clocked latching comparators, encoding logic and output buffer registers operating at minimum rates of 35 MSPS preclude a need for a sample-and-hold (S/H) or track-and-hold (T/H) in most system designs using the AD9048. All digital control inputs and outputs are TTL compatible.

Devices operating over two ambient temperature ranges and with two grades of linearity are available. Linearities of either 0.5 LSB or 0.75 LSB can be ordered for a commercial range of 0°C to 70°C or extended case temperatures of –55°C to +125°C.

Commercial versions are packaged in 28-lead DIPs; extended temperature versions are available in ceramic DIP and ceramic LCC packages. Both commercial units and MIL-STD-883 units are standard products.

The AD9048 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9048/883B data sheet for detailed specifications.

REV. E

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AD9048–SPECIFICATIONS (typical with nominal supplies unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} to DGND . . . . . –0.5 V dc to +7.0 V dc
AGND to DGND . . . . . –0.5 V dc to +0.5 V dc
V_{EE} to AGND . . . . . +0.5 V dc to –7.0 V dc
V_{IN}, V_{RT} or V_{RB} to AGND . . . . . 0.5 V to V_{EE}
V_{RT} to V_{RB} . . . . . –2.2 V dc to +2.2 V dc
CONV, NMINV or NLINV to DGND –0.5 V dc to +5.5 V dc
Applied Output Voltage to DGND . . –0.5 V dc to +5.5 V dc[2]
Applied Output Current, Externally Forced
. . . . . –1.0 mA to +6.0 mA[3, 4]
Output Short-Circuit Duration . . . . . 1.0 sec[5]
Operating Temperature Range (Ambient)
AD9048JJ/KJ/JQ/KQ . . . . . 0°C to 70°C
AD9048SE/SQ/TE/TQ . . . . . –55°C to +125°C
Maximum Junction Temperature (Plastic) . . . . . 150°C[6]
Maximum Junction Temperature (Hermetic) . . . . . 150°C[6]
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Storage Temperature Range . . . . . –65°C to +150°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V; V_{EE} = –5.2 V; Differential Reference Voltage = 2.0 V, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9048JJ/JQ Min	Typ	Max	AD9048KJ/KQ Min	Typ	Max	AD9048SE/SQ Min	Typ	Max	AD9048TE/TQ Min	Typ	Max	Unit
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Nonlinearity	25°C	I		0.4	0.75		0.3	0.5		0.4	0.75		0.3	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Nonlinearity	25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR															
Top of Reference Ladder	25°C	I		5	12		5	12		5	12		5	12	mV
	Full	VI			12			12			12			12	mV
Bottom of Reference Ladder	25°C	I		4	8		4	8		4	8		4	8	mV
	Full	VI			8			8			8			8	mV
Offset Drift Coefficient	Full	V		20			20			20			20		µV/°C
ANALOG INPUT															
Input Voltage Range	Full	V		–2.1; +0.1			–2.1; +0.1			–2.1; +0.1			–2.1; +0.1		V
Input Bias Current[7]	25°C	I		36	60		36	60		36	60		36	60	µA
	Full	VI			100			100			100			100	µA
Input Resistance	25°C	I	200	300		200	300		200	300		200	300		kΩ
	Full	VI	40			40			40			40			kΩ
Input Capacitance	25°C	IV		16	20		16	20		16	20		16	20	pF
Full Power Bandwidth[8]	25°C	IV	10	15		10	15		10	15		10	15		MHz
REFERENCE INPUT															
Positive Reference Voltage[9]	Full	V		0.0			0.0			0.0			0.0		V
Negative Reference Voltage[9]	Full	V		–2.0			–2.0			–2.0			–2.0		V
Differential Reference Voltage	Full	V		2.0			2.0			2.0			2.0		V
Reference Ladder Resistance	Full	VI	30	60	125	30	60	125	30	60	125	30	60	125	Ω
Ladder Temperature Coefficient	Full	V		0.22			0.22			0.22			0.22		Ω/°C
Reference Ladder Current	Full	VI		23	40		23	40		23	40		23	40	mA
Reference Input Bandwidth	25°C	V		10			10			10			10		MHz
DYNAMIC PERFORMANCE[10]															
Conversion Rate	25°C	I	35	38		35	38		35	38		35	38		MHz
Aperture Delay	25°C	IV		2.4	5		2.4	5		2.4	5		2.4	5	ns
Aperture Uncertainty (Jitter)	25°C	IV		25	50		25	50		25	50		25	50	ps
Output Delay (t_{PD})	25°C	I		13	15		9	15		9	15		9	15	ns
Output Hold Time (t_{OH})[11]	25°C	I	5	8		5	8		5	8		5	8		ns
Transient Response[12]	25°C	IV		6	20		6	20		6	20		6	20	ns
Overvoltage Recovery Time[13]	25°C	V		8			8			8			8		ns
Rise Time	25°C	I			9			9			9			9	ns
Fall Time	25°C	I			14			14			14			14	ns
Output Time Skew[14]	25°C	I		4.5	7		4.5	7		4.5	7		4.5	7	ns
NMINV and NLINV INPUTS															
0.4 V Input Current	Full	VI			200			200			200			200	µA
2.4 V Input Current	Full	VI			150			150			150			150	µA
5.5 V Input Current	Full	VI			150			150			150			150	µA
CONVERT INPUT															
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			150			150			150			150	µA
Logic "0" Current	Full	VI			500			500			500			500	µA
Input Capacitance	25°C	IV		4	6		4	6		4	6		4	6	pF
Convert Pulsewidth (LOW)	25°C	I	18			18			18			18			ns
Convert Pulsewidth (HIGH)	25°C	I	10			10			10			10			ns

Parameter (Conditions)	Temp	Test Level	AD9048JJ/JQ Min	Typ	Max	AD9048KJ/KQ Min	Typ	Max	AD9048SE/SQ Min	Typ	Max	AD9048TE/TQ Min	Typ	Max	Unit
AC LINEARITY															
In-Band Harmonics															
dc to 2.438 MHz[15]	25°C	I	47	50		49	55		47	50		49	55		dBc
dc to 9.35 MHz[16]	25°C	V		48			48			48			48		dBc
Signal-to-Noise Ratio (SNR)[15]															
1.248 MHz Input Frequency[17]	25°C	I	43.5	44		45	46		43.5	44		45	46		dB
2.438 MHz Input Frequency[17]	25°C	I	43	44		44	46		43	44		44	46		dB
1.248 MHz Input Frequency[18]	25°C	I	52.5	53		54	55		52.5	53		54	55		dB
2.438 MHz Input Frequency[18]	25°C	I	52	53		53	55		52	53		53	55		dB
Signal-to-Noise Ratio (SNR)[16]															
1.248 MHz Input Frequency[17]	25°C	I	43.5	44		45	46		43.5	44		45	46		dB
9.35 MHz Input Frequency[17]	25°C	V		40.5			40.5			40.5			40.5		dB
Noise Power Ratio (NPR)[19]	25°C	IV	36.5	39		36.5	39		36.5	39		36.5	39		dB
Differential Phase [20]	25°C	IV			1			1			1			1	Degree
Differential Gain [20]	25°C	IV			2			2			2			2	%
DIGITAL OUTPUTS															
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.5			0.5			0.5			0.5	V
Short Circuit Current[5]	Full	VI			30			30			30			30	mA
POWER SUPPLY															
Positive Supply Current	25°C	I		34	56		34	56		34	56		34	56	mA
	Full	VI			58			58			58			58	mA
Negative Supply Current	25°C	I		90	110		90	110		90	110		90	110	mA
	Full	VI			120			120			120			120	mA
Nominal Power Dissipation	25°C	V		550			550			550			550		mW
Reference Ladder Dissipation	25°C	V		45			45			45			45		mW

NOTES

[1]Maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the device may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]Applied voltage must be current-limited to specified range.

[3]Forcing voltage must be limited to specified range.

[4]Current is specified as negative when flowing into the device.

[5]Output High; one pin to ground; one second duration.

[6]Typical thermal impedances (no air flow) are as follows:
Ceramic DIP: θ_{JA} = 49°C/W; θ_{JC} = 15°C/W, LCC: θ_{JA} = 69°C/W; θ_{JC} = 21°C/W, JLCC: θ_{JA} = 59°C/W; θ_{JC} = 19°C/W.
To calculate junction temperature (T_J), use power dissipation (PD) and thermal impedance: T_J = PD (θ_{JA}) + $T_{AMBIENT}$ = PD (θ_{JC}) = + T_{CASE}.

[7]Measured with V_{IN} = 0 V and CONVERT low (sampling mode).

[8]Determined by beat frequency testing for no missing codes.

[9]$V_{RT} \geq V_{RB}$ under all circumstances.

[10]Outputs terminated with 40 pF and eight 10 Ω pull-up resistors.

[11]Interval from 50% point of leading edge CONVERT pulse to change in output data.

[12]For full-scale step input, 8-bit accuracy attained in specified time.

[13]Recovers to 8-bit accuracy in specified time after –3 V input overvoltage.

[14]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[15]Measured at 20 MHz encode rate with analog input 1 dB below full scale.

[16]Measured at 35 MHz encode rate with analog input 1 dB below full scale.

[17]RMS signal to rms noise.

[18]Peak signal to rms noise.

[19]DC to 8 MHz noise bandwidth with 1.248 MHz slot; four sigma loading; 20 MHz encode.

[20]Clock frequency = 4 × NTSC = 14.32 MHz. Measured with 40-IRE modulated ramp.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.

Test Level II – 100% production tested at 25°C and sample tested at specific temperatures.

Test Level III – Sample tested only.

Test Level IV – Parameter is guaranteed by design and characterization testing.

Test Level V – Parameter is a typical value only.

Test Level VI – All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Linearity	Temperature	Package Option[1]
AD9048JJ	0.75 LSB	0°C to 70°C	J-28A
AD9048KJ	0.5 LSB	0°C to 70°C	J-28A
AD9048JQ	0.75 LSB	0°C to 70°C	D-28
AD9048KQ	0.5 LSB	0°C to 70°C	D-28
AD9048SE[2]	0.75 LSB	–55°C to +125°C	E-28A
AD9048TE[2]	0.5 LSB	–55°C to +125°C	E-28A
AD9048SQ[2]	0.75 LSB	–55°C to +125°C	D-28
AD9048TQ[2]	0.5 LSB	–55°C to +125°C	D-28

NOTES
[1]E = Leadless Ceramic Chip Carrier; J = J-Leaded Ceramic; D = Cerdip.
[2]For temperature designation only. MIL-STD-883 and Standard Military Drawing available.

MECHANICAL INFORMATION

Die Dimensions . . . . . 140 × 137 × 21 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Gold
Backing . . . . . None
Substrate Potential . . . . . V_{EE}
Passivation . . . . . Nitride
Die Attach . . . . . Gold Eutectic
Bond Wire . . . . . 1 mil Gold; Gold Ball Bonding

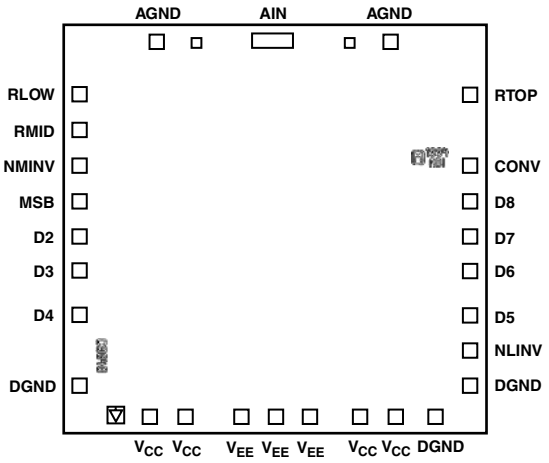
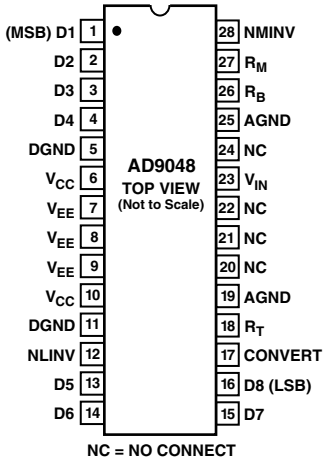


Figure 1. Bonding Diagram

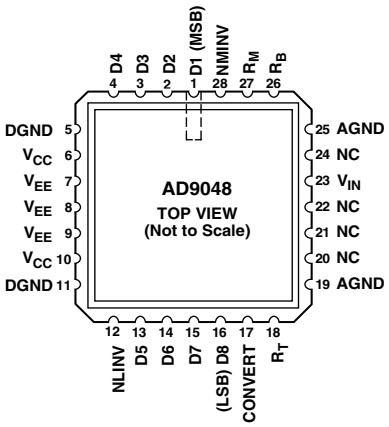
PIN CONFIGURATIONS

DIP (D Package)



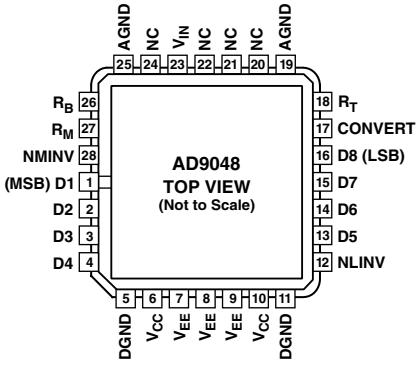
NC = NO CONNECT

LCC (E Package)



NC = NO CONNECT

J-Leaded Ceramic (J Package)



NC = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9048 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin	Description
D1–D8	Eight digital outputs. D1 (MSB) is the most significant bit of the digital output word; D8 (LSB) is the least significant bit.
AGND	One of two analog ground returns. Both grounds should be connected together and to low impedance ground plane near the AD9048.
DGND	One of two digital ground returns. Both grounds should be connected together and to low impedance ground plane near the AD9048.
V_{CC}	Positive supply terminals; nominally +5.0 V.
V_{EE}	Negative supply terminals; nominally –5.2 V.
CONVERT	Input for conversion signal; sample of analog input signal taken on rising edge of this pulse.
R_B	Most negative reference voltage for internal reference ladder.
R_M	Midpoint tap on internal reference ladder.
R_T	Most positive reference voltage for internal reference ladder.
V_{IN}	Analog input signal pin.
NMINV	"Not Most Significant Bit Invert." In normal operation, this pin floats high; logic LOW at NMINV inverts most significant bit of digital output word [D1 (MSB)].
NLINV	"Not Least Significant Bit Invert." In normal operation, this pin floats high; logic LOW at NLINV inverts the seven least significant bits of the digital output word.

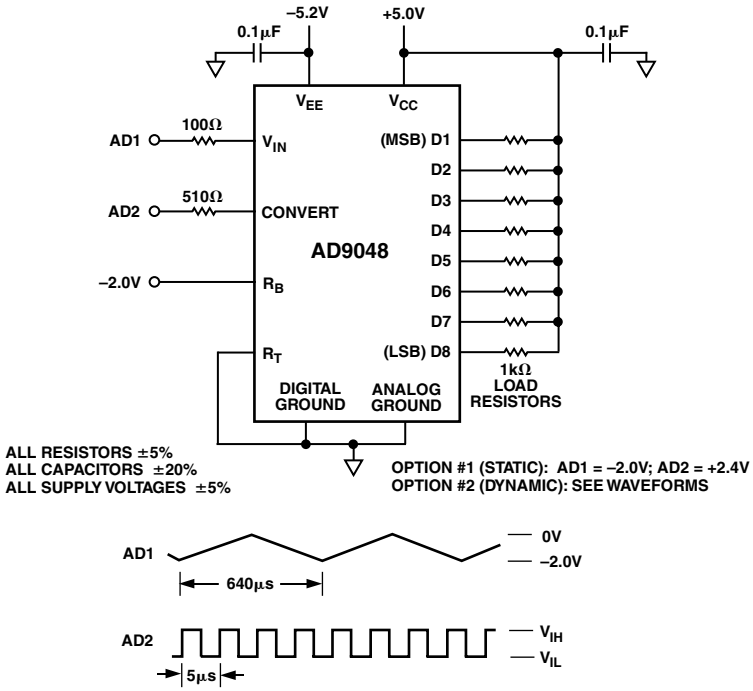


Figure 2. Burn-In Diagram

THEORY OF OPERATION

Refer to the Functional Block Diagram of the AD9048. The AD9048 comprises three functional sections: a comparator array, encoding logic and output latches.

Within the array, the analog input signal to be digitized is compared with 255 reference voltages. The outputs of all comparators whose references are below the input signal level will be high; outputs whose references are above that level will be low.

The n-of-255 code that results from this comparison is applied to the encoding logic where it is converted into binary coding. When it is inverted with dc signals applied to the NLINV and/or NMINV pins, it becomes two's complement.

After encoding, the signal is applied to the output latch circuits where it is held constant between updates controlled by the application of CONVERT pulses.

The AD9048 uses strobed latching comparators in which comparator outputs are either high or low, as dictated by the analog input level. Data appearing at the output pins have a pipeline delay of one encode cycle.

Input signal levels between the references applied to R_T (Pin 18) and R_B (Pin 26) will appear at the output as binary numbers between 0 and 255, inclusive. Signals outside that range will show up as either full-scale positive or full-scale negative outputs. No damage will occur to the AD9048 as long as the input is within the voltage range of V_{EE} to +0.5 V.

The significantly reduced input capacitance of the AD9048 lowers the drive requirements of the input buffer/amplifier and also induces much smaller phase shift in the analog input signal.

Applications that depend on controlled phase shift at the converter input can benefit from using the AD9048 because of its inherently lower phase shift.

The CONVERT, analog input and digital output circuits are shown in Figure 3.

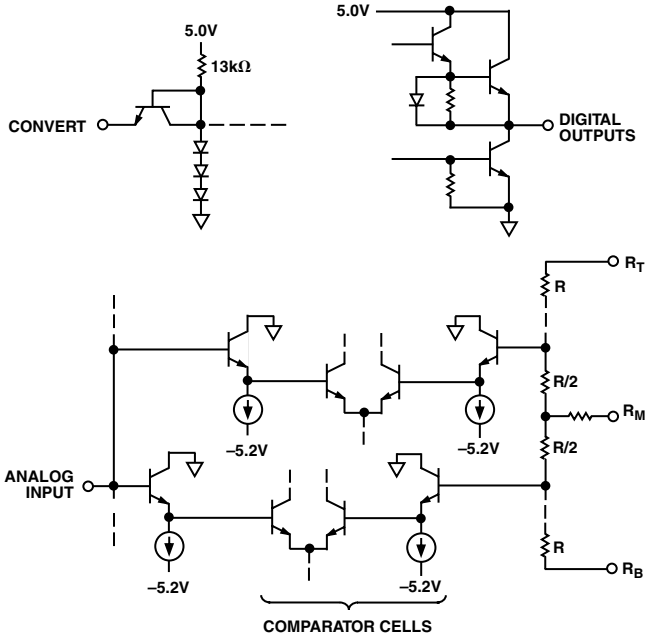


Figure 3. Input/Output Circuits

System timing, which provides details on delays through the AD9048 as well as the relationships of various timing events, is shown in Figure 4.

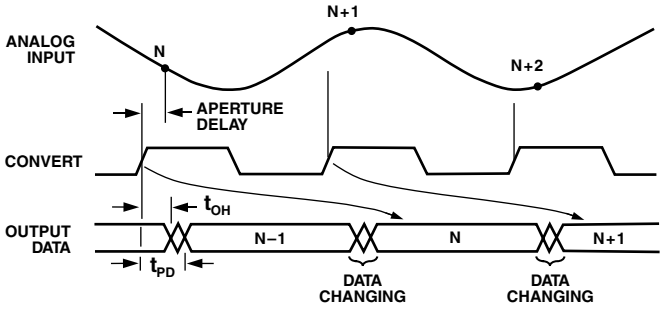


Figure 4. Timing Diagram

Dynamic performance of the AD9048, i.e., typical signal-to-noise ratio, is illustrated in Figures 3 and 4.

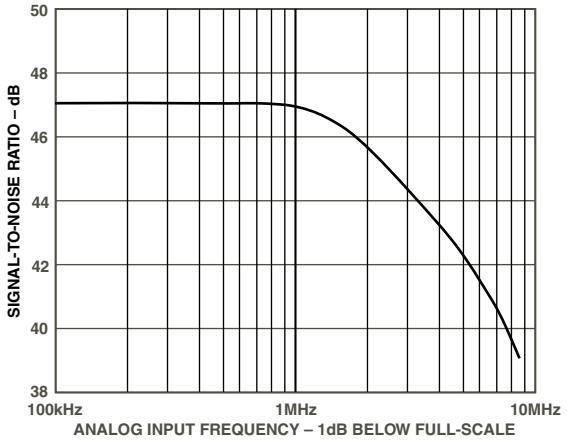


Figure 5. Dynamic Performance (20 MHz Encode Rate)

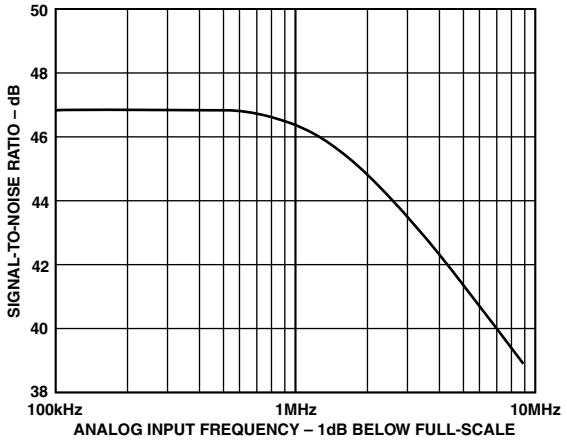


Figure 6. Dynamic Performance (35 MHz Encode Rate)

LAYOUT SUGGESTIONS

Designs that use the AD9048 or any other high speed device must follow some basic layout rules to ensure optimum performance.

The first requirement is to have a large, low impedance ground plane under and around the converter. If the system uses separate analog and digital grounds, both should be solidly connected together, and to the ground plane, as closely to the AD9048 as practical to avoid ground loop currents.

Ceramic 0.1 μF decoupling capacitors should be placed as closely as possible to the supply pins of the AD9048. For decoupling low frequency signals, use 10 μF tantalum capacitors, also connected as closely as practical to voltage supply pins.

Within the AD9048, reference currents may vary because of coupling between the clock and input signals. As a result, it is important that the ends of the reference ladder, R_T (Pin 18) and R_B (Pin 28), be connected to low impedances (as measured from ground).

If the AD9048 is being used in a circuit in which the reference is not varied, a bypass capacitor to ground is strongly recommended. In applications that use varying references, they must be driven from a low impedance source.

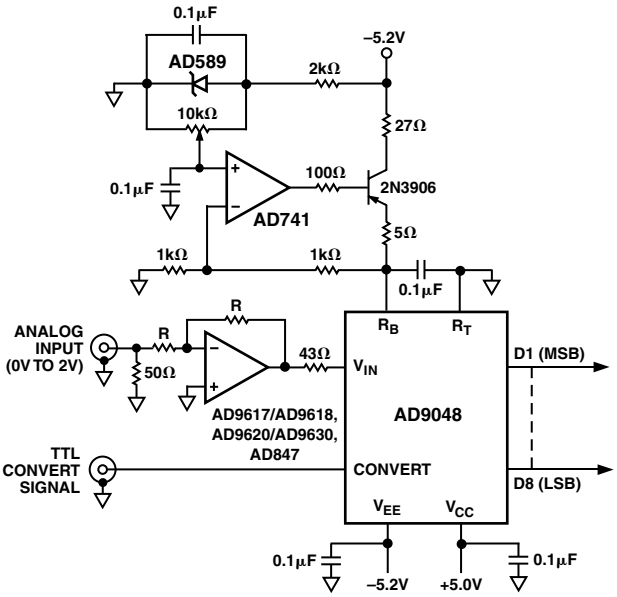


Figure 7. Typical Connections

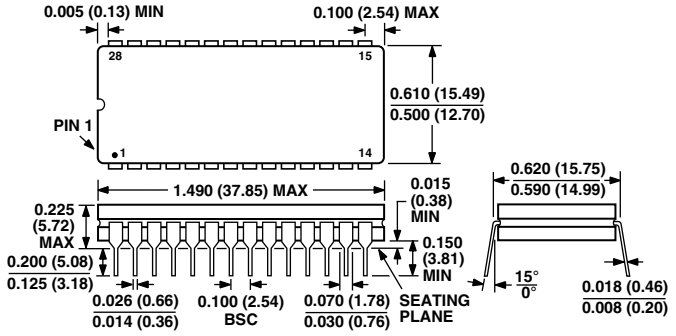
Table I. Truth Table

Step	Range		Binary		Offset Two's Complement	
			True	Inverted	True	Inverted
	–2.000 V FS	–2.0480 V FS	NMINV = 1	0	0	1
	7.8431 mV Step	8.000 mV Step	NLINV = 1	0	1	0
000	0.0000 V	0.0000 V	00000000	11111111	10000000	01111111
001	–0.0078 V	–0.0080 V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	–0.9961 V	–1.0160 V	01111111	10000000	11111111	00000000
128	–1.0039 V	–1.0240 V	10000000	01111111	00000000	11111111
129	–1.0118 V	–1.0320 V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	–1.9921 V	–2.0320 V	11111110	00000001	01111110	10000001
255	–2.0000 V	–2.0400 V	11111111	00000000	01111111	10000000

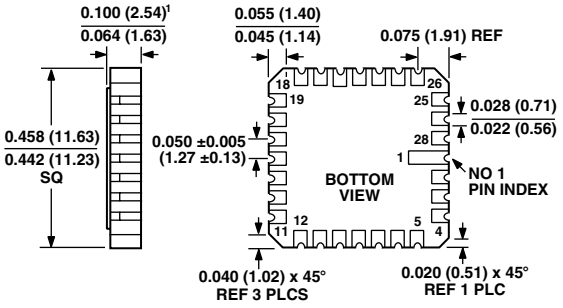
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Ceramic Side-Brazed DIP

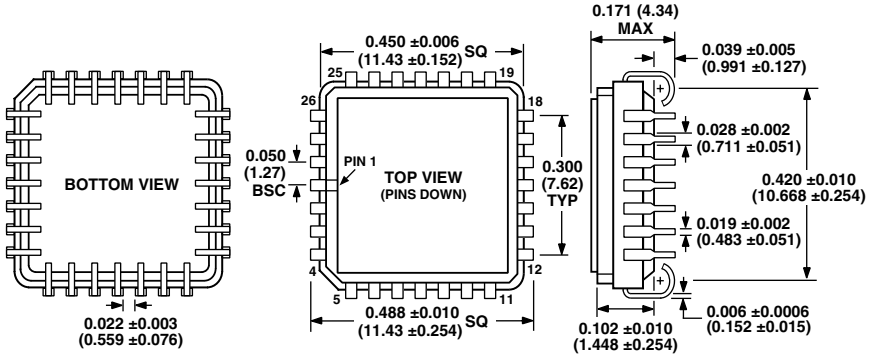


28-Terminal Leadless Chip Carrier



NOTES:
[1]THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS
APPLIES TO ALL FOUR SIDES
ALL TERMINALS ARE GOLD PLATED

28-Lead J-Lead Package



Revision History

Location	Page
09/01—Data Sheet changed from REV. D to REV. E.	
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