ASIX AX88871AP

10/100BASE
Dual Speed “Bripeater” Controller
Data Sheets (08/11/’ 99)

Always contact ASIX for possible updates
before starting a design.

DOCUMENT NO. : AX871A-05.DOC

ASIX ELECTRONICS CORPORATION
2F, NO.13, Industry East Rd. II, Science-based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.
TEL: 886-3-579-9500 FAX: 886-3-579-9558 http://www.asix.com.tw

CONTENTS

FIGURES

1.0 AX88871A Overview

The AX88871A 10/100Mbps Dual Speed "**Bripeater"** Controller is **"a dual speed repeater with build in bridge function"** It is design for low cost dumb HUB application. The AX88871A directly supports up-to eight 10/100Mbps automatic links MII interfaces. Maximum up-to 192 ports can be constructed when using inter-repeater bus horizontally cascades 4 AX88871A and vertically cascades 6 repeaters. When using the legacy method, maximum up-to 64 ports can be constructed when using expansion bus cascades 8 AX88871As. The AX88871A is designed base on IEEE 802.3u clause 27 " Repeater for 100Mb/s base-band networks" It is fully compatible with IEEE 802.3u standard.

All of the ASIX repeater products with the same speeds has the same cascade methodology. So the AX88871A can cascade with AX88850, AX88860 and AX88870 series chips. That is ASIX maintain the consistency of the cascade method for all the repeater product line.

1.1 General Description

The AX88871A Repeater Controller is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. The AX88871A has only Media Independent Interface (MII) to connect to PHY devices. Other then AX88850 series chips that has 2 kinds of interfaces. There are Physical coding sub-layer (PCS) interface and Media Independent Interface (MII).

The AX88871A supports 8 MII interfaces ports, a bridge packet buffer SRAM interface, a 100Mbps port expansion interface and LED display interface.

The AX88871A supports stand along 10/100Mbps dual speed repeater applications. Also it can expand the ports count via cascade to other AX88850 and AX88860 pure 100Mbps repeater chips..

The AX88871A has two application mode.

Mode 0	Single chip repeater application.
Mode 1	Multiple chips cascaded repeater application.

1.2 Features

- IEEE 802.3u repeater compatible
- Supports per port 10/100Mbps alternative with auto detected
- Build in 10/100Mbps Bridge engine with following features
  1. Minimum 32K bytes, maximum 256K bytes SRAM to buffer packets
  2. Seamless buffer management without waste any space of buffer memory
  3. Simple asynchronous 8-bit SRAM interface to reduce system cost
  4. 256 or 1024 entries is supported
  5. Auto learning and filtering
  6. Two forwarding modes are supported : Store-n-Forward and fragment-free
  7. Flow-control is supported optionally.
  8. Buffer RAM auto testing
  9. Routing and Learning at wire speed (148810 packets/sec at 100Mbps)
- Supports 8 10/100Mbps network connections
- 8 dedicated MII interfaces can support 100BASE-TX/T4/FX PHY interfaces
- Port 7 and/or 8 can connect to bridge, switch or MAC type device optionally.
- Up-to 8 repeater chips can be cascaded for large HUB application(old method)
- Up-to 6 repeaters can be cascaded for vertical expansion(new feature)
- Up-to 4 chips can be cascaded locally for horizontal expansion(new feature)
- Support two application mode : single or cascade
- Low latency design supports Class II repeater implementation with large port number
- All ports can be separately isolated or partitioned in response to fault condition
- Separate jabber and partition state machines for each port
- Per-port LED display for Jabber, Partition, Activity. Global partition, RAM test fail and collision, utilization (%) for 10/100Mbps presentation
- Power on LED diagnosis. All the LED display will follow the “ON-OFF-ON-OFF-Normal” operation procedure during/after power on reset
- 208-pin PQFP

1.3 Block Diagram

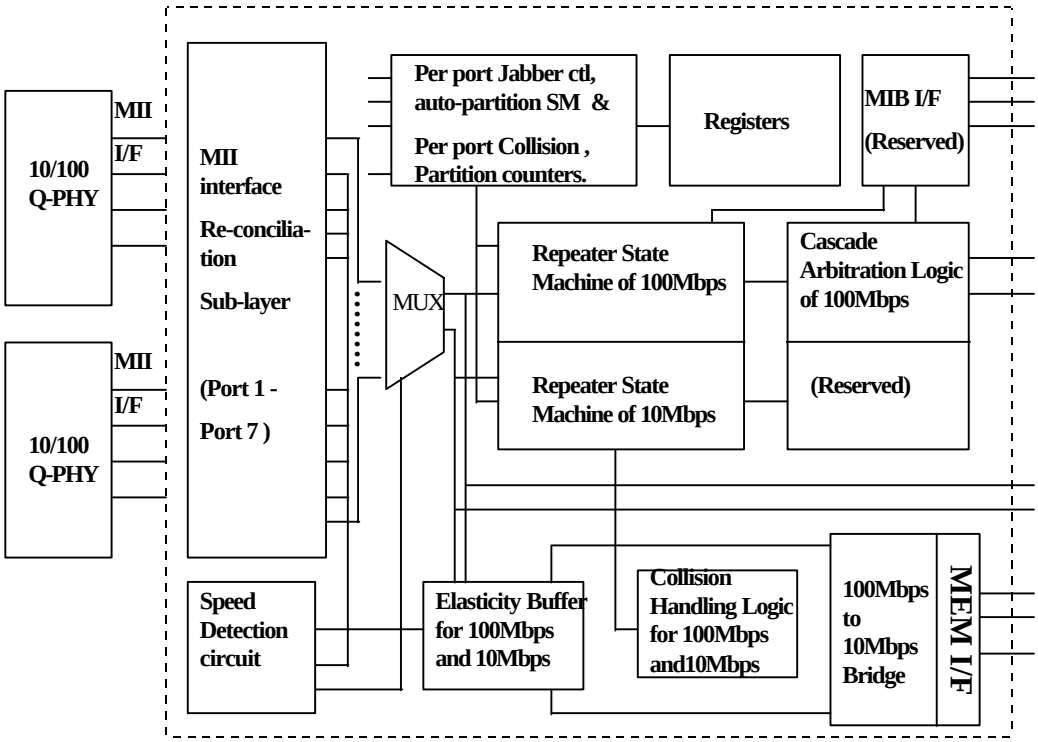


Fig - 1 Chip Block Diagram

1.4 Pin Connection Diagram (mode 0)

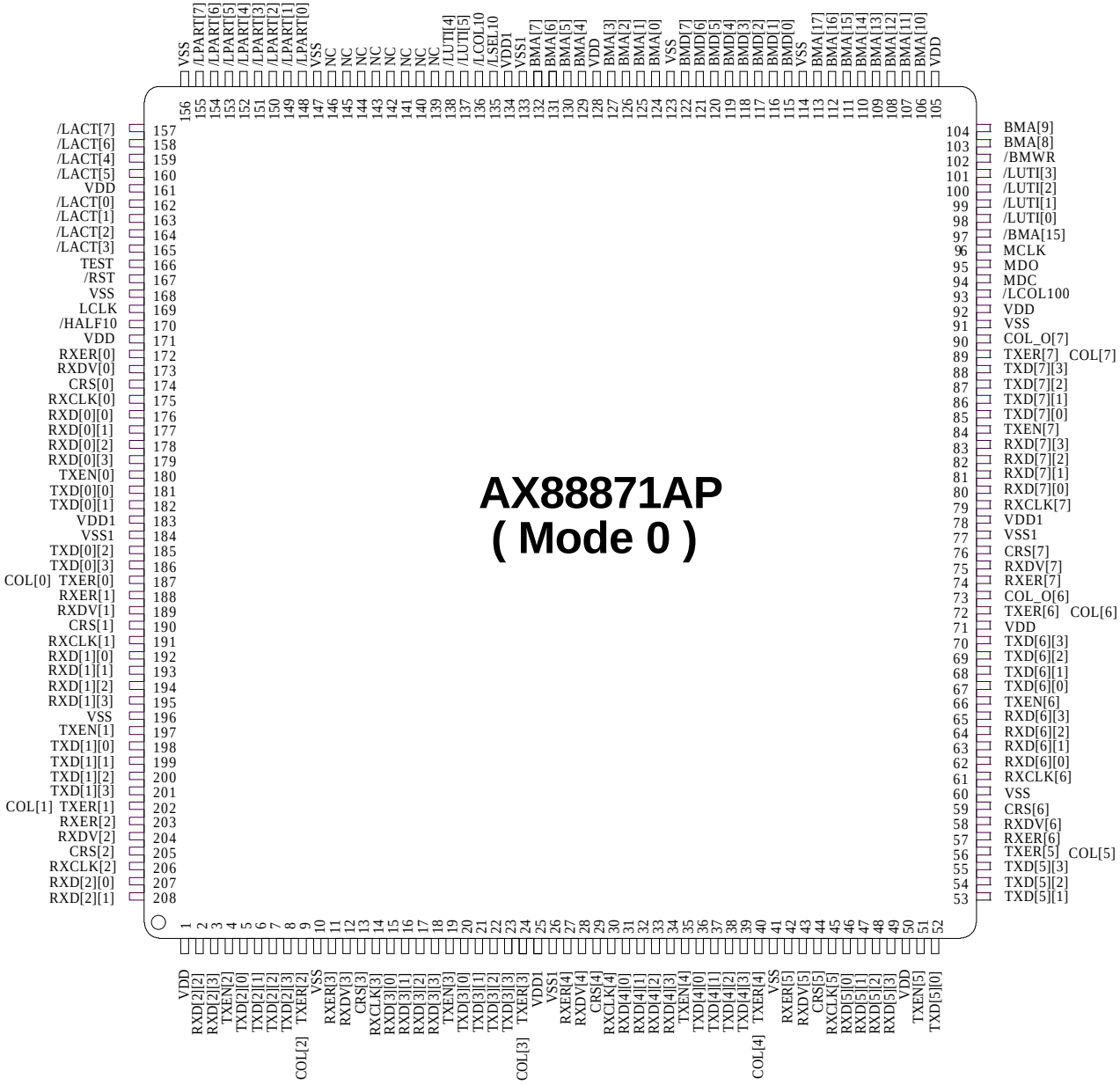


Fig - 2 Pin Connection Diagram for mode 0

Note : Power on configuration setup signals refer section 2.6 cross referance table

1.5 Pin Connection Diagram (mode 1)

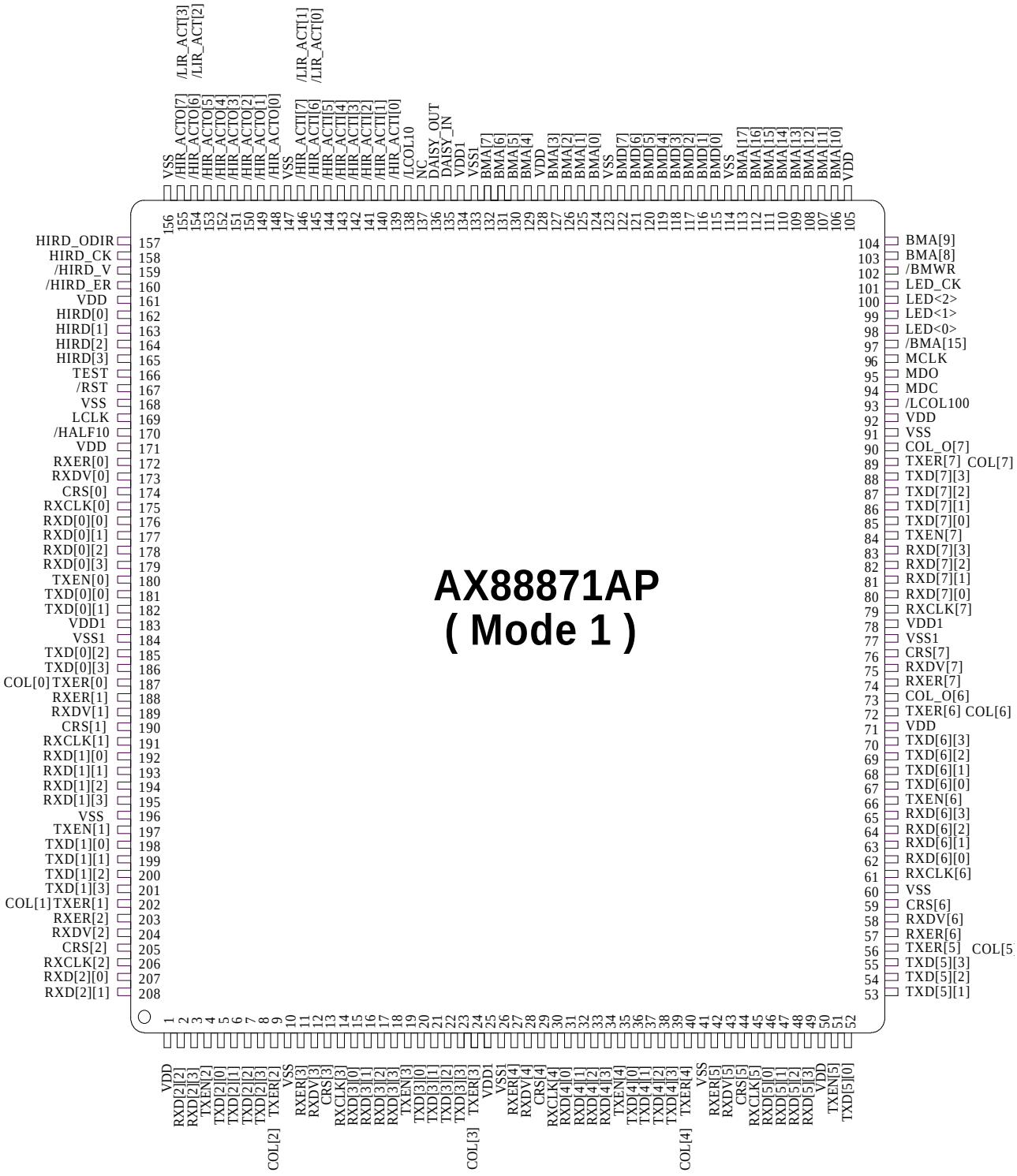


Fig - 3 Pin Connection Diagram for mode 1

Note : Power on configuration setup signals refer section 2.6 cross referance table

2.0 Pin Description

The following terms describe the AX88871A pinout:

All pin names with the "/" suffix are asserted low.

I	=	Input
O	=	Output
I/O	=	Input /Output

2.1 MII interfaces

Signal Name	Type	Pin No.	Description
TXER[7:0] or COL[7:0]	O or I	89, 72, 56 40, 24, 9 202, 187	Transmit Error : When /HALF10 pin set to "high". TXER is transition synchronously with respect to the rising edge of TXCLK . Asserted high when a code violation is request to be send Collision : When /HALF10 pin set to "low". COL is input from PHY, when 10Mbps PHY is in half-duplex mode.
TXD[7:0][3:0]	O	88-85, 70-67 55-52, 39-36 23-20, 8-5 201-198 186-185 182-181	Transmit Data : TXD[3:0] is transition synchronously with respect to the rising edge of TXCLK. For each TXCLK period in which TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY.
TXEN[7:0]	O	84, 66,51 35, 19, 4 197, 180	Transmit Enable : TXEN is transition synchronously with respect to the rising edge of TXCLK. TXEN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
RXD[7:0][3:0]	I	83-80, 65-62 49-46, 34-31 18-15, 3-2 208-207 195-192 179-176	Receive Data : RXD [3:0] is driven by the PHY synchronously with respect to RXCLK.
RXER[7:0]	I	74, 57, 42 27, 11, 203, 188, 172	Receive Error : RXER ,is driven by PHY and synchronous to RXCLK, is asserted for one or more RXCLK periods to indicate to the port that an error has detected.
RXCLK[7:0]	I	79, 61, 45 30, 14, 206, 191, 175	Receive Clock : RX_CLK is a continuous clock that provides the timing reference for the transfer of the RXDV,RXD [3:0] and RXER signals from the PHY to the MII port of the repeater.
RXDV[7:0]	I	75, 58, 43 28, 12, 204, 189, 173	Receive Data Valid : RX_DV is driven by the PHY synchronously with respect to RXCLK. Asserted high when valid data is present on RXD [3:0].
CRS[7:0]	I	76, 59, 44, 29, 13, 205, 190, 174	Carrier Sense : Asynchronous signal CRS is asserted by the PHY when receive medium is non-idle at full duplex mode.
COL_O[6]	O	73	Collision : Collision detection signal for port 6
COL_O[7]	O	90	Collision : Collision detection signal for port 7

2.2 Expansion Bus Interface for 100 Mbps

Signal Name	Type	Pin No.	Description
HIRD[3:0] or /LACT[3:0]	I/O/Z /PU	165-162	INTER REPEATER DATA : When MODE="1" , Nibble data input/output. Transfer data from the "active" AX88871A to all other "inactive" AX88871As. The bus-master of the IRD bus is determined by IR_VECT bus arbitration. /LACT[3:0] : When MODE="0" , Those pins drive activity[3:0] LEDs directly.
/HIRD_V or /LACT[4]	I/O/Z /PU	159	INTER REPEATER DATA VALID : When MODE="1" ,This signal reflect the RX_DV status of the active port across the inter repeater bus. Used to frame good packets. /LACT[4] : When MODE="0" , This pin drives port 4 activity LED directly.
/HIRD_ER or /LACT[5]	I/O/Z /PU	160	INTER REPEATER DATA ERROR: When MODE="1" ,This signal reflect the RX_ER status of the active port across the inter repeater bus. Used to track receive errors from the PHY in real time. /LACT[5] : When MODE="0" , This pin drives port 5 activity LED directly.
HIRD_CK or /LACT[6]	I/O/Z /PU	158	INTER REPEATER CLOCK VALID : When MODE="1" ,All inter repeater signals are synchronized to the rising edge of this clock. /LACT[6] : When MODE="0" , This pin drives port 6 activity LED directly.
HIRD_ODIR or /LACT[7]	O	157	INTER REPEATER DATA IN/OUT DIRECTION : When MODE="1" ,This pin indicates the direction of data for external transceiver. "High" = IRD[3:0], /IRD_ER, /IRD_V , IRD_CK are Output. "Low" = IRD[3:0], /IRD_ER, /IRD_V , IRD_CK are Input. /LACT[7] : When MODE="0" , This pin drives port 7 activity LED directly.
/HIR_ACTO[5:0] or /LPART[5:0]	I/O/OC	153-148	INTER REPEATER ACTIVITY IN/OUT: When MODE="1", The local repeater activity appearance, the signal of the related RID (Repeater ID) will be asserted and as a output pin. All other pins serve as input pins but except the collision conditions. When collision occurred , the signal of related (RID-1) pins will also served as outputs and will active during local collision period. The exception case is when RID = 0, then (RID-1) is replaced with (RID+1). /LPART[5:0] : When MODE="0" , Those pins drive partition[5:0] LEDs directly.
/HIR_ACTO[7:6] or /LIR_ACT[3:2] or /LPART[7:6]	I/O/OC	155-1154	INTER REPEATER ACTIVITY IN/OUT: When MODE ="1" and STACK ="1" the function is the same as /HIR_ACTO[5:0]. LOCAL REPEATER ACTIVITY IN/OUT : When MODE ="1" and STACK ="0" the function is the same as /HIR_ACTO[5:0] but for local repeater activity only. /LPART[7:6] : When MODE="0" , Those pins drive partition[7:6] LEDs directly.
/HIR_ACTI[5:0] or NC[5:0]	I/PU	144-139	INTER REPEATER ACTIVITY IN: These pins perform the same function as /IR_ACTO[7:0] when they serve as input function. Then the /IR_ACTO[7:0] insert external buffers the input function must be replaced with /IR_ACTI [7:0]. NC : When MODE="0" , Those pins keep no connection.
/HIR_ACTI[7:6] or /LIR_ACT[1:0] or NC[7:0]	I/O/PU	146-145	INTER REPEATER ACTIVITY IN : When MODE ="1" and STACK ="1" the function is the same as /HIR_ACTI[5:0]. LOCAL REPEATER ACTIVITY IN/OUT : When MODE ="1" and STACK ="0" the function is the same as /HIR_ACTO[5:0] but for local repeater activity only. NC : When MODE="0" , Those pins keep no connection.

2.3 LED Display

<table>
<tr><th>Signal Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>LED[2:0]

or
/LUTI[2:0]</td><td>O</td><td>100-98</td><td>LED Display Information : When MODE="1" , Those signals indicate each port's Partition, Jabber, Activity, Collision (global), Repeater ID, Utilization % (global), Collision % (global) in sequence. For detail , see the LED timing specification
/LUTI[2:0] : When MODE="0" , Those pins drive utilization[2:0] LEDs directly.

The Utilization % display define as following : (See Note 1 also)
<table>
<tr><th>Utilization %</th><th>LED0</th><th>LED1</th><th>LED2</th><th>LED3</th><th>LED4</th><th>LED5</th><th>LED6</th><th>LED7</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>30</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>40</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>60</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>80+</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
The Collision % display define as following :
<table>
<tr><th>Collision %</th><th>LED0</th><th>LED1</th><th>LED2</th><th>LED3</th><th>LED4</th><th>LED5</th><th>LED6</th><th>LED7</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>5</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>10</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>20</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>30</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>60+</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>LED_CK
or

/LUTI[3]</td><td>O</td><td>101</td><td>LED clock signal : When MODE="1" , The signal is a discontinue clock for LED signals serial shift out. The clock period width is 40nS and last 16 cycle with every 125ms repeated.
/LUTI[3] : When MODE="0" , This pin drive utilization[3] LED directly.</td></tr>
<tr><td>/LCOL10
or
/LUTI[4]</td><td>O/Z</td><td>138</td><td>Collision LED for 10Mbps : When MODE="1" , This pin indicates 10Mbps repeater collision occurred.
/LUTI[4] : When MODE="0" , This pin drive utilization[4] LED directly.</td></tr>
<tr><td>NC
or
/LUTI[5]</td><td>O</td><td>137</td><td>NC : When MODE="1" , The pin function is reserved.

/LUTI[5] : When MODE="0" , This pin drive utilization[5] LED directly.</td></tr>
<tr><td>/LCOL100</td><td>O/Z</td><td>93</td><td>Collision LED for 100Mbps : This pin indicates 100Mbps repeater collision occurred.</td></tr>
</table>

Note : The Utilization % display define as following for Mode 0 LED direct driving.

Utilization %	/LUTI0	/LUTI1	/LUTI2	/LUTI3	/LUTI4	/LUTI5
0	1	1	1	1	1	1
1	0	1	1	1	1	1
5	0	0	1	1	1	1
10	0	0	0	1	1	1
15	0	0	0	0	1	1
30	0	0	0	0	0	1
60	0	0	0	0	0	0

Note 1 :
The calculation formulas of Traffic Utilization between ASIX and NetCom is difference, so you will get different results when using SmartBit (SB) testing this item.
We found the SmartBit calculate the Utilization without include 96 Bit time inter frame gap. So the utilization value can be 100%. As well as we found SB used min packet size (64 byte) and min IFG (96 bit-time) as 100% utilization. In theory, when max packet size(1518 byte) and min IFG the utilization will be more than 100%, but SB also treat it as 100%.
In our AX88871 design, we use real cable bandwidth as calculation base. We calculate the bit counts of carrier within a unit time. Because of the existence of inter frame gap, In our calculation 100% utilization is impossible. So the above two cases (64 byte packet size and 1518 byte packet size with min. IFG), we will count as 85.7% and 99.2%.
If using SB test result to indicate utilization LED the value must be modified. See the following reference table.

ASIX's Utilization%	1	5	10	15	30	60
SmartBit's Utilization%	2	7	12	17	34	68

2.4 Buffer memory pins group

Signal Name	Type	Pin No.	Description
BMA[17:0]	O	113-106, 104, 103, 132-129, 127, 124	Buffer address bus.
BMD[7:0]	I/O	122-115	Buffer data bus.
/BMWR	I/O	102	Memory control pin for write.
/BMA[15]	I/O	97	Invert Buffer address 15.

2.5 Miscellaneous

Signal Name	Type	Pin No.	Description
LCLK	I	169	Local Clock : Must be run at 25Mhz . Used for transmit data to PHY devices,
/RST	I	167	Reset : The chip is reset when this signal is asserted Low.
DAISY_IN or /LSEL10	I/PU	135	Repeater Identification Number Daisy-Chain In : When MODE="1" , This pin is a daisy chain serial input for Repeater ID. A state machine always monitor the input if a correct data (RID) present at the pin, the (RID+1) will be written to RID register and override the power on setup RID for the chip. /LSEL10 : When MODE="0" , This pin select 10Mbps global LED status (utilization (%) and collision (%)) when ' low' ; Otherwise , 100Mbps LED status is selected.
DAISY_OUT or /LCOL10	O/ML	136	Repeater Identification Number Daisy-Chain Out : When MODE="1" , This pin is periodically shift out the RID of itself to the next chained chip to inform that this ID has already been occupied. The RID is shift out periodically every about 200us. /LCOL : When MODE="0" , This pin drives 10Mbps collision LED directly.
MCLK	O	96	MII Clock Out : 2.5MHz 10Mbps MII reference clock
MDO	O	95	Station Management Data Out : For setup PHY auto-negotiation registers. A burst write commands are issue to setup PHY register after reset. The PHY address 4h, 5h, 6h, 7h, 8h, 9h,Ah and Bh will be written as register 4h to value 00A1h (Advertise register set to 10/100 half-duplex mode)and register 0h to value 1000h(Enable auto-negotiation).
MDC	O	94	Station Management Data Clock Out : For MDO reference clock.
TEST	I/PD	166	Test Pin : The pin is just for test mode setting purpose only. Must be pull low when normal operation.
/HALF10	I/PU	170	Half-duplex mode in 10Mbps : Pull low with 10K ohm resister for 10Mbps PHY in half-duplex mode.
VDD	I	1, 25, 50, 71, 78, 92 105, 128, 134, 161, 171, 183	POWER : +5V +/-5%
VSS	I	10, 26, 41 60, 77, 91, 114, 123, 133, 147, 156, 168, 184, 196	POWER: 0V

2.6 Power on configuration setup signals cross reference table

Signal Name	Share with	Description
OPT[6]	COL_O[6]	OPT[6] : Option for external device type to connect to port 6. Default 'high' is for PHY type device. Otherwise, 'low' for bridge, switch or MAC type device.
OPT[7]	COL_O[7]	OPT[7] : Option for external device type to connect to port 7. Default 'high' is for PHY type device. Otherwise, 'low' for bridge, switch or MAC type device.
OPT[0]	TXEN7	OPT[0] : Option for LED display. Default 'high' for normal operation. User may pull the pin '**low**' with 10K ohm resister to force 10M or 100M LED disable when all the ports are the same speed condition.
OPT[1]	TXD[5][3]	OPT[1] : Option for partition schime. Default 'high' for normal operation. User may pull the pin '**low**' with 10K ohm resister to force hardly enter partition state.
TXM_MODE	TXD[6][3]	TXM_MODE : Option for internal used. Default 'high' user may pull the pin 'low' with 10K ohm resister for reserve transmition mode alternaty.
MODE	TXD[6][2]	MODE = 0 : Single chip repeater application. MODE = 1 : Multiple chips cascaded repeater application.
OPT[3]	TXD[6][1]	OPT[3] : Option for internal used. Please keep the pin with default value.
EN_FLOW_CTL	TXD[6][0]	EN_FLOW_CTL = 0 : Disable flow control function. EN_FLOW_CTL = 1 : Enable flow control function.
ST_FW	TXD[7][3]	ST_FW : Default 'high' for Store and Forward mode. User may pull the pin '**low**' with 10K ohm resister to seting to Fragment Free mode.
ENTRIES	TXD[7][2]	ENTRIES = 0 : 1024 entries supported ENTRIES = 1 : 256 entries supported
MEM_SIZE[1] MEM_SIZE[0]	TXD[7][1] TXD[7][0]	MEM_SIZE[1] MEM_SIZE[0] SIZE (K) 1 1 32K 1 0 64K 0 1 128K 0 0 256K
/IR_ACT_EN	/BMWR	Inter Repeater Active Input Pin Enable : This input active low to enable /HIR_ACTI[7:0] pins as inter-repeater carrier sense detection input. Otherwise, /HIR_ACTI[7:0] pins are disabled. The setup works only in MODE = 1.
/DIS_DAISY	/BMA[15]	/DIS_DAISY : Default pull-up to enable daisy chain function. To disable daisy chain function pull the pin down external.
STACK	TXD[5][2]	Stack option : Default is level one using the legacy expansion method to cascade 8 repeater chips. When pull the pin low with 10K ohm resister, using inter-repeater bus horizontally cascades 4 AX88771s and vertically cascades 6 repeaters maximum up-to 192 ports can be constructed.
LRID[1]	TXD[5][1]	Local Repeater Identification Number LRID[1]: When power on reset this pin as inputs to setup the local repeater ID of the chip. LRID[1:0] indicate the local repeater ID from 0 to 3.
LRID[0]	TXD[5][0]	Local Repeater Identification Number LRID[0]: When power on reset this pin as inputs to setup the local repeater ID of the chip. LRID[1:0] indicate the local repeater ID from 0 to 3.
RID[2]	MCLK	Repeater Identification Number RID[2]: When power on reset this pin as inputs to setup the repeater ID of the chip. RID[2:0] indicate the repeater ID from 0 to 7.
RID[1]	MDO	Repeater Identification Number RID[1]: When power on reset this pin as inputs to setup the repeater ID of the chip. RID[2:0] indicate the repeater ID from 0 to 7.
RID[0]	MDC	Repeater Identification Number RID[0]: When power on reset this pin as inputs to setup the repeater ID of the chip. RID[2:0] indicate the repeater ID from 0 to 7.

All of the above signals are pull-up for default values.

3.0 Functional Description

BLANK NOW

Fig - 4 Functional Block Diagram

3.1 Repeater State Machine

The repeater state machine is used to control repeater behavior, generates right signal in corresponding states. The repeater state machine is in Idle state when there is no carrier presented on any ports **.** When there is only one port has receive activity, the repeater state machine will enter Data - forwarding State to ensure correct data forwarding to other connected ports. If collision happens anytime, The repeater state machine detects collision then send jam pattern to all ports until collision ceases.

idle State

The idle state happens when these conditions exists:

a. /RST is low.
b. All CRS[7:0] and DCRS are not asserted high in single chip application.
c. Repeater sense no inter repeater active signal in cascade application, that is, all /IR_ACTO[7:0] remains high.

Data Forwarding State

The state happens when these conditions exists:

a. Only one signal asserted among CRS[7:0] and DCRS in single chip application.
b. Only one of IR_ACTO[7:0] become low if in cascade application.

The repeater state machine stores receiving packet and transmits to all other ports except for

1. The port is jabbered.
2. The port is isolated.

Collision State

The Collision State happens when these conditions exists:

a. There are two or more signals asserted high among CRS[7:0] and DCRS in single chip system.
b. There are two or more signals asserted low among /IR_ACTO[7:0] in cascade system.
c. Only one carrier exists but RXDV still low exceeds 4 clock cycles.The repeater sends collision pattern to all ports.

One Port Left State

The state happens only when there is no collision but still one port which experienced collision has receive activity. The repeater remains send collision pattern to all ports except the port.

3.2 RXE /TXE CONTROL

Idle state

The repeater sends no data to any port.
RXE(ALL) = 0, RXE_IR = 0.
TXE(ALL) = 0, TXE_IR = 0.

Data Forwarding state

If ACTIVE(X) = 1, X is the local connected port,
RXE(X) = 1, RXE(ALL-X) = 0, RXE_IR = 0.
TXE(X) = 0, TXE(ALL-X) = 1, TXE_IR = 1.

If ACTIVE(X) = 1, X is the inter repeater port,
RXE(ALL) = 0, RXE_IR =1.
TXE(ALL) = 1, TXE_IR = 0.

Collision state

The repeater sends jam pattern to all ports.
RXE(ALL) = 0, RXE_IR = 0.
TXE(ALL) = 1, TXE_IR = 0.

One Port Left state

The repeater sends jam pattern to all other port except for the still activity port.
RXE(ALL) = 0, RXE_IR = 0.
TXE(ALL-X) = 1, TXE_IR = 0. Suppose X is the one left port.

3.3 Jabber State Machine

To prevent an illegally long reception of data from reaching the repeater unit, each port has its own jabber timer. If a reception exceeds this duration (64K bit times for AX88871A), the jabber condition will be detected. In this condition, repeater unit will disable receive and transmit packets for the jabbered port and the other ports remain the normal operation.

When the carrier is no longer detected for the jabbered port or reset the repeater, the jabber function will be clear and re-enable reception and transmission.

3.4 Partition State Machine

The partition state machine is used to protect network from being upset when a port suffer continuous collision, each port uses a partition state machine to detect and prevent this condition. When a port suffer from continuous 64 times of collision events, then it goes to partition state. The partitioned port will be not released until a packet without collision be transmitted(more than 512 bit times for AX88871A) or reset the repeater.

3.5 Expansion Logic(Cascade Interface)

The expansion logic is used to stack numerous repeaters to expend the number of connected ports. The expansion logic can be divided into two types:

Expansion Logic without Buffer (minimum mode)

In this mode, use /IR_ACTO[7:0] to cascade repeaters in back plane. Just connect /IR_ACTO[7:0] of all repeaters without using buffer. This mode is supposed to cascade repeaters on the same board. In this application, the stackable system can reach to 4 repeaters.

Expansion Logic with Buffer (maximum mode)

This mode is entered with the setting of /DIS_DMII = 0, the dedicated port isn‘t existed again in this mode. Now the dedicated pins DRXD[3:0], DCRS, DRX_DV, DRX_ER, DRX_CLK play a role as IR_ACTI[7:0]. Use /IR_ACTO[7:0] and /IR_ACTI[7:0] to cascade repeaters in back plane. Buffers are used both in /IR_ACTO[7:0] and /IR_ACTI[7:0]. The mode is supposed to cascade repeaters on different boards via cables. In this application, the stackable system can reach to 8 repeaters.

/IR_ACTO<7:0> are driven according to repeater ID and receive activity of local connected ports as follows:

Repeater ID	IDLE state	Only One Port Activity	More than One Port Activity
000	11111111	11111110	11111100
001	11111111	11111101	11111100
010	11111111	11111011	11111001
011	11111111	11110111	11110011
100	11111111	11101111	11100111
101	11111111	11011111	11001111
110	11111111	10111111	10011111
111	11111111	01111111	00111111

Note: All /IR_ACTO[7:0] will be in open-drain status when they aren‘t driven. These signals present high via external pull high resister.

3.6 Data Flow control

The signals on the IR bus (such as IRD[3:0], IRD_V_N, IRD_ER_N, IRD_CK) flow either into or out of the repeater depending upon the repeater‘s state. Only if the repeater receive packet from local port without collision occurs, the IR signals flow out of repeater. Otherwise, these IR signals flow into repeater.

In cascade system, it must guarantee that only one repeater drives these signals to avoid contention.

3.7 RID Receive-Transmit Interface(Daisy Chain Logic)

In the cascade system, repeater ID of each chip will be re-arranged by serial in/serial out daisy chain logic. The logic use DAISY_IN pin to monitor the RID value of the previous chained chip, and override the original ID of the current chip with the value of (RID+1) . Use the DAISY_OUT pin to periodically (about 200us) send out the exact RID of the current chip to inform the next chained chip. By this way, each repeater chip in 8 AX88871A stackable application will keep unique ID of itself. The RID is used in inter repeater bus arbitration.

DAISY_IN/OUT frame format

idle	start bit	data0	data1	data2	data3
1	0	RID[0]	RID[1]	RID[2]	PARITY

Notes: PARITY = 1 when sum of 1‘s in RID[2:0] is even

If no daisy-chain input, that is, DAISY_IN keep high, the RID of current chip can be clear to 0 during time out period. The timer for time out is about 4sec.

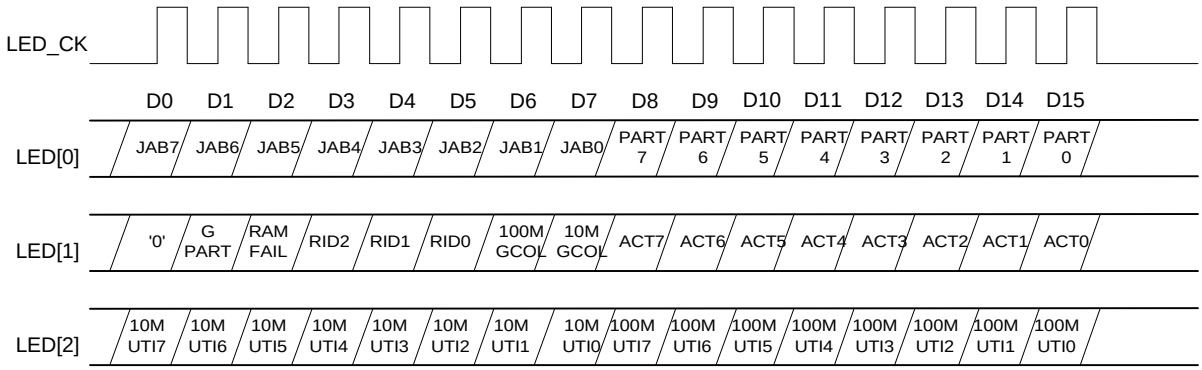
There are a input setting , /DIS_DAISY, which enable/disable daisy-chain function. With the low setting , the RID of current chip don‘t care the present data on DAISY_IN and can‘t be overrided.

3.8 LED Display Interface

AX88871A provides per-port LED status indication for partition, jabber, activity and support rate - based LED for global partition and collision, utilization (%) for 10/100Mbps. .Detail function is described on the previous pin description(LED interface). LED[2:0] are all active low. There are two display ways : complicated and simple way. It depends on the setting of MODE.

Multiple chips cascaded application (MODE = 1)

LED[2:0] Status Driver Wave-form as follows :



Notes: a. PART7~0indicates partition status for each port
b. JAB7~0 indicates jabber status for each port
c. ACT7~0 indicates activity status for each port
d. RID2~0 is the ID of repeater chip
e. 10M UTI7~0 indicate global utilization rate of 10Mbps for each 104.8ms sampling period.
f. 100M UTI7~0 indicate global utilization rate of 100Mbps for each 104.8ms sampling period.
g. 10M GCOL indicate global collision
h. 100M GCOL indicate global collision
i. GPART : indicate global partition.
J. RAM FAIL : Bridge RAM test fail.

It must use external shift register to decode data on LED[2:0]. The application shows as follows:

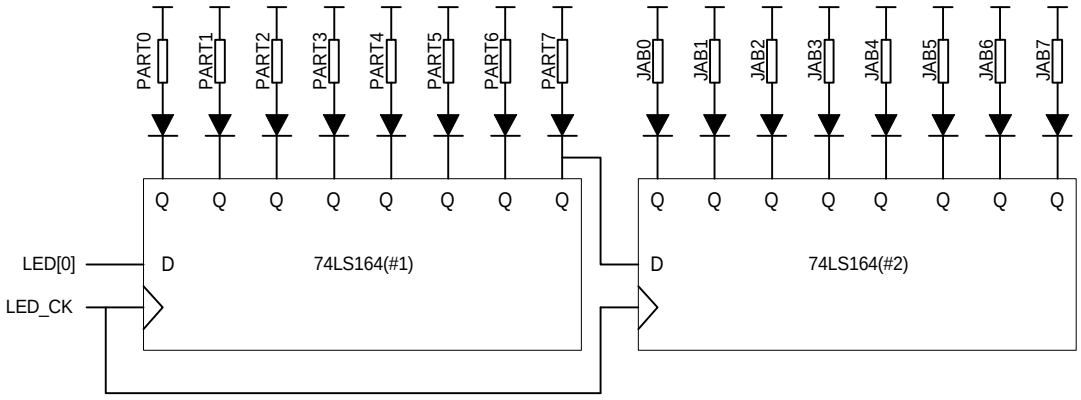


Fig - 5 Application for LED display

If the user don‘t want to show jabber status, take away the latter 74LS164(#2). The application is the same for LED[2:1].

Single chip application (MODE=0)

In this mode, the inter repeater pins are not useful, these pin can be used for display led status directly. Then the led application become simple.

	dump signal		dump signal		dump signal
/HIR_ACTO[0]	/PART[0]	HIRD[0]	/ACT[0]	LED[0]	/UTI[0]
/HIR_ACTO[1]	/PART[1]	HIRD[1]	/ACT[1]	LED[1]	/UTI[1]
/HIR_ACTO[2]	/PART[2]	HIRD[2]	/ACT[2]	LED[2]	/UTI[2]
/HIR_ACTO[3]	/PART[3]	HIRD[3]	/ACT[3]	LED_CK	/UTI[3]
/HIR_ACTO[4]	/PART[4]	/HIRD_V	/ACT[4]	HMD	/UTI[4]
/HIR_ACTO[5]	/PART[5]	/HIRD_ER	/ACT[5]	HTX_RDY	/UTI[5]
/HIR_ACTO[6]	/PART[6]	HIRD_CK	/ACT[6]	DAISY_OUT	/LCOL10
/HIR_ACTO[7]	/PART[7]	HIRD_ODIR	/ACT[7]	/LCOL100	/LCOL100

4.0 INTERNAL REGISTERS

4.1 Configuration Register (CONFIG)

Bit	Bit Name	Access	Bit Description
D14	/HALF10	R/W	Half-duplex mode in 10Mbps : "low" resister to 10Mbps PHY in half-duplex mode. "high" resister to 10Mbps PHY in full-duplex mode.
D13	OPT[0]	R/W	OPT[0] : Option for LED display. Default 'high' for normal operation. User may pull the pin '**low**' with 10K ohm resister to force 10M or 100M LED disable when all the ports are the same speed condition.
D12	OPT[1]	R/W	OPT[1] : Option for partition schime. Default 'high' for normal operation. User may pull the pin '**low**' with 10K ohm resister to force hardly enter partition state.
D11	TXM_MODE	R/W	TXM_MODE : Option for internal used. Default 'high' user may pull the pin 'low' with 10K ohm resister for reserve transmition mode alternaty.
D10	OPT[3]	R/W	OPT[3] : Option for internal used. Please keep the pin with default value.
D9	OPT[4]	R/W	OPT[4] : No Used.
D8	OPT[6]	R/W	OPT[6] : Option for external device type to connect to port 6. Default 'high' is for PHY type device. Otherwise, 'low' for bridge, switch or MAC type device.
D7	OPT[7]	R/W	OPT[7] : Option for external device type to connect to port 7. Default 'high' is for PHY type device. Otherwise, 'low' for bridge, switch or MAC type device.
D6	MODE	R/W	MODE = 0 : Single chip repeater application. MODE = 1 : Multiple chips cascaded repeater application.
D5	ST_FW	R/W	ST_FW = 0 : fragment-free mode ST_FW =1 : Store-n-Forward mode
D4	ENTRIES	R/W	ENTRIES = 0 : 1024 entries supported ENTRIES = 1 : 256 entries supported
D3-2	MEM_SIZE[1] MEM_SIZE[0]	R/W	MEM_SIZE[1] MEM_SIZE[1] SIZE (K) 1 1 32K 1 0 64K 0 1 128K 0 0 256K
D1	/IR_ACT_EN	R/W	Inter Repeater Active Input Pin Enable : This input active low to enable /HIR_ACTI[7:0] pins as inter-repeater carrier sense detection input. Otherwise, /HIR_ACTI[7:0] pins are disabled.
D0	/DIS_DAISY	R/W	/DIS_DAISY : Default pull-up to enable daisy chain function. To disable daisy chain function pull the pin down external.

4.2 Repeater ID Register

Bit	Bit Name	Access	Bit Description
D2-D0	RID[2:0]	R/W	Repeater ID : At the rising edge of /RST , the value of RID[2:0] are latched in this register as D[2:0]. The setting of RID[2:0]can be override according to the data from serial daisy-chain DAISY_IN pin input . Note that in system application, the maximum of 8 devices can be cascade.

5.0 ELECTRICAL SPECIFICATION AND TIMING

5.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vcc	-0.5	+7	V
Input Voltage	Vin	Vss-0.5	Vdd+0.5	V
Output Voltage	Vout	Vss-0.5	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+235	°C

Note : Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability

5.2 General Operation Conditions

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+70	°C
Supply Voltage	Vdd	+4.75	+5.25	V

5.3 DC Characteristics

(Vdd=4.75V to 5.25V, Vss=0V, Ta=0°C to 70°C)

Description	SYM	Min	Max	Units
Low Input Voltage	Vil	Vss-0.5	0.8	V
High Input Voltage	Vih	2	Vdd+0.5	V
Low Output Voltage	Vol		0.4	V
High Output Voltage	Voh	2.4		V
Input Leakage Current 1 (Note 1)	Iil1		10	uA
Input Leakage Current 2 (Note 2)	Iil1		500	uA
Output Leakage Current	Iol		10	uA

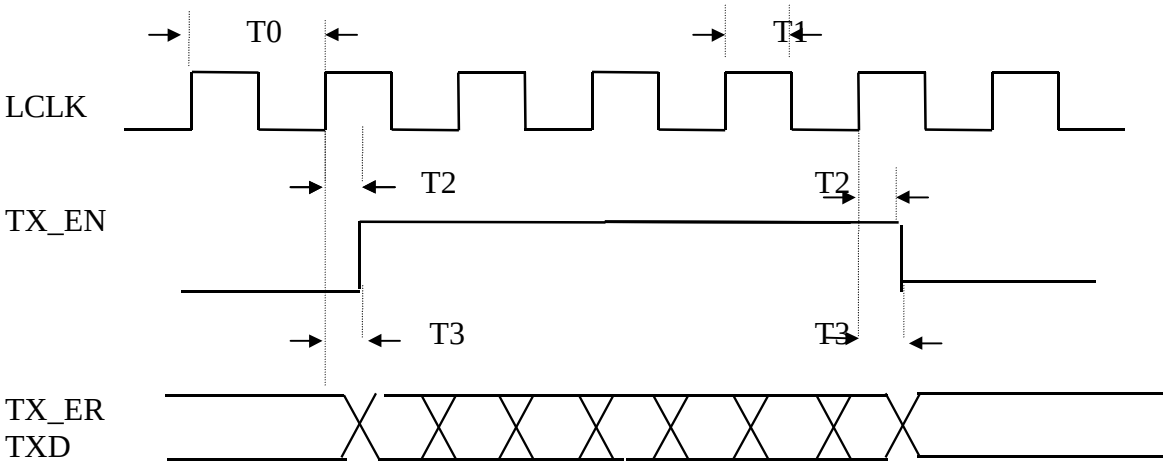
Description	SYM	Min	Tpy	Max	Units
Power Consumption	Pc		180	240	mA

Note :

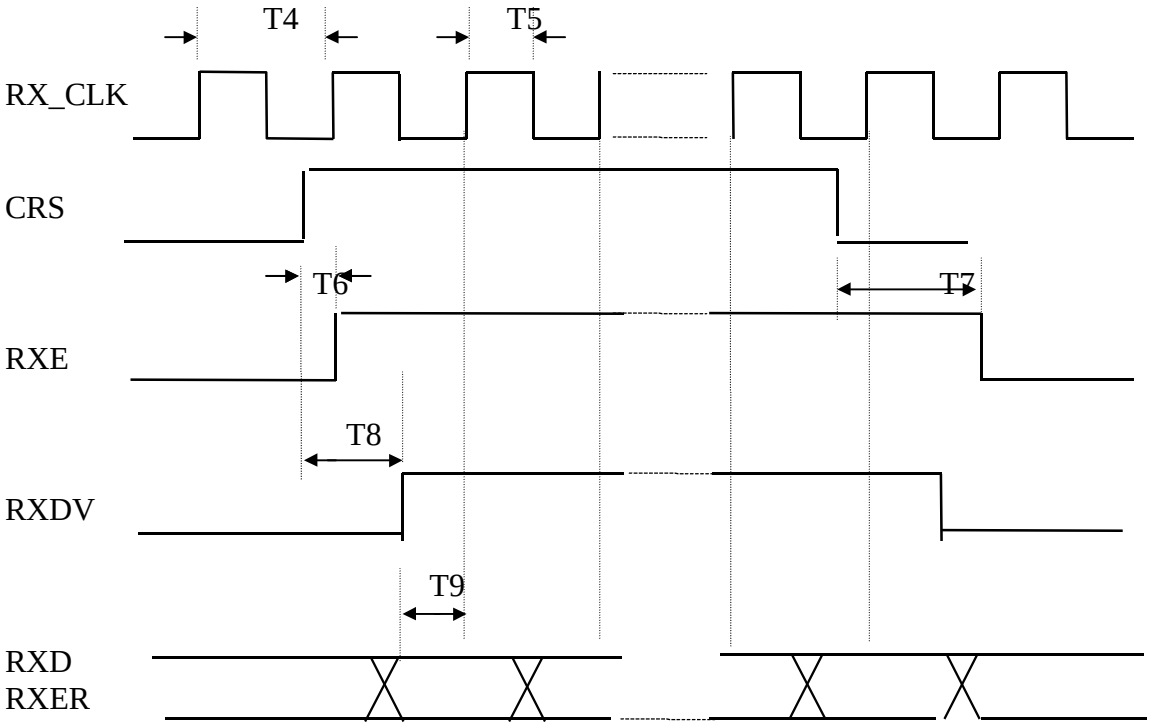
1. All the input pins without pull low or pull high.
2. Those pins had been pull low or pull high.

5.4 AC specifications

5.4.1 MII Interface Timing Tx & Rx

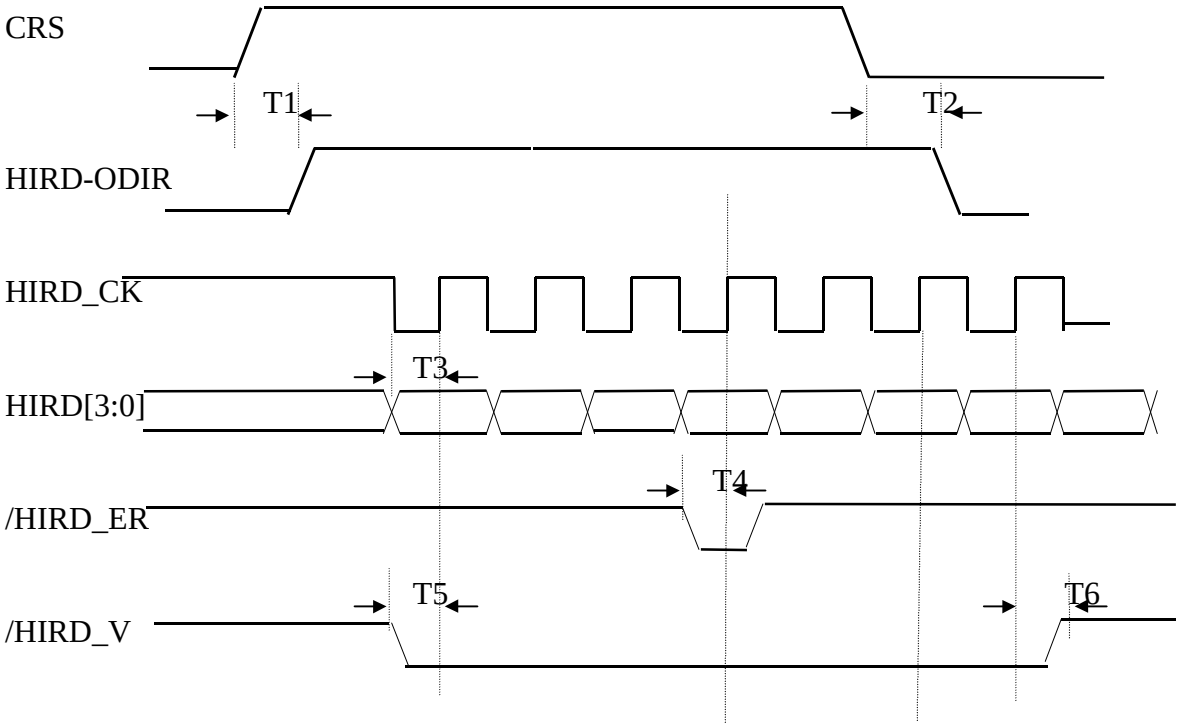


Symbol	Description	Min	Typ.	Max	Units
T0	Local Clock Cycle Time	39.996	40	40.004	ns
T1	Local Clock High Time	14	20	26	ns
T2	TX_EN Delay from LCLK High	7.440		21.760	ns
T3	TX_ER or TXD Delay from LCLK High	3.410		13.320	ns



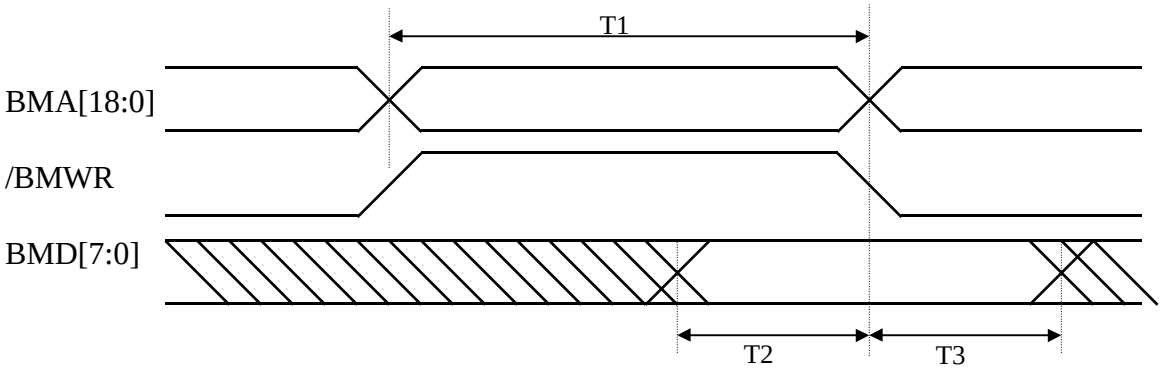
Symbol	Description	Min	Typ.	Max	Units
T4	RX_CLK Clock Cycle Time	39.996	40	40.004	ns
T5	RX_CLK Clock High Time	14	20	26	ns
T6	CRS to RXE Assertion Delay			20	ns
T7	CRS to RXE De-assertion Delay	160		200	ns
T8	CRS to RXDV Delay Requirement	40		160	ns
T9	RXD or RXDV or RX_ER setup to RX_CLK rise time	10		-	ns

5.4.2 Expansion Bus

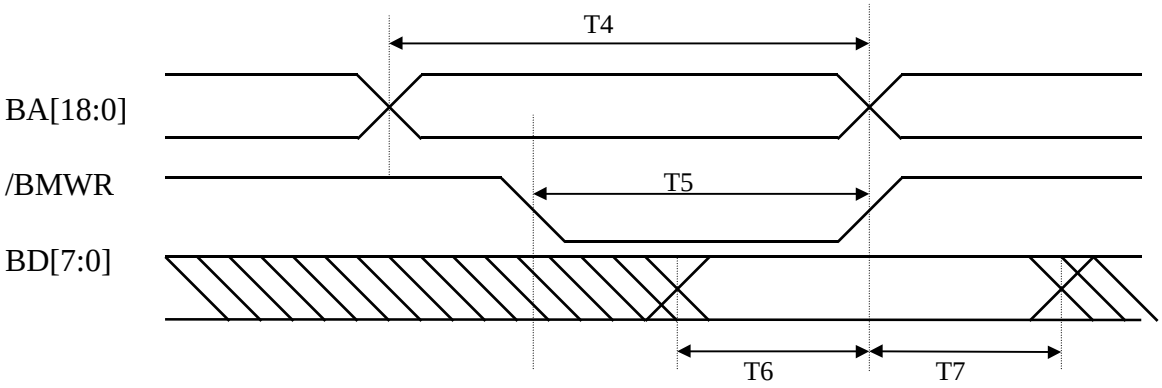


Symbol	Description	Min	Max	Units
T1	CRS Assertion to HIRD-ODIR Assertion	-	20	ns
T2	CRS De-Assertion to HIRD-ODIR De-Assertion	160	200	ns
T3	HIRD[3:0] Setup Time to HIRD-CK High	10	-	ns
T4	/HIRD_ER Setup Time to HIRD-CK High	10	-	ns
T5	/HIRD_V Setup Time to HIRD-CK High	5	-	ns
T6	/HIRD_V Hold Time from HIRD-CK High	5	-	ns

5.4.3 SRAM read cycle and write cycle

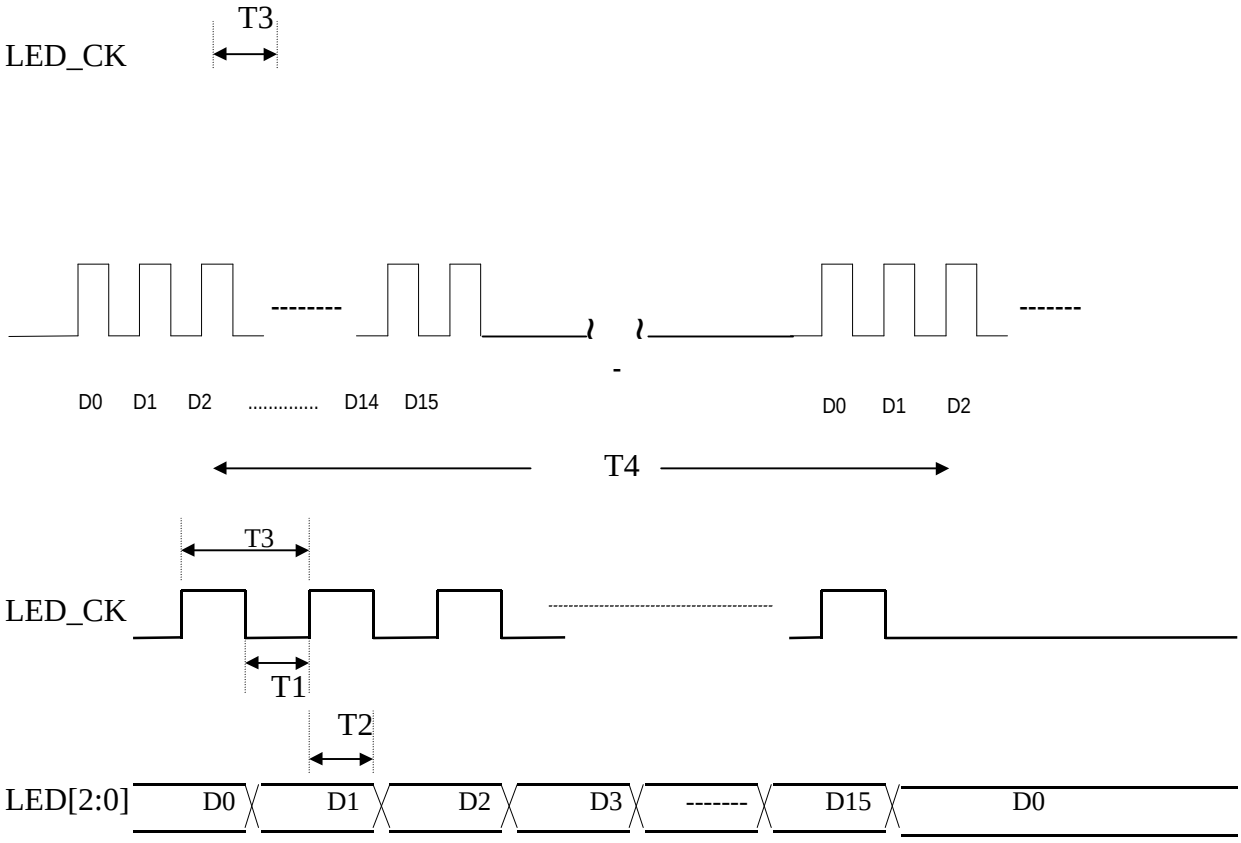


Symbol	Description	Min	Max	Units
T1	Read Cycle Time	40	-	ns
T2	BMD[7:0] Setup Time	3	-	ns
T3	BMD[7:0] Hold Time	3	-	ns



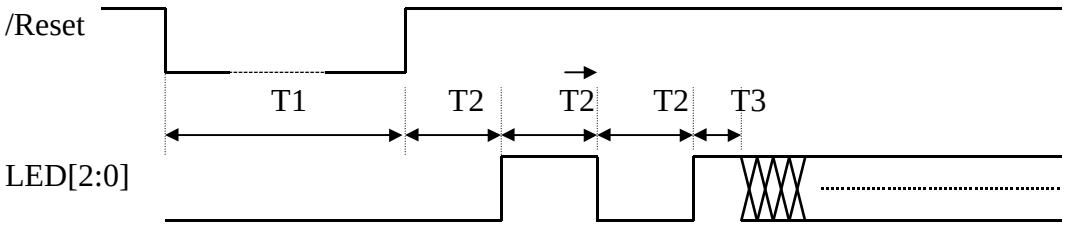
Symbol	Description	Min	Max	Units
T4	Write Cycle Time	38	-	ns
T5	Write Pulse Wtdth	20	-	ns
T6	BMD[7:0] Data Valid to End of Write	14	-	ns
T7	BMD[7:0] Data Hold from End of Write	1		ns

5.4.4 LED DISPLAY



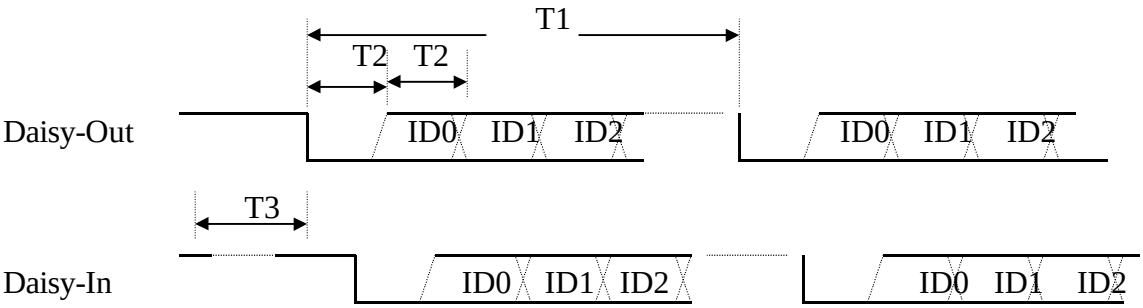
Symbol	Description	Min	Typ.	Max	Units
T1	LED setup to LED_CK High	190		200	ns
T2	LED hold from LED_CK High	200		210	ns
T3	LED_CK Period Width		400		ns
T4	continuous 16 LED_CK Cycle Time		52.4		ms

5.4.5 LED Display After Reset



Symbol	Description	Min	Typ.	Max	Units
T1	Repeater reset time	1000			ns
T2	LED Blink Time After Reset		838.4		ms
T3	LED Dark Time Before Normal Display		419.2		ms

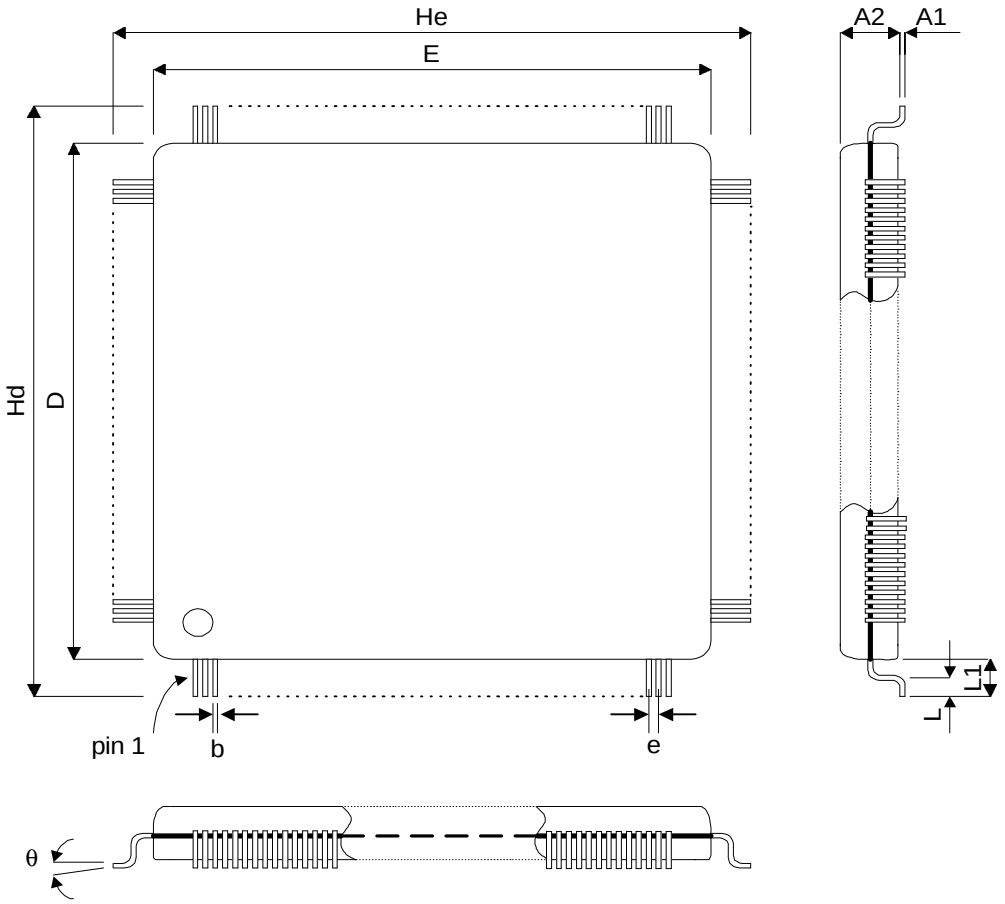
5.4.6 Repeater ID Daisy Chain



Symbol	Description	Min	Typ.	Max	Units
T1	Daisy Chain One Burst period		204.8		us
T2	Start Bit Period or Data Width		12.8		us
T3	Time-out occur when no data present on Daisy_in *		3.8		s

Note : Daisy-Chain Data-In Time-out stands for no input data (always high level) for the specific time.

6.0 PACKAGE INFORMATION



SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.25	0.5
A2	3.17	3.32	3.47
b	0.10	0.20	0.30
D	27.90	28.00	28.10
E	27.90	28.00	28.10
e		0.50	
Hd	30.35	30.60	30.85
He	30.35	30.60	30.85
L	0.45	0.60	0.75
L1		1.30	
θ	0		10

Appendix A: Applications

Two type of applications for AX88871A are illustrated bellow.

A.1 Stand-along 8-ports 10/100Mbps HUB Application

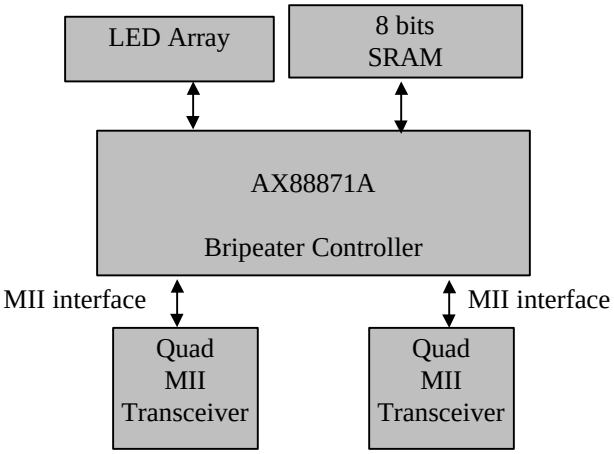


Fig - 6 Stand-along 8-ports 10/100Mbps HUB Application

A.2 Multiple Stand-along HUB Cascade Application (old stack scheme)

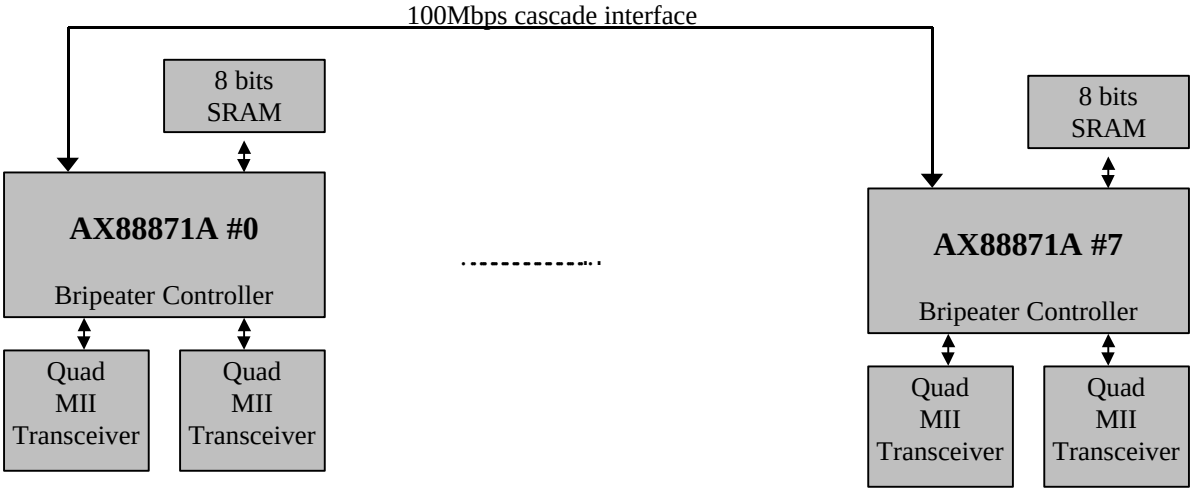


Fig - 7 Multiple Stand-along HUB Cascade Application with old cascade method

A.3 Multiple Stand-along HUB Cascade Application (New stack scheme)

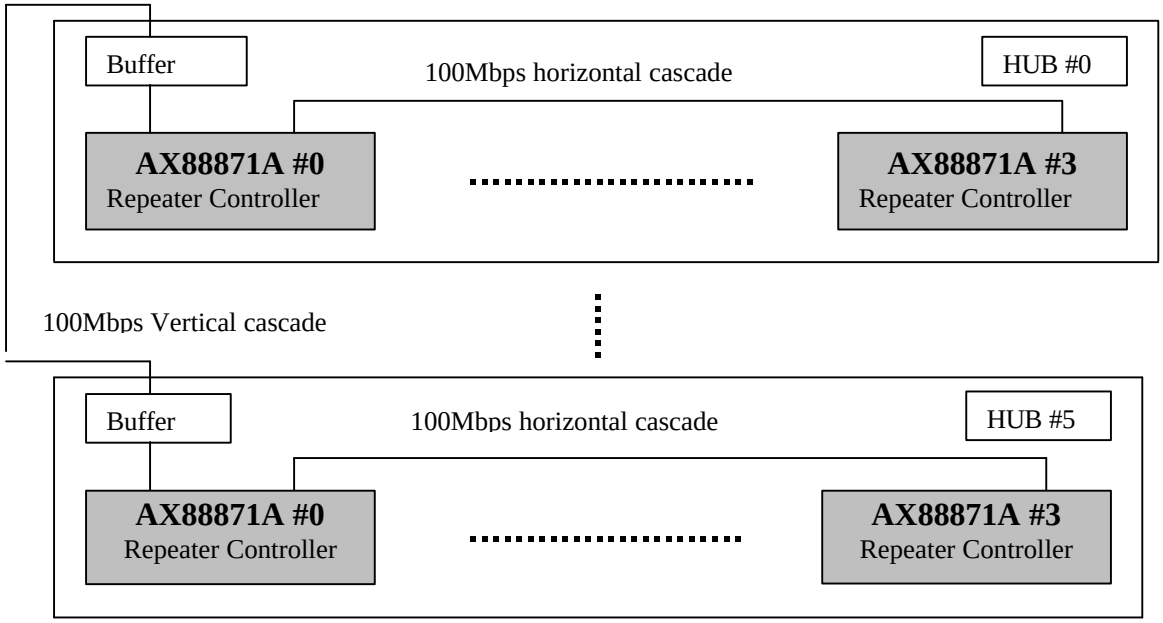
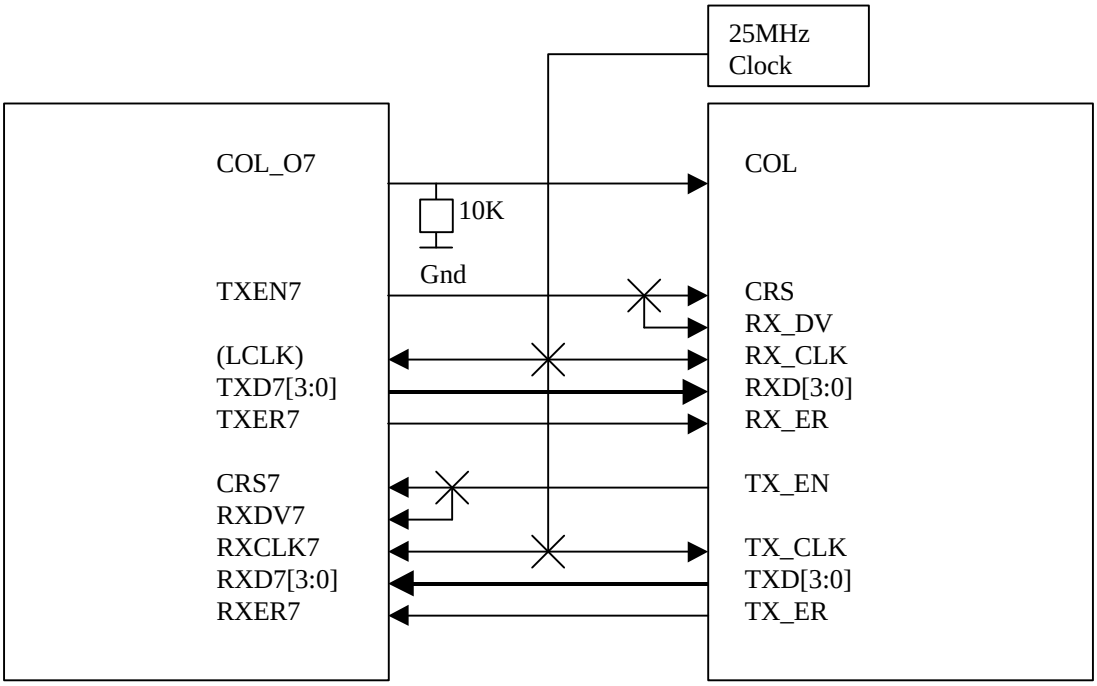


Fig - 8 Multiple Stand-along HUB Cascade Application with new cascade method

Appendix B: Using MII I/F connects to MAC

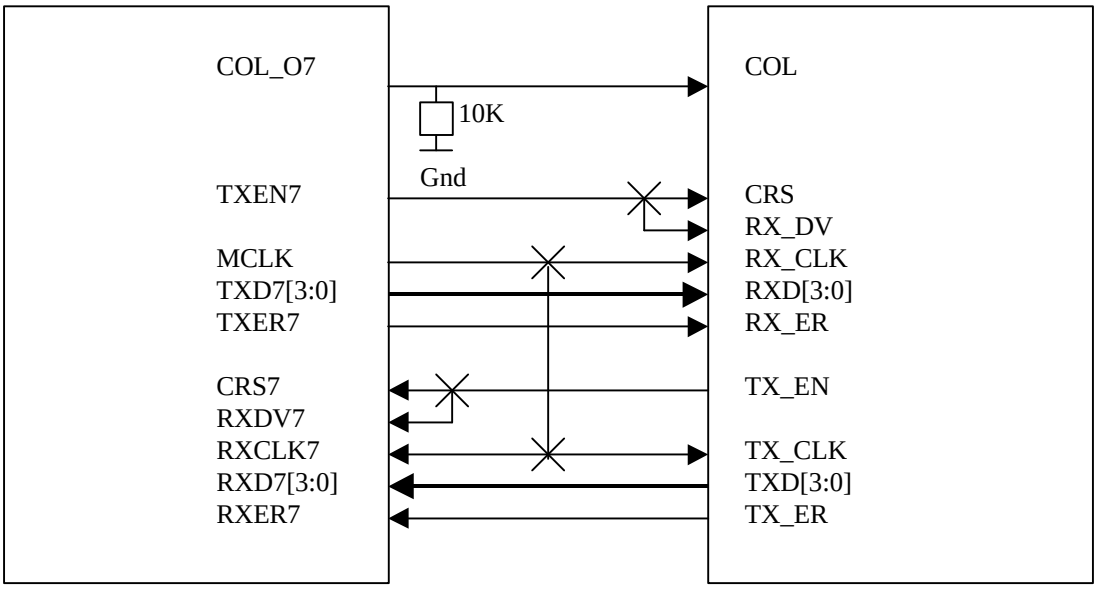
There are two ports of AX88871A can connect to MAC type MII interface. For example, Port 7 is illustrated bellow.



AX88871 / Repeater **AX88195 / MAC**

Note : 1. The MAC needs to run at halfduplex mode.
2. Care must be taken that the receive side has enough setup and/or hold time
3. Some kind of CPU with embbeded MAC can also refer to this example

Using MII interface to connect to 10Mbps MAC device application for AX88871A is illustrated bellow.



AX88871 / Repeater **10Mbps MAC**