



**Flash-ROM Module 8MByte (2Mx32Bit), 72Pin-SO-DIMM, 3.3V
Design**

Part No. HMF2M32B4V

GENERAL DESCRIPTION

The HMF2M32B4V is a high-speed flash read only memory (FROM) module containing 4,194,304 words organized in a x32bit configuration. The module consists of four 1M x 16 FROM mounted on a 72-pin SO-DIMM type, single - sided, FR4-printed circuit board.

Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits. When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single + 3.0V DC power supply and all inputs and outputs are LVTTTL-compatible.

FEATURES

- w Access time: 70, 80, 90, 120ns
- w High-density 8MByte design
- w High-reliability, low-power design
- w Single + 3.0V \pm 0.5V power supply
- w All in/outputs are LVTTTL-compatible
- w FR4-PCB design
- w Minimum 1,000,000 write/erase cycle
- w Sector erases architecture

OPTIONS

- w Timing
 - 70ns access
 - 80ns access
 - 90ns access
 - 120ns access
- w Packages
 - 72-pin SO-DIMM

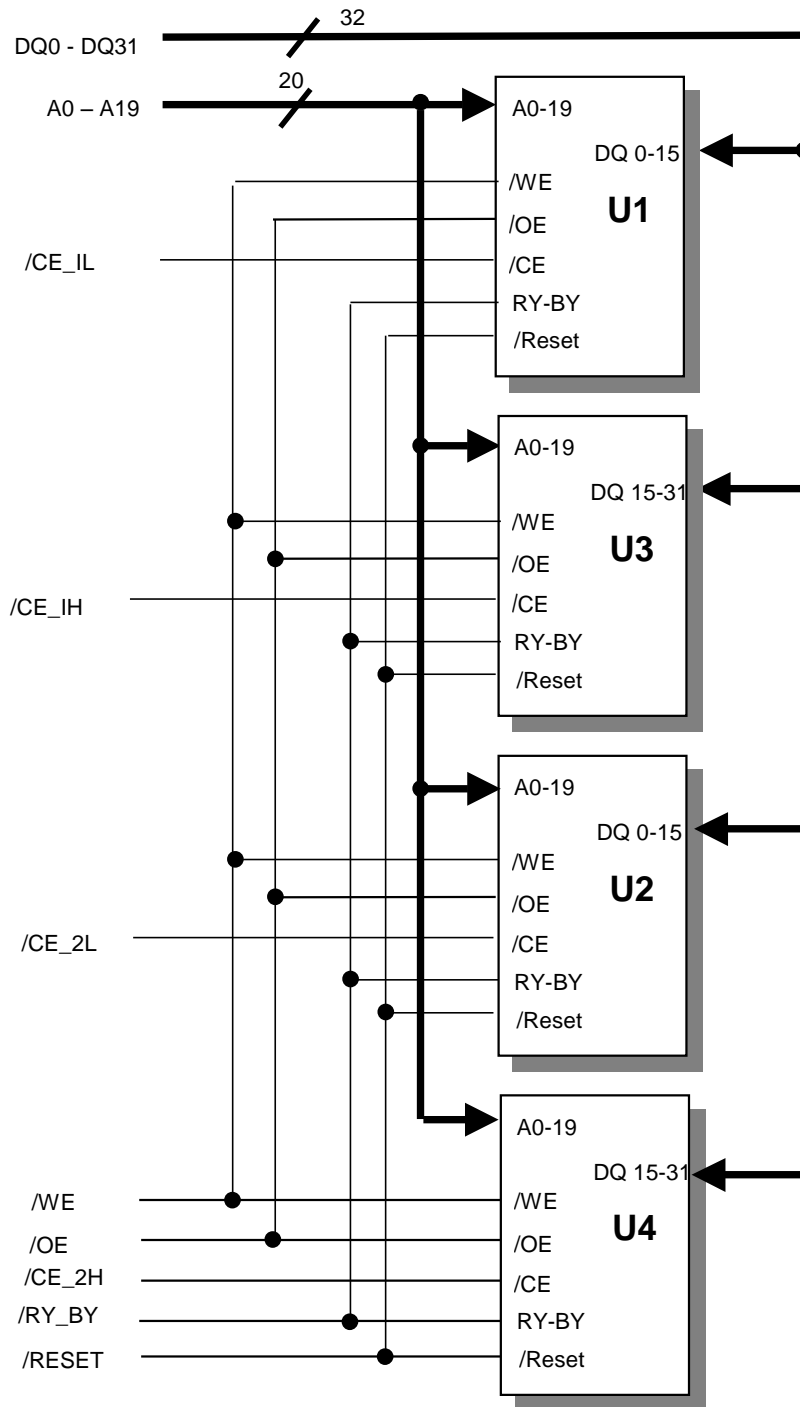
MARKING

- 70
- 80
- 90
- 120
- B

PIN ASSIGNMENT

PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vss	21	DQ15	41	DQ29	61	A8
2	/RESET	22	NC (/CE_4L)	42	DQ30	62	A7
3	DQ0	23	NC (/CE_3H)	43	DQ31	63	A6
4	DQ1	24	DQ16	44	NC	64	A5
5	DQ2	25	DQ17	45	NC (/CE_4H)	65	A4
6	DQ3	26	DQ18	46	NC (/CE_3H)	66	A3
7	DQ4	27	DQ19	47	A19	67	A2
8	DQ5	28	DQ20	48	/OE	68	A1
9	DQ6	29	DQ21	49	/WE	69	A0
10	Vcc	30	Vcc	50	A18	70	A20
11	DQ7	31	DQ22	51	A17	71	NC
12	/CE_1L	32	DQ23	52	A16	72	Vss
13	/CE_2L	33	/CE_1H	53	A15		
14	DQ8	34	/CE_2H	54	A14		
15	DQ9	35	DQ24	55	A13		
16	DQ10	36	DQ25	56	A12		
17	DQ11	37	DQ26	57	A11		
18	DQ12	38	DQ27	58	A10		
19	DQ13	39	Vss	59	Vcc		
20	DQ14	40	DQ28	60	A9		

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	/RESET	DQ (/BYTE=L)	POWER
STANDBY	X	H	X	V _{CC} ±0.3V	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
READ	L	L	H	H	D _{OUT}	ACTIVE
WRITE or ERASE	X	L	L	H	D _{IN}	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	V _{IN,OUT}	-0.5V to V _{CC} +0.5V
Voltage with respect to ground V _{CC}	V _{CC}	-0.5V to +4.0V
Storage Temperature	T _{STG}	-65°C to +150°C
Operating Temperature	T _A	-55°C to +125°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
V _{CC} for ± 10% device Supply Voltages	V _{CC}	2.7V		3.6V
Ground	V _{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS (0°C ≤ T_A ≤ 70 °C)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNIT	
Input Load Current	V _{CC} =V _{CC} max, V _{IN} = GND to V _{CC}	I _{L1}		±1.0	μA	
Output Leakage Current	V _{CC} =V _{CC} max, V _{OUT} = GND to V _{CC}	I _{L0}		±1.0	μA	
Output High Voltage	I _{OH} = -2.0mA, V _{CC} = V _{CC} min	V _{OH}	2.4		V	
Output Low Voltage	I _{OL} = 4.0mA, V _{CC} =V _{CC} min	V _{OL}		0.45	V	
V _{CC} Active Read Current (1)	/CE = V _{IL} , /OE = V _{IH} ,	I _{CC1}	5MHZ	18	32	mA
			1MHZ	4	8	
V _{CC} Active Write Current (2)	/CE = V _{IL} , /OE=V _{IH}	I _{CC2}	40	60	mA	
V _{CC} Standby Current	/CE, /RESET=V _{CC} ±0.3V	I _{CC3}		60	mA	
Low V _{CC} Lock-Out Voltage		V _{LKO}	2.3	2.5	V	

- Notes:
1. The I_{CC} current listed is typically less than 2mA/MHz, with /OE at V_{IH}.
 2. I_{CC} active while embedded algorithm (program or erase) is in progress
 3. Maximum I_{CC} current specifications are tested with V_{CC}=V_{CC} max

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		25		sec	
Byte Programming Time	-	9	300	μs	Excludes system-level overhead
Chip Programming Time	-	18	54	sec	

TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0	6	7.5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	8.5	12	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	7.5	9	pF

Notes : Test conditions T_A = 25° C, f=1.0 MHz.

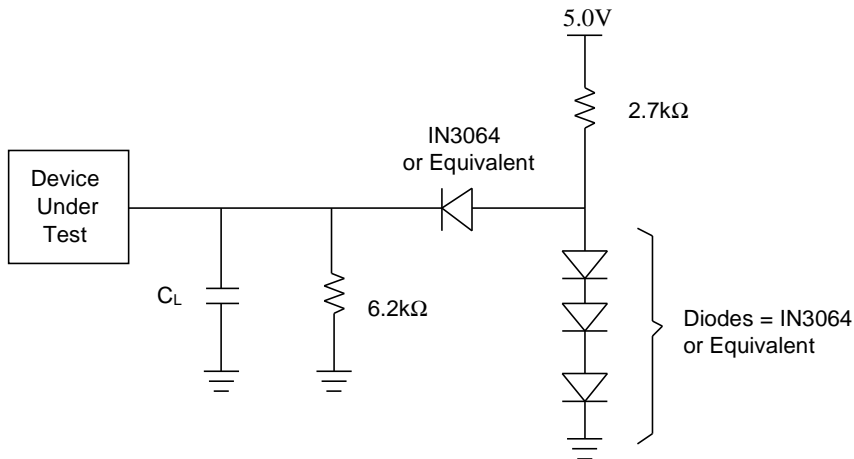
AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP	Speed Options				UNIT
JEDEC	STANDARD			-70R	-80	-90	-120	
t _{AVAV}	t _{RC}	Read Cycle Time	Min	70	80	90	120	ns
t _{AVQV}	t _{ACC}	Address to Output Delay	/CE = V _{IL} /OE = V _{IL} Max	70	80	90	120	ns
t _{ELQV}	t _{CE}	Chip Enable to Output Delay	/OE = V _{IL} Max	70	80	90	120	ns
t _{GLQV}	t _{OE}	Chip Enable to Output Delay	Max	30	30	35	35	ns
t _{EHQZ}	t _{DF}	Chip Enable to Output High-Z	Max	25	25	30	30	ns
t _{GHQZ}	t _{DF}	Output Enable to Output High-Z	Max	25	25	30	30	ns
t _{AXQX}	t _{QH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First	Min	0				ns

TEST SPECIFICATIONS

TEST CONDITION	70R, 80	90, 120	UNIT
Output load	1TTL gate		
Output load capacitance, C _L (Including jig capacitance)	30	100	pF
Input rise and full times	5		ns
Input pulse levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V



Note : $C_L = 100\text{pF}$ including jig capacitance

u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION	Speed Options				UNIT	
JEDEC	STANDARD		70R	80	90	120		
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	80	90	12	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0				ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	9				μs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	0.7				sec
	t_{VCS}	Vcc set up time	Min	50				μs

- Notes :
- 1 . This does not include the preprogramming time
 - 2 . This timing is only for Sector Protect operations

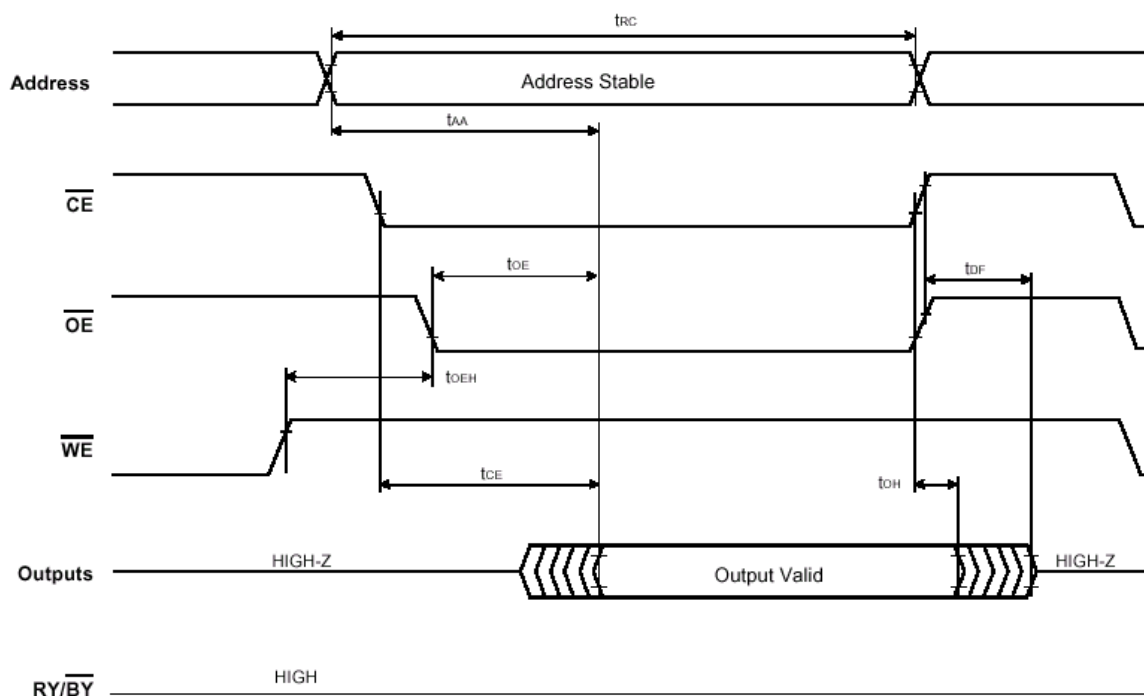
Eraser/Program Operations

Alternate /CE Controlled Writes

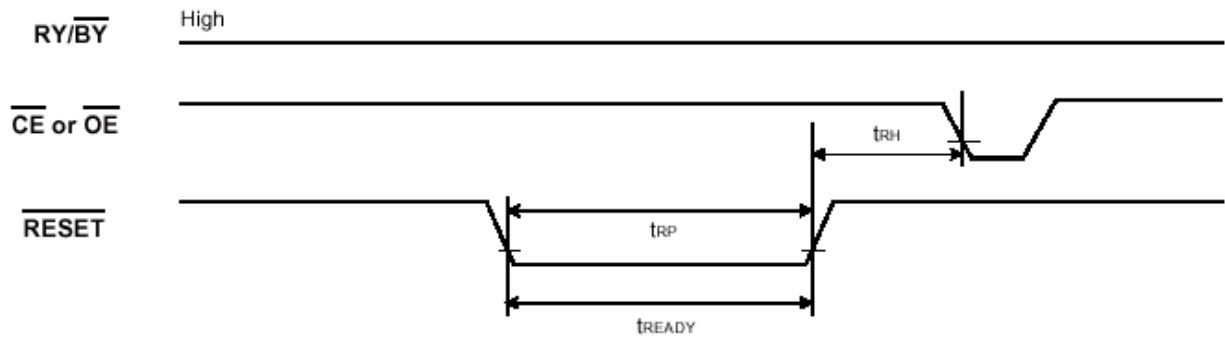
PARAMETER SYMBOLS		DESCRIPTION		Speed Options				UNIT
JEDEC	STANDARD			-70R	-80	-90	120	
t _{AVAV}	t _{WC}	Write Cycle Time	Min	70	80	90	12	ns
t _{AVWL}	t _{AS}	Address Setup Time	Min	0				ns
t _{WLAX}	t _{AH}	Address Hold Time	Min	45	45	45	50	ns
t _{DVWH}	t _{DS}	Data Setup Time	Min	35	35	45	50	ns
t _{WHDX}	t _{DH}	Data Hold Time	Min	0				ns
	t _{oES}	Output Enable Setup Time	Min	0				ns
t _{GHWL}	t _{GHWL}	Read Recover Time Before Write	Min	0				ns
t _{ELWL}	t _{CS}	/CE Setup Time	Min	0				ns
t _{WHEH}	t _{CH}	/CE Hold Time	Min	0				ns
t _{WLWH}	t _{WP}	Write Pulse Width	Min	35	35	35	50	ns
t _{WHWL}	t _{WPH}	Write Pulse Width High	Min	30				ns
t _{WHWH1}	t _{WHWH1}	Byte Programming Operation	Typ	9				μs
t _{WHWH2}	t _{WHWH2}	Sector Erase Operation (Note1)	Typ	0.7				sec

- Notes :
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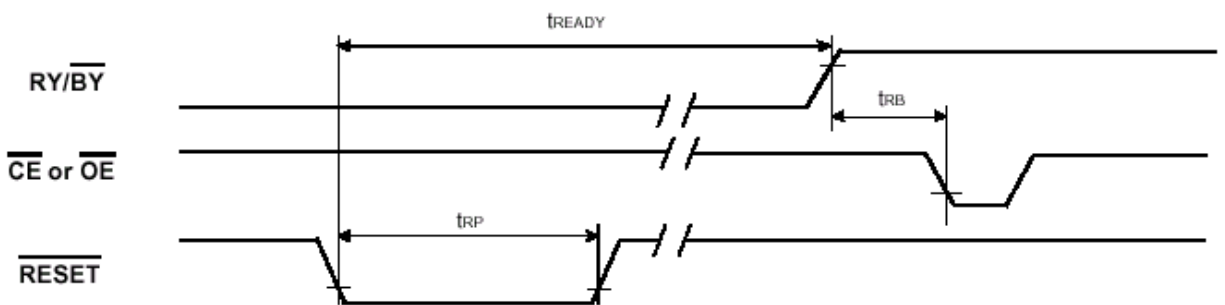
READ OPERATIONS TIMING



RESET TIMING



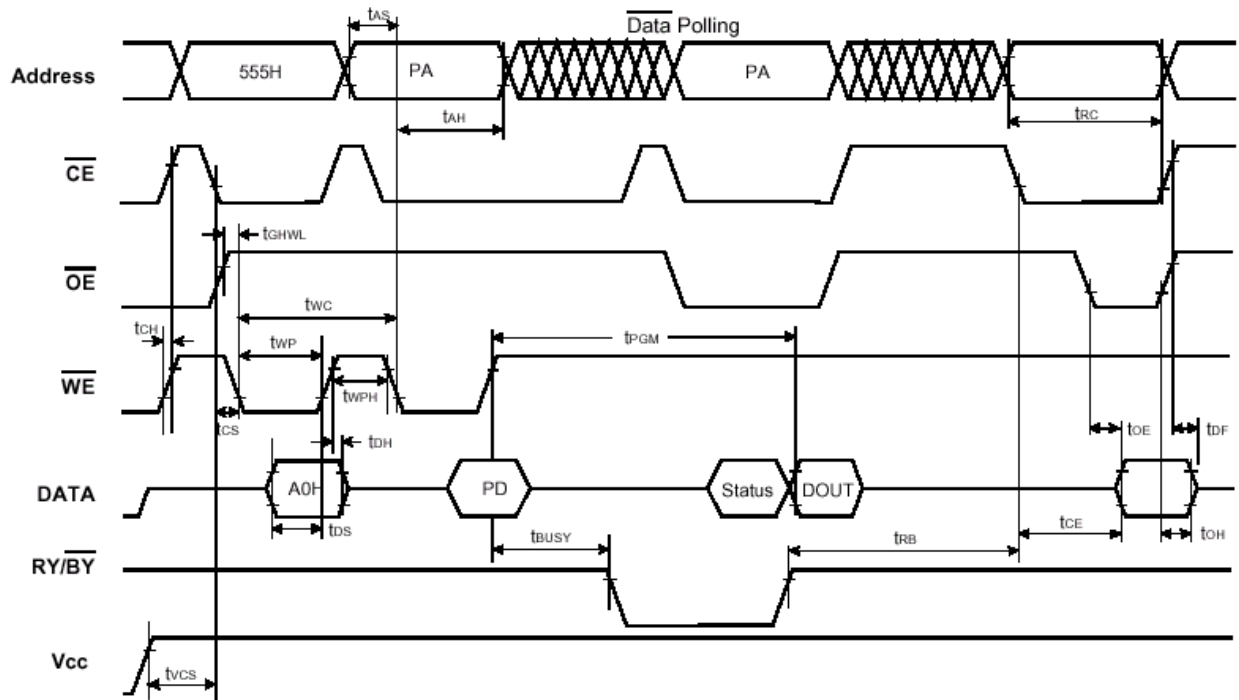
Reset Timings NOT during Internal Routine



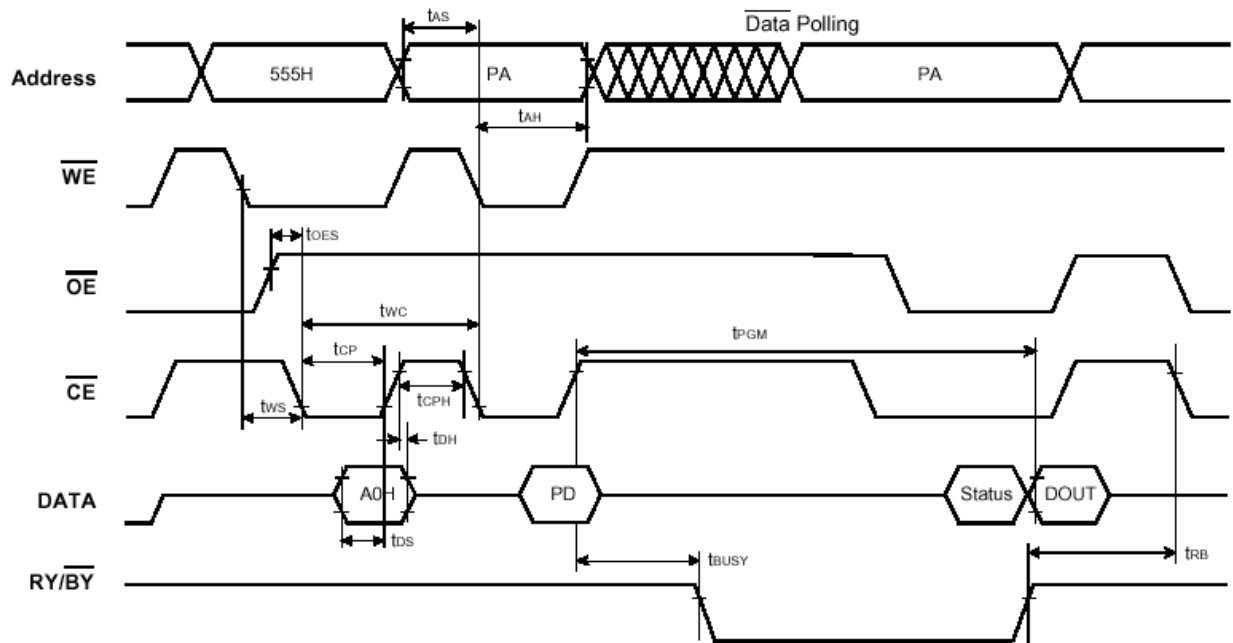
Reset Timings during Internal Routine

PROGRAM OPERATIONS TIMING

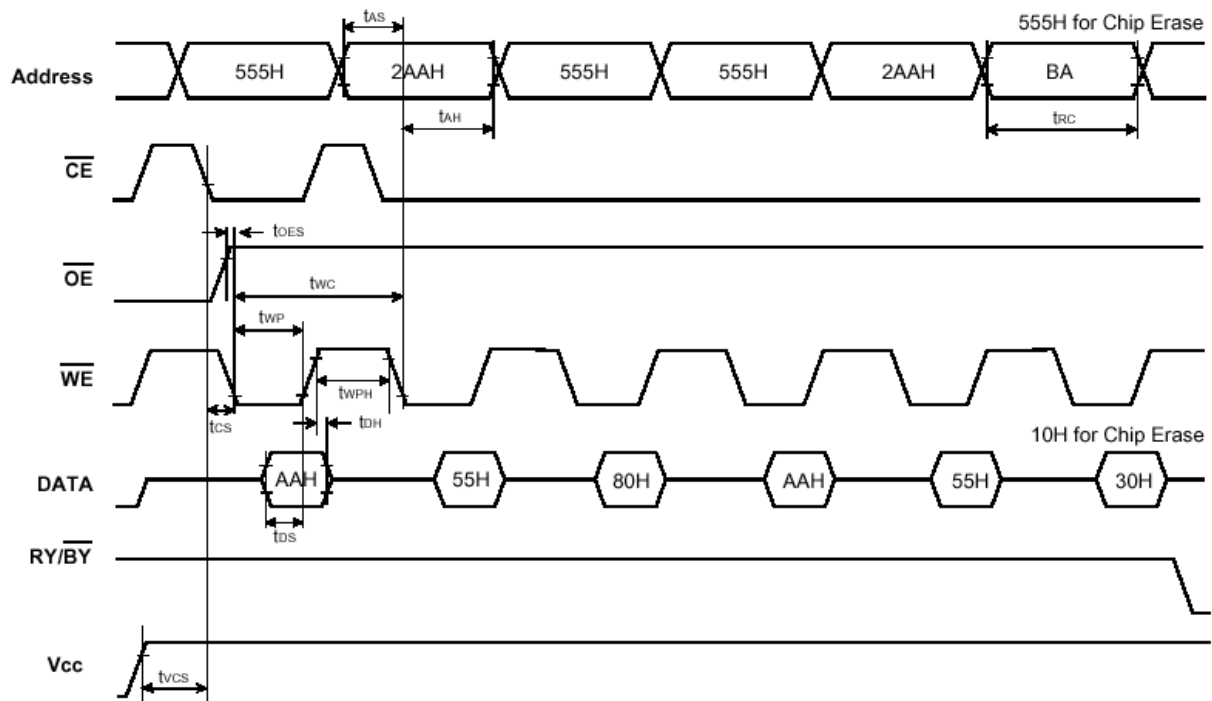
Alternate /WE Controlled Writes



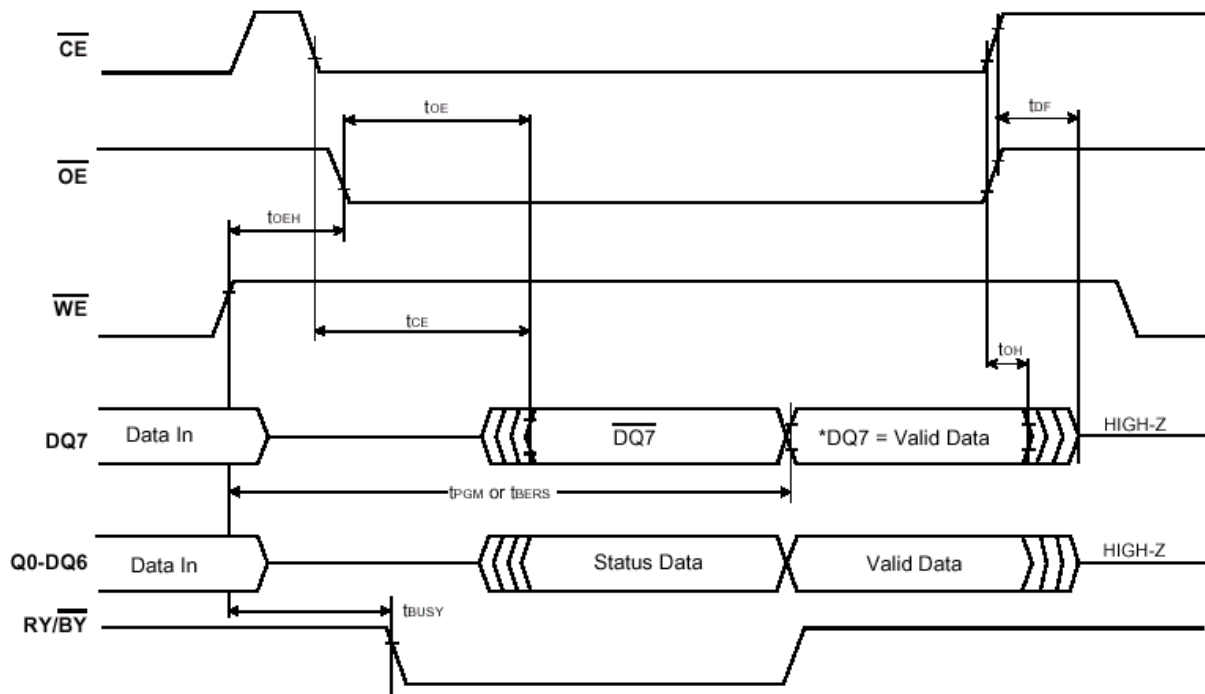
Alternate /CE Controlled Writes



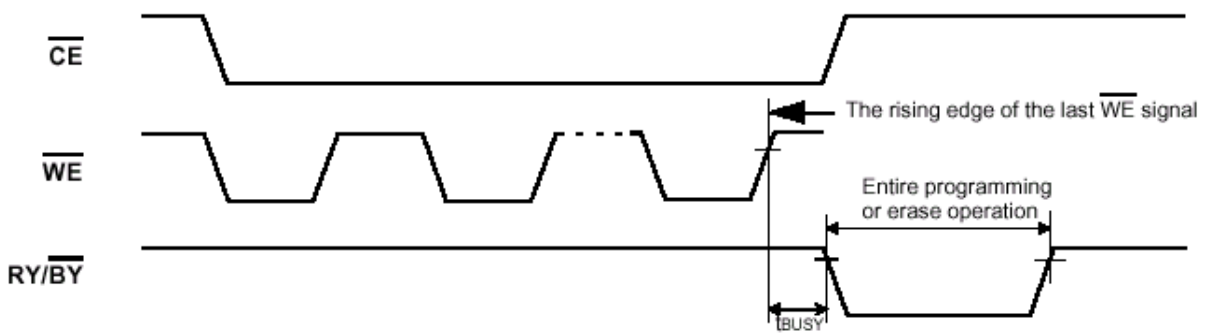
CHIP/BLOCK ERASE OPERATION TIMINGS



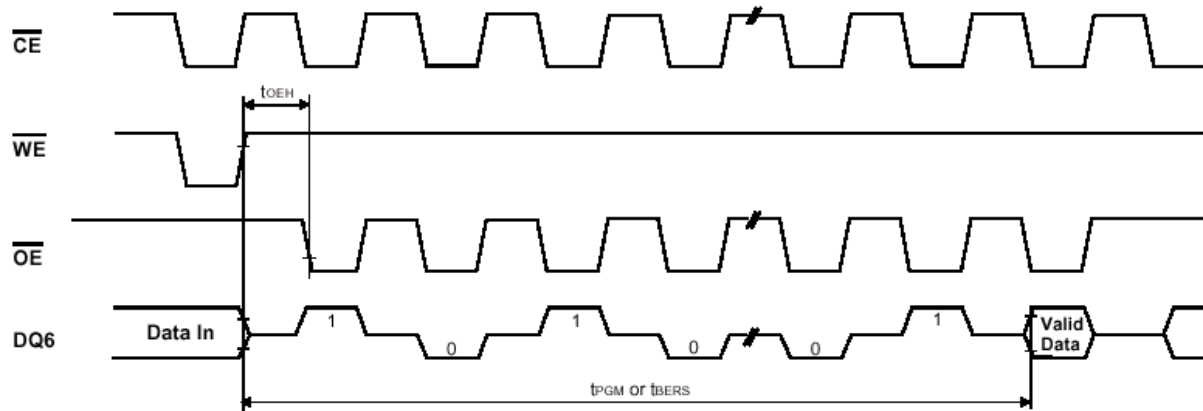
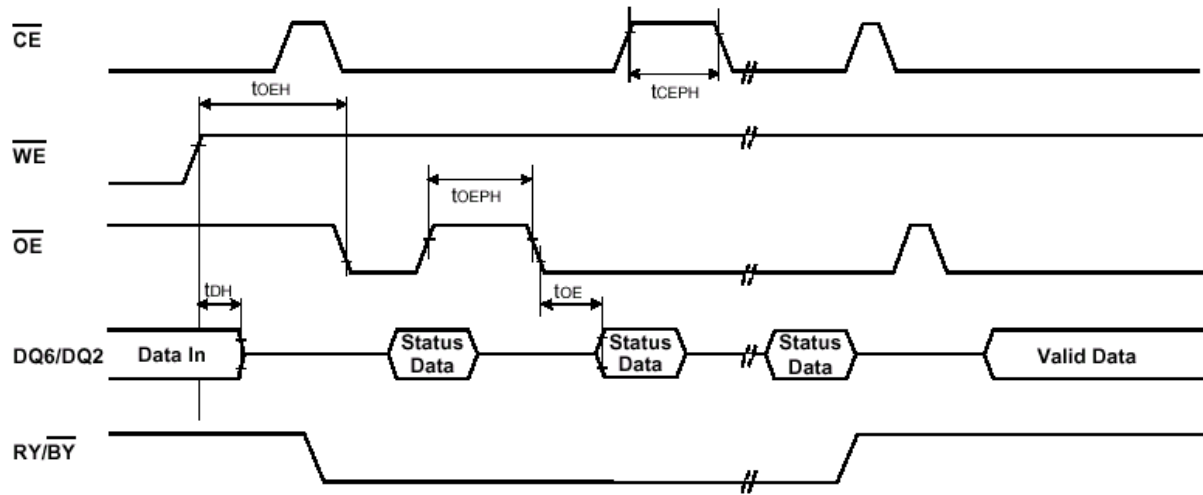
DATA# POLLING TIMES DURING INTERNAL ROUTINE OPERATION



RY_/BY TIMEING DURING ERASE / PROGRAM OPERATION

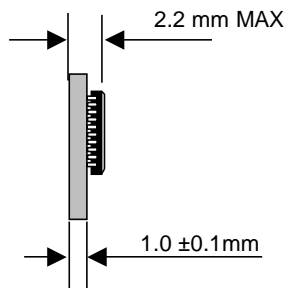
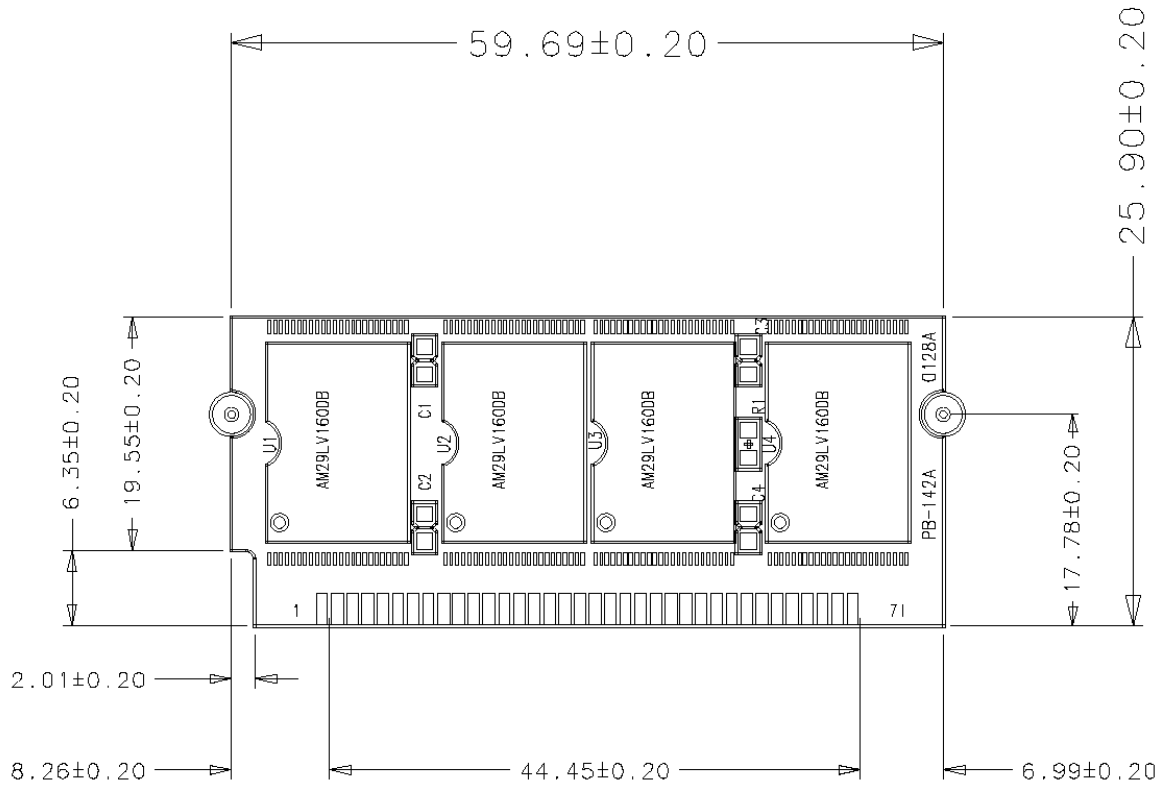


U TOGGLE# BIT DURING INTERNAL ROUTINE OPERATION



PACKAGE DIMENSIONS

<TOP VIEW>



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF2M32B4V-70	8MByte	2Mx 32	72Pin –SODIMM	4EA	3.3V	70ns
HMF2M32B4V-80	8MByte	2Mx 32	72Pin –SODIMM	4EA	3.3V	80ns
HMF2M32B4V-90	8MByte	2Mx 32	72Pin –SODIMM	4EA	3.3V	90ns
HMF2M32B4V-120	8MByte	2Mx 32	72Pin –SODIMM	4EA	3.3V	120ns