HD74AC112/HD74ACT112

Dual JK Negative Edge-Triggered Flip-Flop

HITACHI

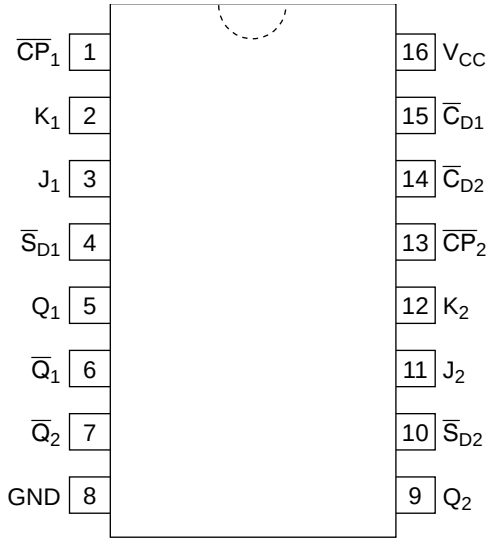
Description

The HD74AC112/HD74ACT112 features individual J, K, Clock and asynchronous Set and Clear inputs to each flip-flop. When the clock goes High, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may change when the clock is High and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Features

- Outputs Source/Sink 24 mA
- HD74ACT112 has TTL-Compatible Inputs

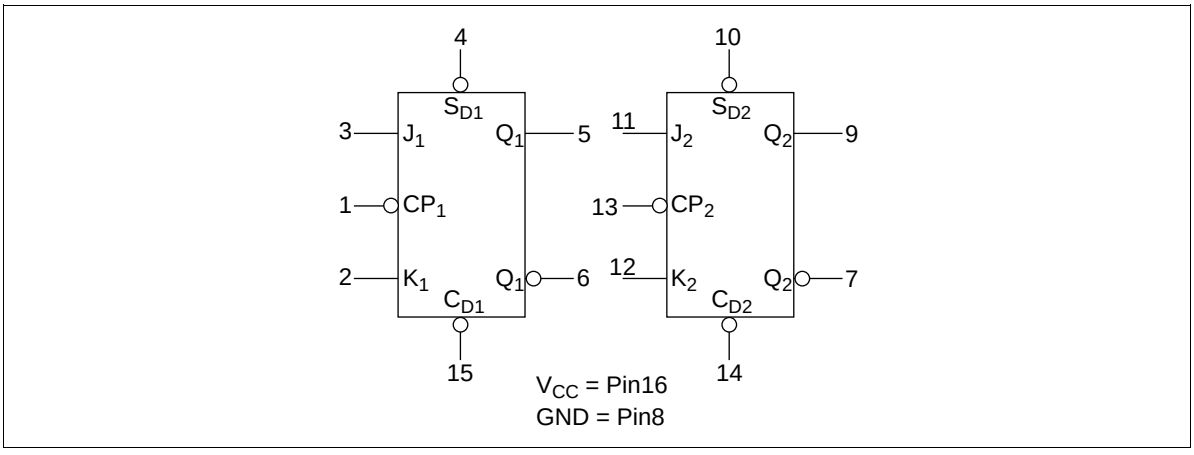
Pin Arrangement



(Top view)

Hitachi semiconductor

Logic Symbol



Pin Names

J_1, J_2, K_1, K_2	Data Inputs
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active Low)
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active Low)
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

Asynchronous Inputs:

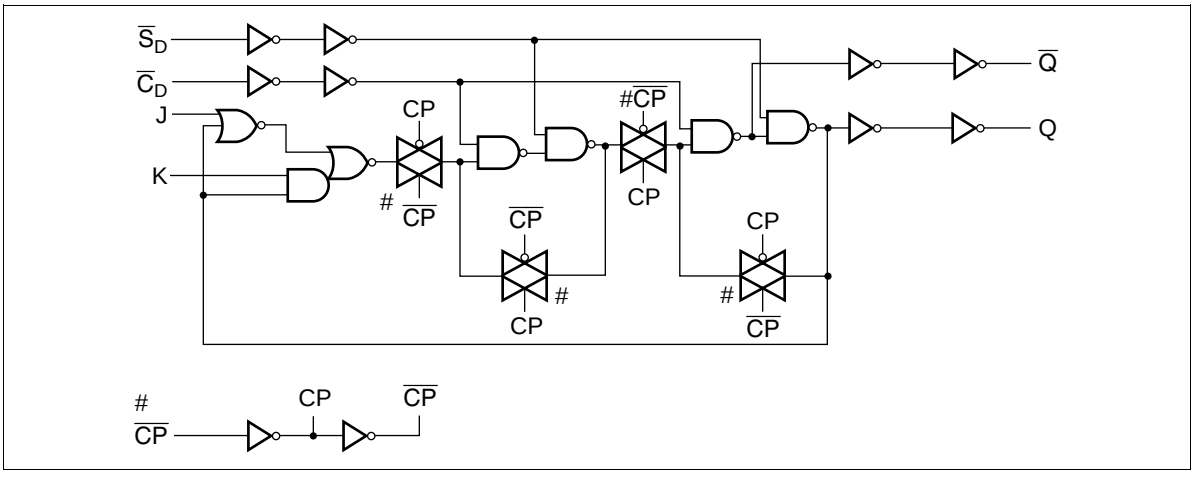
Low input to $\overline{S}_D$ sets Q to High level
Low input to $\overline{C}_D$ sets Q to Low level
Clear and Set are independent of clock
Simultaneous Low on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ High

Truth Table

Inputs		Outputs
$@t_n$		$@t_{n+1}$
J	**K**	**Q**
L	L	Qn
L	H	L
H	L	H
H	H	Qn

t_n : Bit time before clock pulse.
t_{n+1} : Bit time after clock pulse.
H : High Voltage Level
L : Low Voltage Level

Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	µA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5$ V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	8.0	µA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5$ V, Ta = 25°C
Maximum additional I_{CC}/input (HD74ACT112)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} – 2.1$ V, $V_{CC} = 5.5$ V Ta = Worst case

AC Characteristics: HD74AC112

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF Min	Typ	Max	Ta = –40°C to +85°C C_L = 50 pF Min	Max	Unit
Maximum clock	f_{max}	3.3	125	—	—	100	—	MHz
frequency		5.0	150	—	—	125	—	
Propagation delay	t_{PLH}	3.3	1.0	11.0	14.0	1.0	15.0	ns
$\overline{C}_P$ to Q or $\overline{Q}$		5.0	1.0	8.5	11.0	1.0	12.0	
Propagation delay	t_{PHL}	3.3	1.0	11.0	14.0	1.0	15.0	
$\overline{C}_P$ to Q or $\overline{Q}$		5.0	1.0	8.5	11.0	1.0	12.0	
Propagation delay	t_{PLH}	3.3	1.0	9.5	12.5	1.0	13.5	
$\overline{C}_D$, $\overline{S}_D$ to Q or $\overline{Q}$		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay	t_{PHL}	3.3	1.0	11.5	14.5	1.0	15.5	
$\overline{C}_D$, $\overline{S}_D$ to Q or $\overline{Q}$		5.0	1.0	9.0	11.0	1.0	12.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC112

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF Typ	Guaranteed Minimum	Ta = –40°C to +85°C C_L = 50 pF	Unit
Setup time	t_{su}	3.3	3.0	5.5	6.0	ns
J or K to $\overline{C}_P$		5.0	2.0	4.5	4.6	
Hold time	t_h	3.3	–1.5	0.0	0.0	
$\overline{C}_P$ to J or K		5.0	–0.5	0.0	0.0	
Pulse width	t_w	3.3	2.0	5.5	7.0	
$\overline{C}_P$ or $\overline{C}_D$ or $\overline{S}_D$		5.0	2.0	4.5	5.0	
Recovery time	t_{rec}	3.3	–1.0	3.5	3.5	
$\overline{C}_D$ or $\overline{S}_D$ to $\overline{C}_P$		5.0	–1.0	3.0	3.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT112

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF Min	Typ	Max	Ta = –40°C to +85°C C_L = 50 pF Min	Max	Unit
Maximum clock frequency	f_{max}	5.0	100	—	—	80	—	MHz
Propagation delay $\overline{C}_P$ to Q or $\overline{Q}$	t_{PLH}	5.0	1.0	10.5	13.0	1.0	14.0	ns
Propagation delay $\overline{C}_P$ to Q or $\overline{Q}$	t_{PHL}	5.0	1.0	10.5	13.0	1.0	14.0	
Propagation delay $\overline{C}_D$, $\overline{S}_D$ to Q or $\overline{Q}$	t_{PLH}	5.0	1.0	8.0	10.0	1.0	11.0	
Propagation delay $\overline{C}_D$, $\overline{S}_D$ to Q or $\overline{Q}$	t_{PHL}	5.0	1.0	10.5	12.5	1.0	13.5	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT112

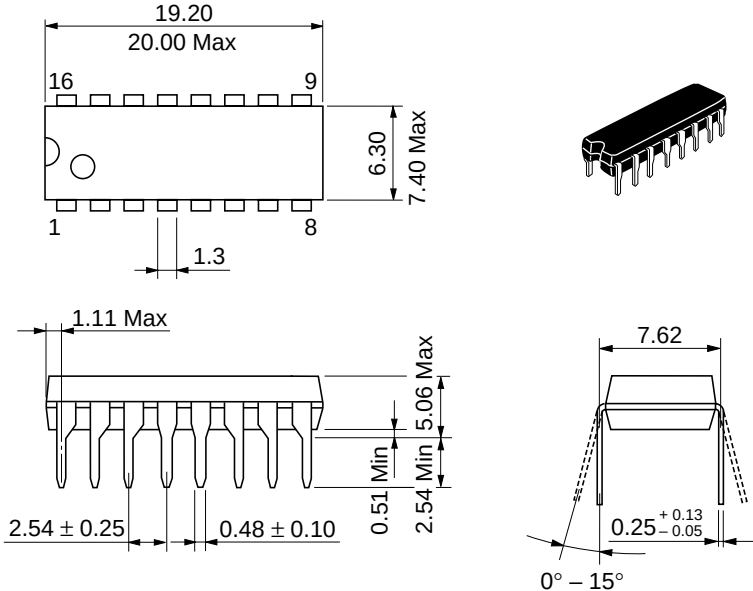
Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF Typ	Ta = –40°C to +85°C C_L = 50 pF Guaranteed Minimum		Unit
Setup time J or K to $\overline{C}_P$	t_{su}	5.0	2.5	7.0	8.0	ns
Hold time $\overline{C}_P$ to J or K	t_h	5.0	0.0	1.5	1.5	
Pulse width $\overline{C}_P$ or $\overline{C}_D$ or $\overline{S}_D$	t_w	5.0	4.5	7.0	8.0	
Recovery time $\overline{C}_D$, $\overline{S}_D$ to $\overline{C}_P$	t_{rec}	5.0	–2.5	3.0	3.0	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

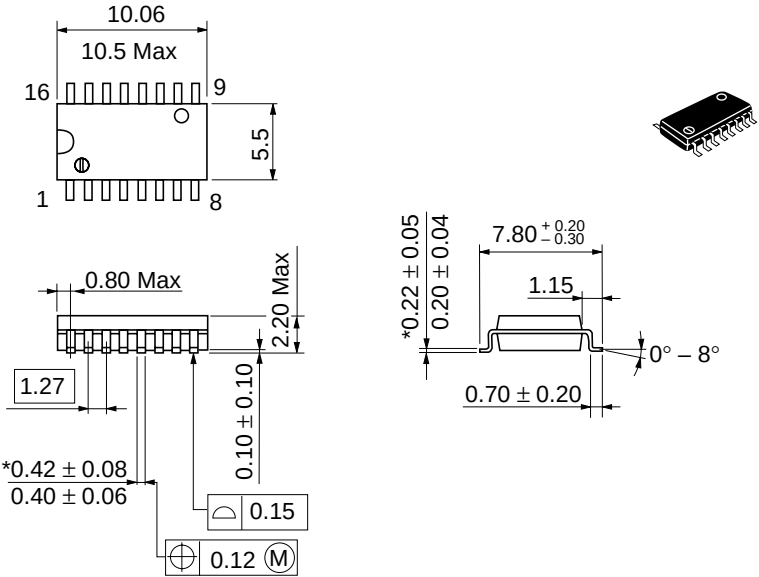
Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	35.0	pF	V_{CC} = 5.0 V

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

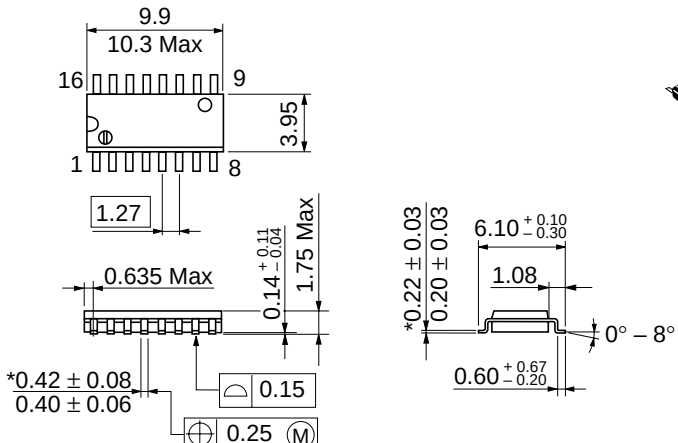
Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

*Dimension including the plating thickness / Base material dimension

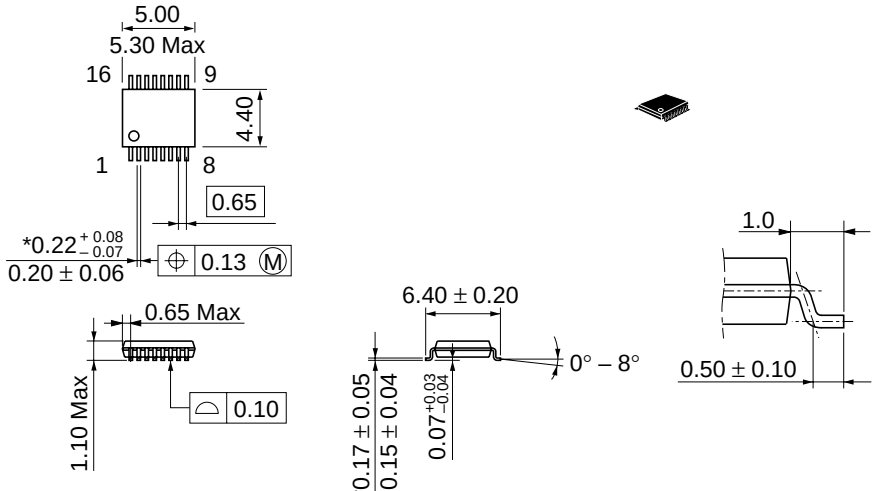
Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness / Base material dimension

Unit: mm



Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

*Dimension including the plating thickness / Base material dimension

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