Synchronous DRAM Module 128Mbyte (32M x 32-Bit) 72-Pin SIMM based on 32Mx8, 4Banks, 8K Ref., 3.3V Part No. HSD32M32M4V

GENERAL DESCRIPTION

The HSD32M32M4V is a 32M x 32 bit Synchronous Dynamic RAM high density memory module. The module consists of four CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II packages mounted on a 72-pin, FR-4-printed circuit board. Two 0.01uF decoupling capacitor is mounted on the printed circuit board in parallel for each SDRAM. The HSD32M32M4V is a SIMM designed. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications All module components may be powered from a single 3.3V DC power supply and all inputs and outputs are LVTTL-compatible.

FEATURES

• Part Identification
  HSD32M32M4V-13/F13 :133MHz (CL=3)
  HSD32M32M4V-12/F12: 125MHz (CL=3)
  HSD32M32M4V-10/F10: 100MHz (CL=2)
  HSD32M32M4V-10L/F10L: 100MHz
  F means Auto & Self refresh with Low –Power (3.3V)

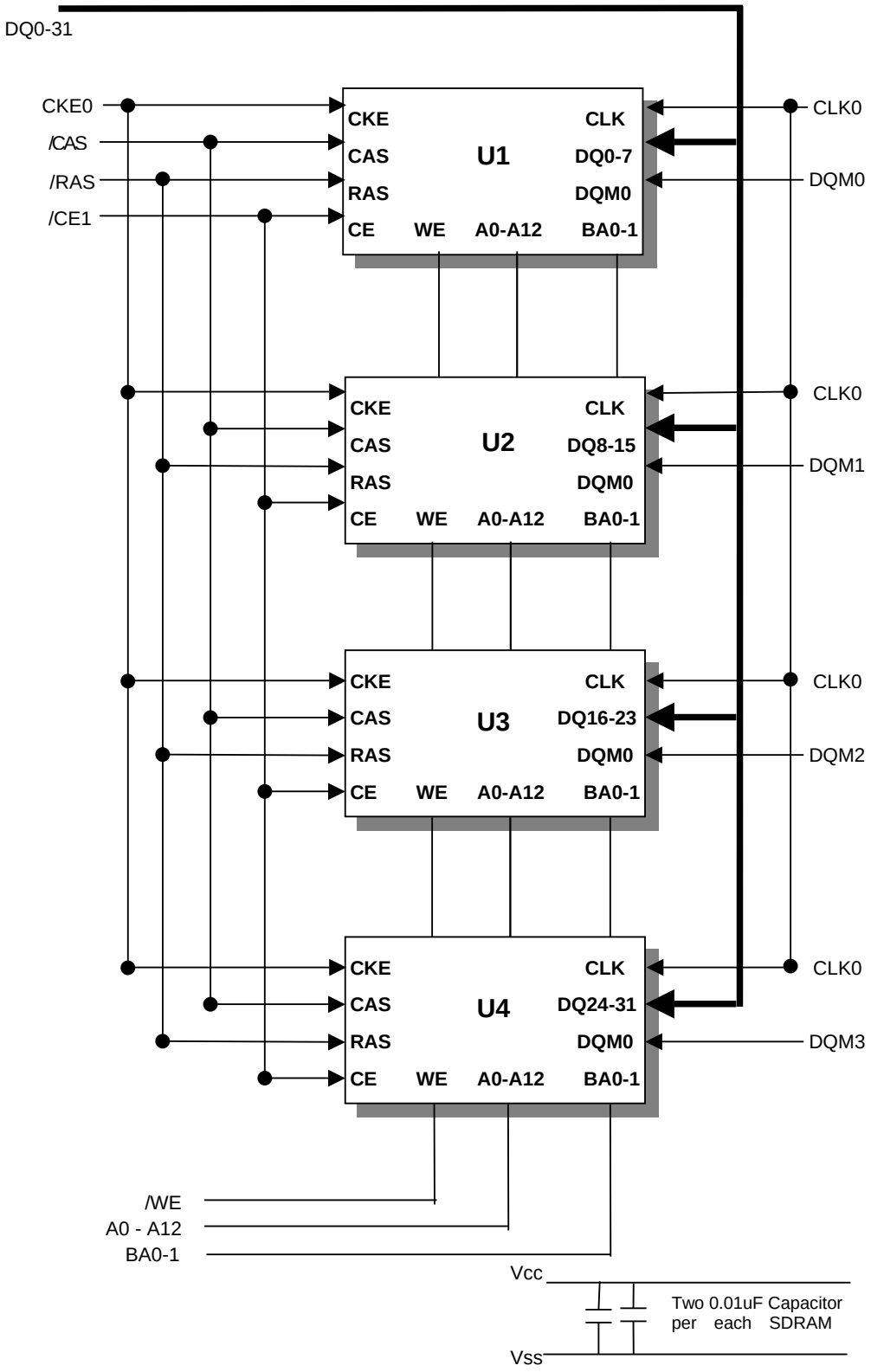
• Burst mode operation
• Auto & self refresh capability (8192 Cycles/64ms)
• LVTTL compatible inputs and outputs
• Single 3.3V ±0.3V power supply
• MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
• All inputs are sampled at the positive going edge of the system clock
• FR4-PCB design
• 72-Pin SIMM Package
• The used device is 8Mx8bitx4Bank SRAM
• Pin assignment is compatible with
  - HSD8M32M4V
  - HSD16M32M4V

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	DQ14	49	A5
2	DQ0	26	DQ15	50	A6
3	DQ1	27	DQM1	51	A7
4	DQ2	28	NC	52	A8
5	DQ3	29	/WE	53	A9
6	DQ4	30	/CAS	54	DQ24
7	DQ5	31	Vcc	55	DQ25
8	DQ6	32	/RAS	56	DQ26
9	DQ7	33	/CS0	57	DQ27
10	DQM0	34	NC	58	DQ28
11	Vcc	35	NC	59	DQ29
12	NC	36	CLK0	60	DQ30
13	A0	37	CKE0	61	DQ31
14	A1	38	Vss	62	DQM3
15	A2	39	DQ16	63	NC
16	A3	40	DQ17	64	A10/AP
17	A4	41	DQ18	65	A11
18	Vss	42	DQ19	66	A12
19	DQ8	43	DQ20	67	Vcc
20	DQ9	44	DQ21	68	BA0
21	DQ10	45	DQ22	69	BA1
22	DQ11	46	DQ23	70	NC
23	DQ12	47	DQM2	71	NC
24	DQ13	48	Vcc	72	Vss

72-PIN SIMM TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
/CE	Chip enable	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
/WE	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 3	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 31	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-1V to 4.6V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 4.6V
Power Dissipation	P_D	4W
Storage Temperature	T_{STG}	$-55^{o}C$ to $150^{o}C$
Short Circuit Output Current	I_{OS}	50mA

Notes :
Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to VSS = 0V, TA = 0 to 70°C))

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Supply Voltage	Vcc	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	Vcc+0.3	V	1
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	2
Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes :

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(VCC = 3.3V, TA = 23°C, f = 1MHz, VREF =1.4V ± 200 mV)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Address(A0~A12, BA0~BA1)	C_{ADD}	15	25	pF
/RAS, /CAS, /WE	C_{IN}	15	25	pF
CKE(CKE0)	C_{CKE}	15	25	pF
Clock (CLK0)	C_{CLK}	7.5	9	pF
/CE (/CE1)	C_{CS}	15	25	pF
DQM (DQM0 ~ DQM3)	C_{DQM}	6.5	7.5	pF
DQ (DQ0 ~ DQ32)	C_{OUT}	7	8.5	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	VERSION				UNIT	NOTE
			-A	-8	-H	-L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0mA	480	480	440	440	mA	1
Precharge standby current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max) t_{CC}=10ns	8				mA	
	$I_{CC2}PS$	CKE & CLK ≤ V_{IL}(max) t_{CC}=∞	8				mA	

Precharge standby current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min) CS* ≥ V_{IH}(min), t_{CC}=10ns Input signals are changed one time during 20ns	64				mA	
	$I_{CC2}NS$	CKE ≥ V_{IH}(min) CLK ≤ V_{IL}(max), t_{CC}=∞ Input signals are stable	56				mA	
Active standby current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), t_{CC}=10ns	24				mA	
	$I_{CC3}PS$	CKE&CLK ≤ V_{IL}(max) t_{CC}=∞	24				mA	
Active standby current in non power-down mode (One bank active)	$I_{CC3}N$	CKE≥V_{IH}(min), CS*≥V_{IH}(min), t_{CC}=10ns Input signals are changed one time during 20ns	120				mA	
	$I_{CC3}NS$	CKE≥VIH(min) CLK ≤VIL(max), t_{CC}=∞ Input signals are stable	100				mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs	560	560	460	460	mA	1
Refresh current	I_{CC5}	t_{RC} ≥ t_{RC}(min)	840	840	800	800	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	20				mA	G
			8				mA	F

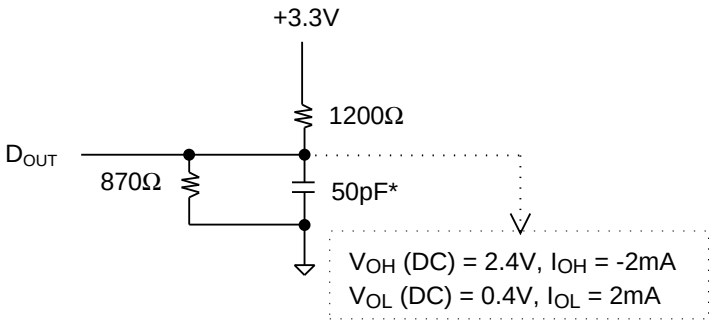
Notes :

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

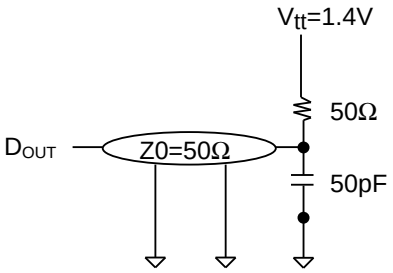
AC OPERATING TEST CONDITIONS

(vcc = 3.3V ± 0.3V, TA = 0 to 70°C)

PARAMETER	Value	UNIT
AC Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	VERSION				UNIT	NOTE
			-A	-8	-H	-L		
Row active to row active delay		t_{RRD}(min)	15	16	20	20	ns	1
RAS to CAS delay		t_{RP}(min)	20	20	20	20	ns	1
Row precharge time		t_{RP}(min)	20	20	20	20	ns	1
Row active time		t_{RAS}(min)	45	48	50	50	ns	1
		t_{RAS}(max)	100				ns	
Row cycle time		$_{tRC}$(min)	65	68	70	70	ns	1
Last data in to row precharge		t_{RDL}(min)	2				CLK	2.5
Last data in to Active delay		t_{DAL}(min)	2 CLK + 20 ns				-	5
Last data in to new col. address delay		t_{CDL}(min)	1				CLK	2
Last data in to burst stop		t_{BDL}(min)	1				CLK	2
Col. address to col. address delay		t_{CCD}(min)	1				CLK	3
Number of valid output data	CAS latency=3		2				ea	4
	CAS latency=2		-		1			

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. For -8/H/L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
   (Recommand : tRDL=2CLK and tDAL=2CLK & 20ns.)

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	-A		-8		-H		-L		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	8	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		10		12			
CLK to valid output delay	CAS latency=3	t_{SAC}		5.4		6		6		6	ns	1,2
	CAS latency=2			-		-		6		7		
Output data hold time	CAS latency=3	t_{OH}	2.7		3		3		3		ns	2
	CAS latency=2		-		-		3		3			
CLK high pulse width		t_{CH}	2.5		3		3		3		ns	3
CLK low pulse width		t_{CL}	2.5		3		3		3		ns	3
Input setup time		t_{SS}	1.5		2		2		2		ns	3
Input hold time		t_{SH}	0.8		1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		1		ns	3
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		5.4		6		6		6	ns	2
	CAS latency=2			-		-		6		7	ns	

Notes :
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered, ie., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DQM	BA 0,1	A10/ AP	A11,A12, A9~A0	NOTE
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		

Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge disable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge disable									H		4,5
Burst Stop		H	X	L	L	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X	X	X	X	X				
Precharge power down mode	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	V	V	V					
DQM		H	X					V	X			7
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :

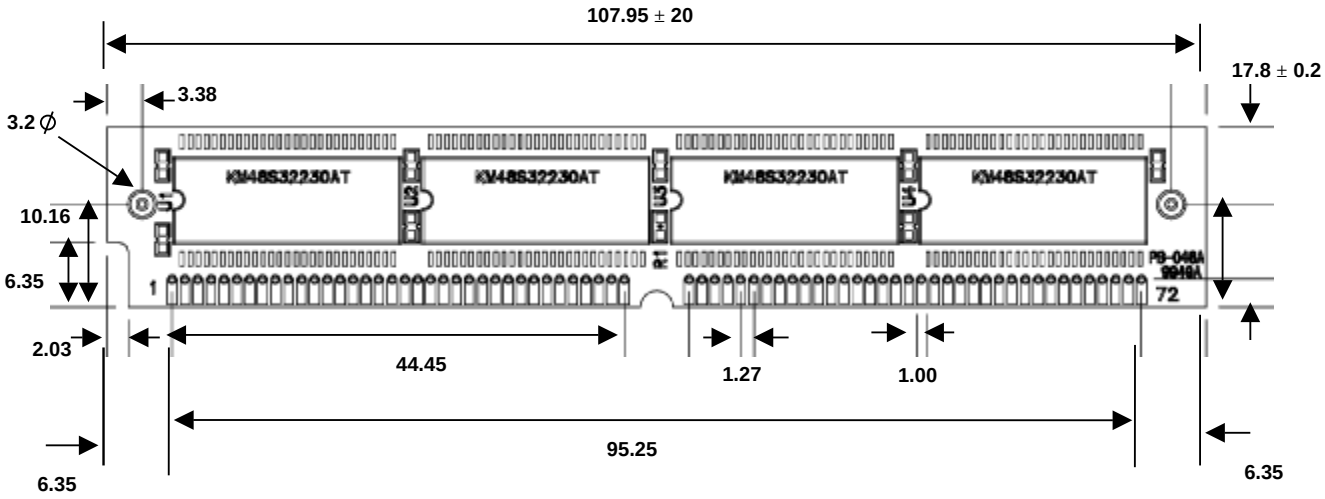
1. OP Code : Operand code
   A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

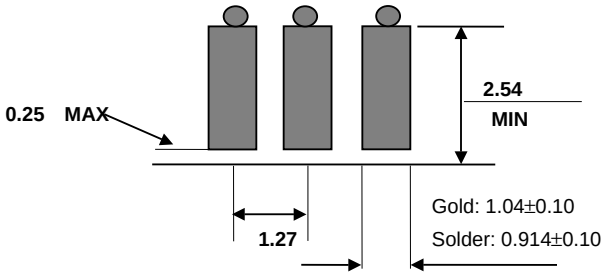
TIMING DIAGRAMS

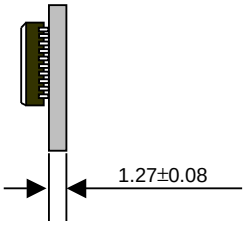
Please refer to timing diagram chart (II)

PACKAGING INFORMATION

Unit : mm







(Solder & Gold Plating)

ODERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	Feature	MAX.frq
HSD32M32M4V-13	128MByte	32Mx 32	72 Pin SIMM	8K	3.3V		133MHz (CL=3)
HSD32M32M4V-F13	128MByte	32Mx 32	72 Pin SIMM	8K	3.3V	Low Power	133MHz (CL=3)
HSD32M32M4V-12	128MByte	32Mx 32	72 Pin SMM	8K	3.3V		125MHz (CL=3)
HSD32M32M4V-F12	128MByte	32Mx 32	72 Pin SIMM	8K	3.3V	Low Power	125MHz (CL=3)
HSD32M32M4V-10	128MByte	32Mx 32	72 Pin SIMM	8K	3.3V		100MHz (CL=2)
HSD32M32M4V-F10	128MByte	32Mx 32	72 Pin SIMM	8K	3.3V	Low Power	100MHz (CL=2)
HSD32M32M4V-10L	128MByte	32Mx 32	72 Pin SIMM	8K	3.3V		100MHz
HSD32M32M4V-F10L	128MByte	32Mx 32	72 Pin SIMM	8K	3.3V	Low Power	100MHz

F means Auto & Self refresh with Low –Power (3.3V)