



AK4124

192kHz / 24Bit High Performance Asynchronous SRC

GENERAL DESCRIPTION

AK4124 is a stereo digital sample rate converter (SRC). The input sample rate ranges from 8kHz to 216kHz. The output sample rate is from 8kHz to 216kHz. By using the AK4124, the system can take very simple configuration because the AK4124 has an internal PLL and does not need any master clock at slave mode. Then the AK4124 is suitable for the application interfacing to different sample rates like high-end Car Audio, DVD recorder, etc.

FEATURES

1. SRC

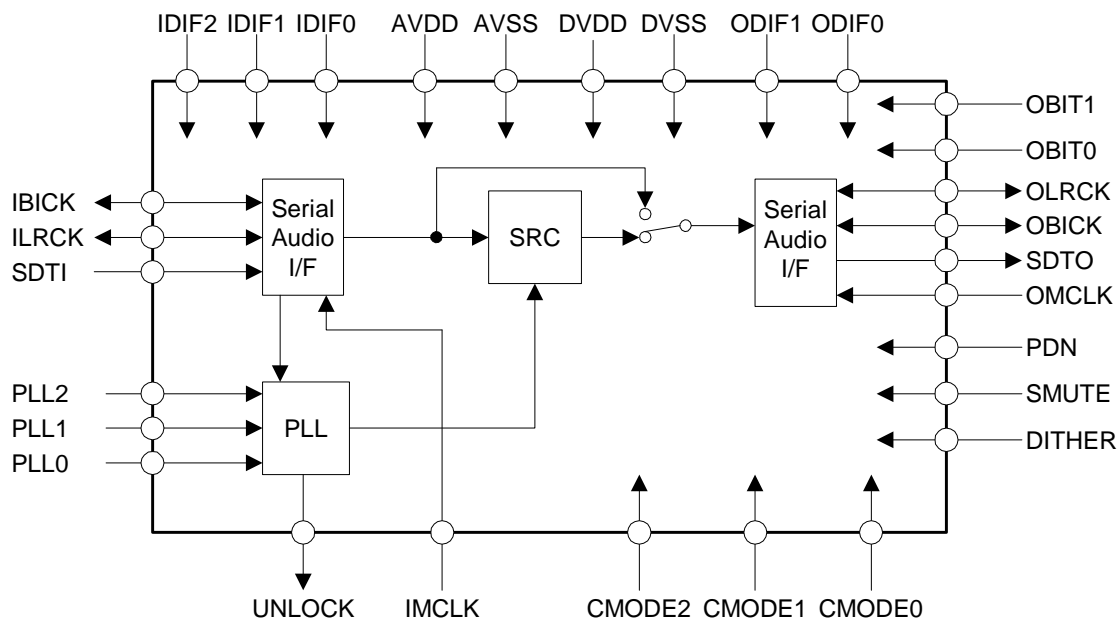
- Asynchronous Sample Rate Converter
- Input Sample Rate Range (fsi) : 8kHz ~ 216kHz
- Output Sample Rate (fso) : 8kHz ~ 216kHz
- Input to Output Sample Rate Ratio : 1/6 to 6
- THD+N : -130dB
- Dynamic Range : 140dB (A-weighted)
- I/F format : MSB justified, LSB justified and I²S compatible
- PLL for Internal Operation Clock
- Clock for Master mode : 128/192/256/384/512/768fsi, 128/192/256/384/512/768fso
- SRC Bypass mode
- Soft Mute Function

2. Power Supply

- AVDD, DVDD: 3.0 ~ 3.6V (typ. 3.3V)

3. Ta = -40 ~ 85°C

4. Package : 30pin VSOP

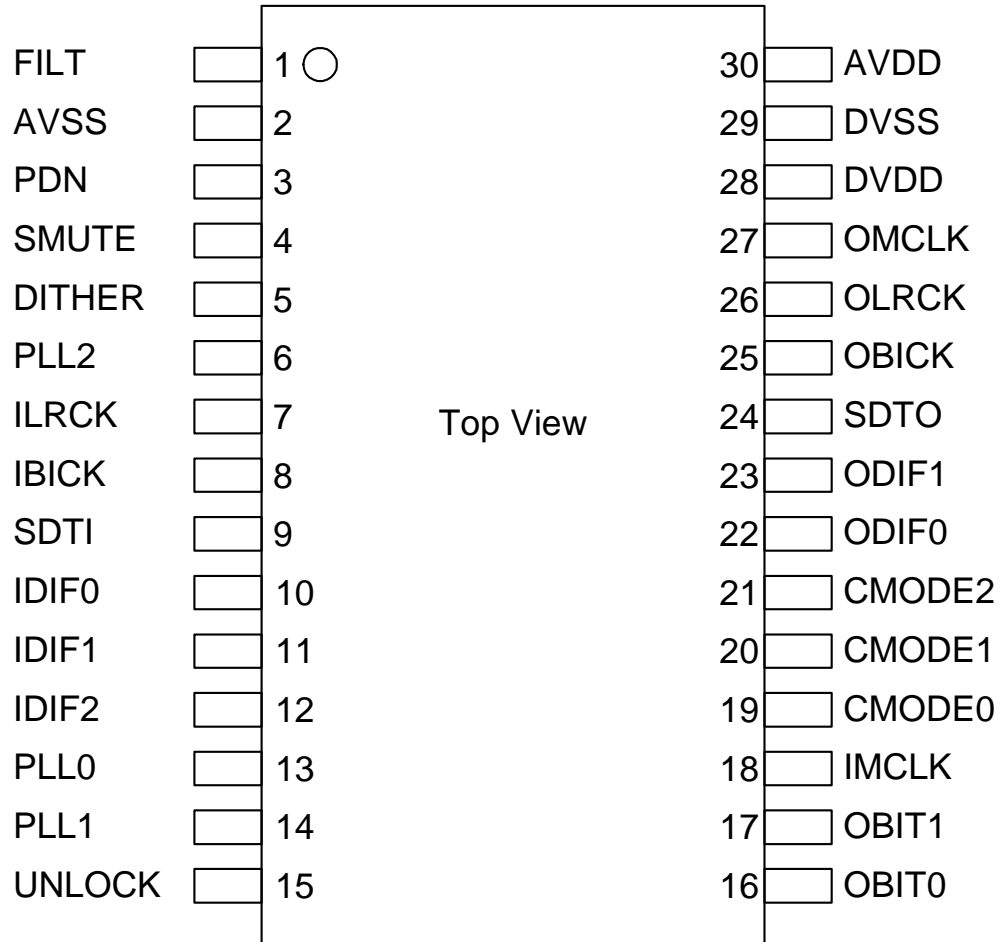


■ Ordering Guide

AK4124VF
AKD4124

-40 ~ +85°C 30pin VSOP (0.65mm pitch)
Evaluation Board for AK4124

■ Pin Layout



■ Compatibility with AK4121

| | AK4124 | AK4121 |
|--------------------------------------|----------------------------|-----------------------|
| Pin 5 | DITHER | DEM0 |
| Pin 6 | PLL2 | DEM1 |
| THD+N | -130dB | -113dB |
| D-Range (A-weighted) | 140dB | 117dB |
| Gain between Input and Output Signal | -0.01dB (typ) | -0.2dB (typ) |
| fs | 8kHz ~ 216kHz | 8kHz ~ 96kHz |
| Master mode for Input PORT | Yes | No |
| MCLK for Master mode (Input PORT) | 128/192/256/384/512/768fsi | No |
| MCLK for Master mode (Output PORT) | 128/192/256/384/512/768fso | 256/384/512/768fso |
| Output Data Length | 16/18/20/24 bit | 16/20 bit |
| De-emphasis Filter | No | Yes (32k/44.1k/48kHz) |
| PLL Unlock Flag (UNLOCK pin) | Yes | No |
| 5V tolerant | No | Yes (TVDD) |
| Package | 30VSOP | 24VSOP |

| PIN/FUNCTION | | | |
|--------------|----------|-----|---|
| No. | Pin Name | I/O | Function |
| 1 | FILT | O | PLL Loop Filter Pin |
| 2 | AVSS | - | Analog Ground Pin |
| 3 | PDN | I | Power-Down Mode Pin “H”: Power up, “L”: Power down reset and initializes the control register. |
| 4 | SMUTE | I | Soft Mute Pin “H” : Soft Mute, “L” : Normal Operation |
| 5 | DITHER | I | Dither Enable Pin “H” : Dither ON, “L” : Dither OFF |
| 6 | PLL2 | I | PLL Mode Select 2 Pin |
| 7 | ILRCK | I/O | Input Channel Clock Pin |
| 8 | IBICK | I/O | Audio Serial Data Clock Pin |
| 9 | SDTI | I | Audio Serial Data Input Pin |
| 10 | IDIF0 | I | Audio Interface Format 0 Pin for Input PORT |
| 11 | IDIF1 | I | Audio Interface Format 1 Pin for Input PORT |
| 12 | IDIF2 | I | Audio Interface Format 2 Pin for Input PORT |
| 13 | PLL0 | I | PLL Mode Select 0 Pin |
| 14 | PLL1 | I | PLL Mode Select 1 Pin |
| 15 | UNLOCK | O | Unlock Status Pin |
| 16 | OBIT0 | I | Bit Length Select 0 Pin for Output Data |
| 17 | OBIT1 | I | Bit Length Select 1 Pin for Output Data |
| 18 | IMCLK | I | Master Clock Input Pin for Input PORT |
| 19 | CMODE0 | I | Clock Mode Select 0 Pin |
| 20 | CMODE1 | I | Clock Mode Select 1 Pin |
| 21 | CMODE2 | I | Clock Mode Select 2 Pin |
| 22 | ODIF0 | I | Audio Interface Format 0 Pin for Output PORT |
| 23 | ODIF1 | I | Audio Interface Format 1 Pin for Output PORT |
| 24 | SDTO | O | Audio Serial Data Output Pin for Output PORT |
| 25 | OBICK | I/O | Audio Serial Data Clock Pin for Output PORT |
| 26 | OLRCK | I/O | Output Channel Clock Pin for Output PORT |
| 27 | OMCLK | I | Master Clock Input Pin for Output PORT |
| 28 | DVDD | - | Digital Power Supply Pin, 3.0 ~ 3.6V |
| 29 | DVSS | - | Digital Ground Pin |
| 30 | AVDD | - | Analog Power Supply Pin, 3.0 ~ 3.6V |

Note: All input pins should not be left floating.

■ Handling of Unused pins

The unused digital I/O pins should be processed appropriately as below.

| Classification | Pin Name | Setting |
|----------------|---------------|---|
| Analog | FILT | This pin should be open. |
| Digital | SMUTE, DITHER | These pins should be connected to DVSS. |
| | IMCLK, OMCLK | These pins should be connected to DVSS in slave mode. |
| | UNLOCK | This pin should be open. |

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

| Parameter | | Symbol | min | max | Units |
|--|-----------------------|--------|------|----------|-------|
| Power Supplies: | Analog | AVDD | -0.3 | 4.6 | V |
| | Digital | DVDD | -0.3 | 4.6 | V |
| | AVSS – DVSS (Note 2) | ΔGND | - | 0.3 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Digital Input Voltage | | VIND | -0.3 | DVDD+0.3 | V |
| Ambient Temperature (Power applied) | | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Note 1. All voltages with respect to ground.

Note 2. AVSS, BVSS and DVSS must be connected to the same ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

| Parameter | | Symbol | min | typ | max | Units |
|----------------------------|---------|--------|-----|-----|------|-------|
| Power Supplies (Note 3) | Analog | AVDD | 3.0 | 3.3 | 3.6 | V |
| | Digital | DVDD | 3.0 | 3.3 | AVDD | V |

Note 1. All voltages with respect to ground.

Note 3. The power up sequence between AVDD and DVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

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| SRC CHARACTERISTICS |
|----------------------------|

(Ta=25°C; AVDD=DVDD=3.3V; AVSS=DVSS=0V; data = 24bit; measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

| Parameter | Symbol | min | typ | max | Units |
|---|---------|-----|------|------|-------|
| SRC Characteristics: | | | | | |
| Resolution | | | | 24 | Bits |
| Input Sample Rate | FSI | 8 | | 216 | kHz |
| Output Sample Rate | FSO | 8 | | 216 | kHz |
| THD+N (Input = 1kHz, 0dBFS, Note 4) | | | | | |
| FSO/FSI = 44.1kHz/48kHz | | - | -130 | - | dB |
| FSO/FSI = 48kHz/44.1kHz | | - | -124 | - | dB |
| FSO/FSI = 48kHz/192kHz | | - | -129 | - | dB |
| FSO/FSI = 192kHz/48kHz | | - | -124 | - | dB |
| Worst Case (FSO/FSI = 48kHz/8kHz) | | - | - | -108 | dB |
| Dynamic Range (Input = 1kHz, -60dBFS, Note 4) | | | | | |
| FSO/FSI = 44.1kHz/48kHz | | - | 136 | - | dB |
| FSO/FSI = 48kHz/44.1kHz | | - | 136 | - | dB |
| FSO/FSI = 48kHz/192kHz | | - | 136 | - | dB |
| FSO/FSI = 192kHz/48kHz | | - | 132 | - | dB |
| Worst Case (FSO/FSI = 48kHz/32kHz) | | 132 | - | - | dB |
| Dynamic Range (Input = 1kHz, -60dBFS, A-weighted, Note 4) | | | | | |
| FSO/FSI = 44.1kHz/48kHz | | - | 140 | - | dB |
| Ratio between Input and Output Sample Rate | FSO/FSI | 1/6 | | 6 | - |

Note 4. Measured by Audio Precision System Two Cascade.

| FILTER CHARACTERISTICS | | | | | | |
|----------------------------------|--|-----|-----------|-------|-----------|------|
| (Ta=25°C; AVDD, DVDD=3.0 ~ 3.6V) | | | | | | |
| Parameter | Symbol | min | typ | max | Units | |
| Digital Filter | | | | | | |
| Passband -0.001dB | $0.985 \leq \text{FSO/FSI} \leq 6.000$ | PB | 0 | | 0.4583FSI | kHz |
| | $0.905 \leq \text{FSO/FSI} < 0.985$ | PB | 0 | | 0.4167FSI | kHz |
| | $0.714 \leq \text{FSO/FSI} < 0.905$ | PB | 0 | | 0.3195FSI | kHz |
| | $0.656 \leq \text{FSO/FSI} < 0.714$ | PB | 0 | | 0.2852FSI | kHz |
| | $0.536 \leq \text{FSO/FSI} < 0.656$ | PB | 0 | | 0.2182FSI | kHz |
| | $0.492 \leq \text{FSO/FSI} < 0.536$ | PB | 0 | | 0.1982FSI | kHz |
| | $0.452 \leq \text{FSO/FSI} < 0.492$ | PB | 0 | | 0.1740FSI | kHz |
| | $0.357 \leq \text{FSO/FSI} < 0.452$ | PB | 0 | | 0.1212FSI | kHz |
| | $0.324 \leq \text{FSO/FSI} < 0.357$ | PB | 0 | | 0.1072FSI | kHz |
| | $0.246 \leq \text{FSO/FSI} < 0.324$ | PB | 0 | | 0.0595FSI | kHz |
| | $0.226 \leq \text{FSO/FSI} < 0.246$ | PB | 0 | | 0.0484FSI | kHz |
| | $0.1667 \leq \text{FSO/FSI} < 0.226$ | PB | 0 | | 0.0182FSI | kHz |
| Stopband | $0.985 \leq \text{FSO/FSI} \leq 6.000$ | SB | 0.5417FSI | | | kHz |
| | $0.905 \leq \text{FSO/FSI} < 0.985$ | SB | 0.5021FSI | | | kHz |
| | $0.714 \leq \text{FSO/FSI} < 0.905$ | SB | 0.3965FSI | | | kHz |
| | $0.656 \leq \text{FSO/FSI} < 0.714$ | SB | 0.3643FSI | | | kHz |
| | $0.536 \leq \text{FSO/FSI} < 0.656$ | SB | 0.2974FSI | | | kHz |
| | $0.492 \leq \text{FSO/FSI} < 0.536$ | SB | 0.2732FSI | | | kHz |
| | $0.452 \leq \text{FSO/FSI} < 0.492$ | SB | 0.2510FSI | | | kHz |
| | $0.357 \leq \text{FSO/FSI} < 0.452$ | SB | 0.1983FSI | | | kHz |
| | $0.324 \leq \text{FSO/FSI} < 0.357$ | SB | 0.1822FSI | | | kHz |
| | $0.246 \leq \text{FSO/FSI} < 0.324$ | SB | 0.1366FSI | | | kHz |
| | $0.226 \leq \text{FSO/FSI} < 0.246$ | SB | 0.1255FSI | | | kHz |
| | $0.1667 \leq \text{FSO/FSI} < 0.226$ | SB | 0.0911FSI | | | kHz |
| Passband Ripple | PR | | | ±0.01 | | dB |
| Stopband Attenuation | SA | 113 | | | | dB |
| Group Delay (Note 5) | GD | - | 56 | - | | 1/fs |

Note 5. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.

| DC CHARACTERISTICS | | | | | | |
|--|-----------------|----------|-----|----------|-------|----|
| (Ta=25°C; AVDD, DVDD=3.0 ~ 3.6V) | | | | | | |
| Parameter | Symbol | min | typ | max | Units | |
| High-Level Input Voltage | V _{IH} | 70% DVDD | - | - | | V |
| Low-Level Input Voltage | V _{IL} | - | - | 30% DVDD | | V |
| High-Level Output Voltage (I _{out} =-400μA) | V _{OH} | DVDD-0.4 | - | - | | V |
| Low-Level Output Voltage (I _{out} =400μA) | V _{OL} | - | - | 0.4 | | V |
| Input Leakage Current | I _{in} | - | - | ±10 | | μA |
| Power Supplies | | | | | | |
| Power Supply Current | | | | | | |
| Normal operation (PDN pin = "H") | | | | | | |
| FSI=FSO=48kHz at Slave Mode: AVDD=DVDD=3.3V | | | 13 | | | mA |
| FSI=FSO=192kHz at Master Mode: AVDD=DVDD=3.3V | | | 55 | | | mA |
| : AVDD=DVDD=3.6V | | | | 85 | | mA |
| Power down (PDN pin = "L") (Note 6) | | | | | | |
| AVDD+DVDD | | | 10 | 100 | | μA |

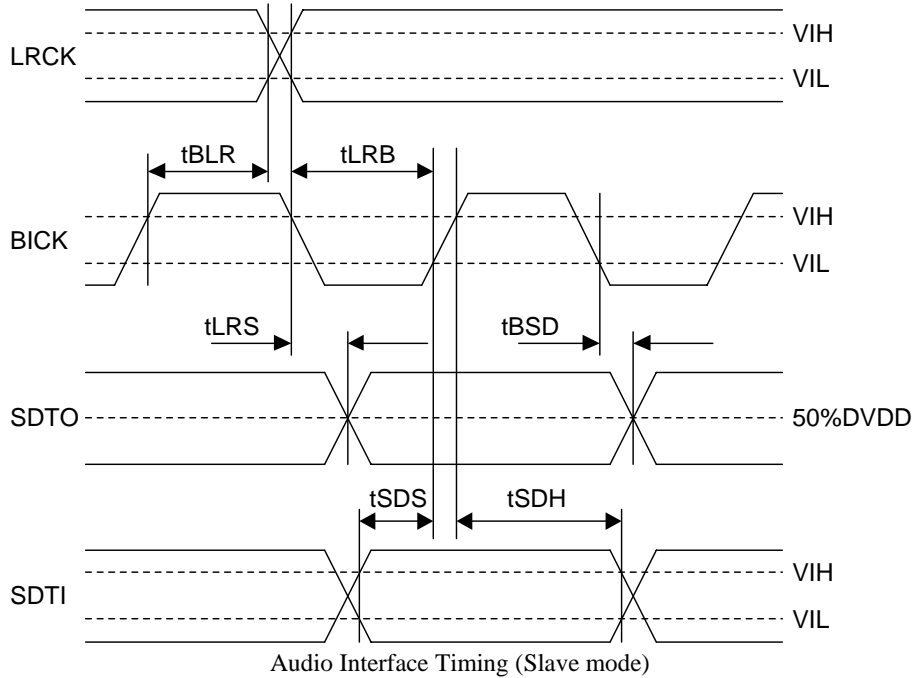
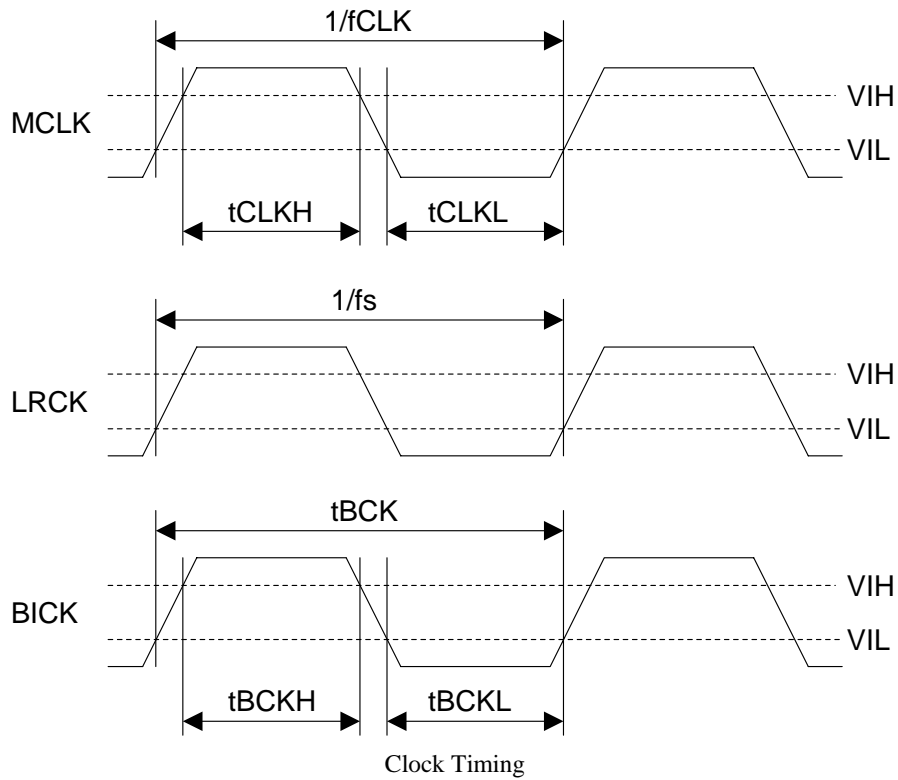
Note 6. All digital input pins are held DVSS.

| SWITCHING CHARACTERISTICS | | | | | |
|--|-------------|----------|------|--------|-------|
| (Ta=25°C; AVDD, DVDD=3.0 ~ 3.6V; CL=20pF) | | | | | |
| Parameter | Symbol | min | typ | max | Units |
| Master Clock Timing | | | | | |
| Frequency | fCLK | 1.024 | | 41.472 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | | | ns |
| Pulse Width High | tCLKH | 0.4/fCLK | | | ns |
| LRCK for Input data (ILRCK) | | | | | |
| Frequency | fs | 8 | | 216 | kHz |
| Duty Cycle | Duty | 48 | 50 | 52 | % |
| LRCK for Output data (OLRCK) | | | | | |
| Frequency | fs | 8 | | 216 | kHz |
| Duty Cycle | Duty | 48 | 50 | 52 | % |
| | Slave Mode | | | | |
| | Master Mode | | 50 | | % |
| Audio Interface Timing | | | | | |
| Input PORT (Slave mode) | | | | | |
| IBICK Period (8kHz ~ 108kHz) | tBCK | 1/128fs | | | ns |
| (108kHz ~ 216kHz) | tBCK | 1/64fs | | | ns |
| IBICK Pulse Width Low | tBCKL | 27 | | | ns |
| Pulse Width High | tBCKH | 27 | | | ns |
| ILRCK Edge to IBICK “↑” (Note 7) | tLRB | 15 | | | ns |
| IBICK “↑” to ILRCK Edge (Note 7) | tBLR | 15 | | | ns |
| SDTI Hold Time from IBICK “↑” | tSDH | 15 | | | ns |
| SDTI Setup Time to IBICK “↑” | tSDS | 15 | | | ns |
| Input PORT (Master mode) | | | | | |
| IBICK Frequency | fBCK | | 64fs | | Hz |
| IBICK Duty | dBCK | | 50 | | % |
| IBICK “↓” to ILRCK | tMBLR | -20 | | 20 | ns |
| SDTI Hold Time from IBICK “↑” | tSDH | 15 | | | ns |
| SDTI Setup Time to IBICK “↑” | tSDS | 15 | | | ns |
| Output PORT (Slave mode) | | | | | |
| OBICK Period (8kHz ~ 108kHz) | tBCK | 1/128fs | | | ns |
| (108kHz ~ 216kHz) | tBCK | 1/64fs | | | ns |
| OBICK Pulse Width Low | tBCKL | 27 | | | ns |
| Pulse Width High | tBCKH | 27 | | | ns |
| OLRCK Edge to OBICK “↑” (Note 7) | tLRB | 20 | | | ns |
| OBICK “↑” to OLRCK Edge (Note 7) | tBLR | 20 | | | ns |
| OLRCK to SDTO (MSB) (Except I ² S mode) | tLRS | | | 20 | ns |
| OBICK “↓” to SDTO | tBSD | | | 20 | ns |
| Output PORT (Master mode) | | | | | |
| OBICK Frequency | fBCK | | 64fs | | Hz |
| OBICK Duty | dBCK | | 50 | | % |
| OBICK “↓” to OLRCK | tMBLR | -20 | | 20 | ns |
| OBICK “↓” to SDTO | tBSD | -20 | | 20 | ns |
| Reset Timing | | | | | |
| PDN Pulse Width (Note 8) | tPD | 150 | | | ns |

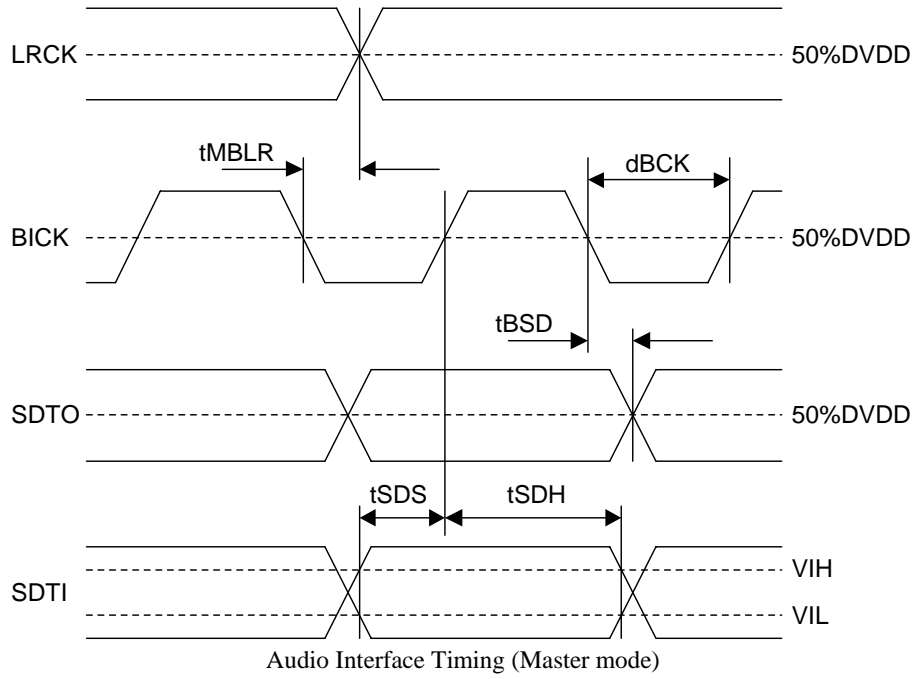
Note 7. BICK rising edge must not occur at the same time as LRCK edge.

Note 8. The AK4124 can be reset by bringing the PDN pin = “L”.

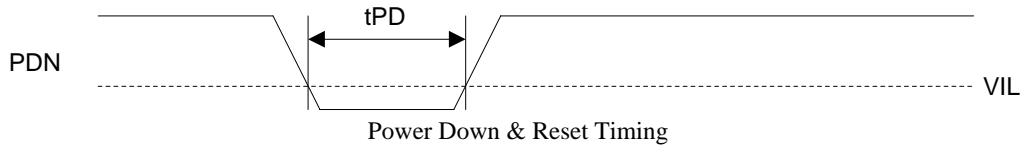
■ Timing Diagram



Note : BICK shows IBICK and OBICK, LRCK shows ILRCK and OLRCK.



Note : BICK shows IBICK and OBICK, LRCK shows ILRCK and OLRCK.



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| OPERATION OVERVIEW |
|---------------------------|

■ System Clock & Audio Interface Format for Input PORT

The input port works in master mode or slave mode. An internal system clock is created by the internal PLL using ILRCK (Mode 0 ~ 2 of Table 2) or IBICK (Mode 4 ~ 7 of Table 2) in slave mode. The MCLK is not needed in slave mode. And an internal system clock is created by IMCLK (Mode 8 ~ 15 of Table 2) in master mode. The PLL2-0 pins and IDIF2-0 pins select the master/slave and PLL mode. The PLL2-0 pins and IDIF2-0 pins should be controlled when PDN pin = "L".

The IDIF2-0 pins select the audio interface format for the input port. The audio data is MSB first, 2's compliment format. The SDTI is latched on the rising edge of IBICK. Select the audio interface format when PDN pin = "L". When in BYPASS mode, both IBICK and OBICK are fixed to 64fs.

| Mode | IDIF2 | IDIF1 | IDIF0 | SDTI Format | ILRCK | IBICK | IBICK Freq | Master / Slave |
|------|-------|-------|-------|---------------------------------------|--------|--------|------------------|----------------|
| 0 | L | L | L | 16bit, LSB justified | Input | Input | ≥ 32fsi | Slave |
| 1 | L | L | H | 20bit, LSB justified | | | ≥ 40fsi | |
| 2 | L | H | L | 24/20bit, MSB justified | | | ≥ 48fsi | |
| 3 | L | H | H | 24/16bit, I ² S Compatible | | | ≥ 48fsi or 32fsi | |
| 4 | H | L | L | 24bit, LSB justified | | | ≥ 48fsi | |
| 5 | H | L | H | 24bit, MSB justified | Output | Output | 64fs | Master |
| 6 | H | H | L | 24bit, I ² S Compatible | | | 64fs | |
| 7 | H | H | H | Reserved | | | | |

Table 1. Input Audio Interface Format (Input PORT)

| Mode | Master / Slave | PLL2 | PLL1 | PLL0 | ILRCK Freq | IBICK Freq | IMCLK | SMUTE (Note 5) | |
|------|---|------|------|-------|--------------------------|-------------------------|----------------------------|----------------|-----------|
| 0 | Slave IMCLK = DVSS IBICK = Input ILRCK = Input | L | L | L | 8k ~ 96kHz | Depending on IDIF2-0 | Not needed. (Note 4) | Manual | |
| 1 | | L | L | H | 8k ~ 216kHz | | | | |
| 2 | | L | H | L | 16k ~ 216kHz (Note 1) | | | | |
| 3 | | L | H | H | Reserved | | | | |
| 4 | | H | L | L | 8k ~ 216kHz (Note 2) | 32fsi (Note 3) | Not needed. (Note 4) | Manual | |
| 5 | | H | L | H | | 64fsi | | | |
| 6 | | H | H | L | | 128fsi | | | |
| 7 | H | H | H | 64fsi | | Semi-Auto | | | |
| 8 | Master IMCLK = Input IBICK = Output ILRCK = Output | L | L | L | 8k ~ 216kHz | 64fs | 128fs | Manual | |
| 9 | | L | L | H | 8k ~ 108kHz | | 256fs | | |
| 10 | | L | H | L | 8k ~ 54kHz | | 512fs | Semi-Auto | |
| 11 | | L | H | H | 8k ~ 216kHz | | 128fs | | |
| 12 | | H | L | L | 8k ~ 216kHz | | 192fs | Manual | |
| 13 | | H | L | H | 8k ~ 108kHz | | 384fs | | |
| 14 | | H | H | L | 8k ~ 54kHz | | 768fs | | |
| 15 | | H | H | H | 8k ~ 216kHz | | 192fs | | Semi-Auto |

Table 2. PLL Setting (Input PORT)

Note 1. PLL lock rage is changed by the value of R and C connected FILT pin. Refer to "PLL Loop Filter".

Note 2. The IBCIK must be continuous except when the clocks are changed.

Note 3. IBCIK = 32fsi is supported only 16bit LSB justified and I²S Compatible.

Note 4. Fixed to DVSS.

Note 5. Refer to "Soft Mute Operation" for Manual mode and Semi-Auto mode.

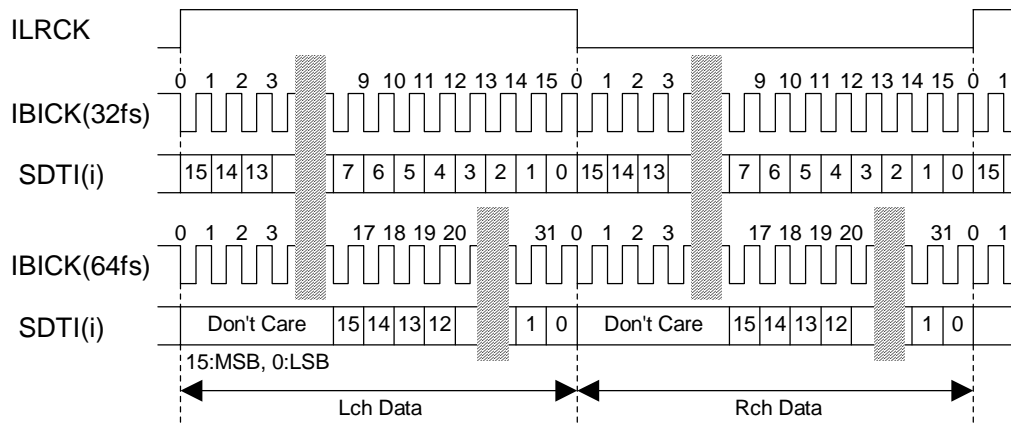


Figure 1. Mode 0 Timing

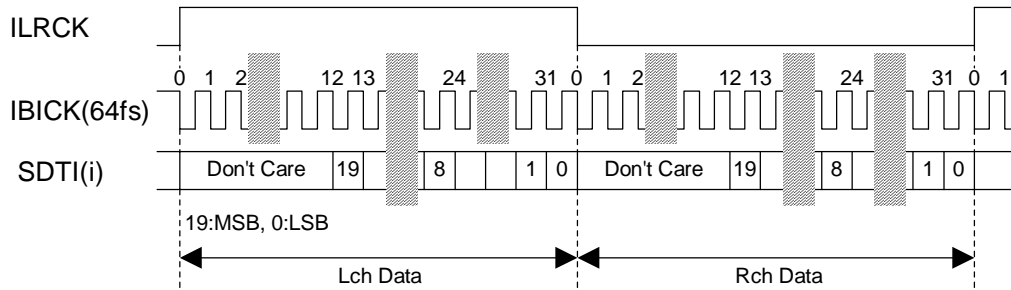


Figure 2. Mode 1 Timing

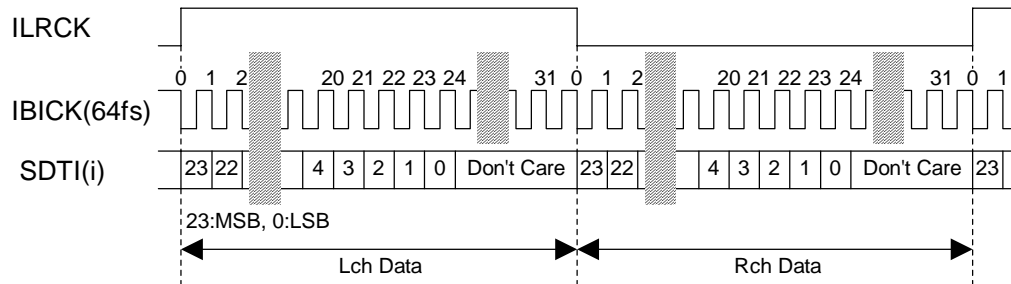


Figure 3. Mode 2,5 Timing (24bit MSB)

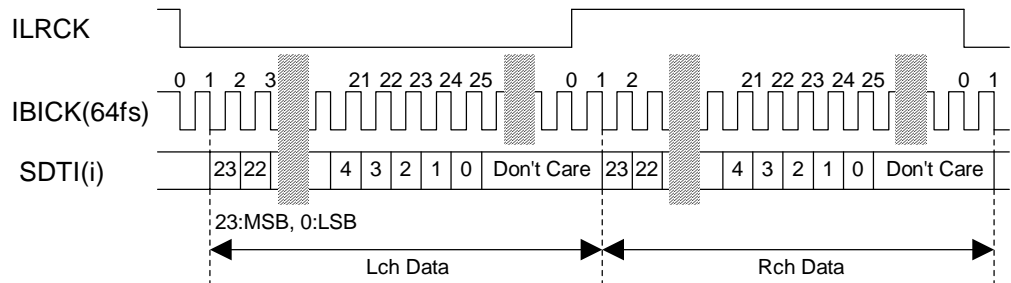


Figure 4. Mode 3, 6 Timing (24bit I²S)

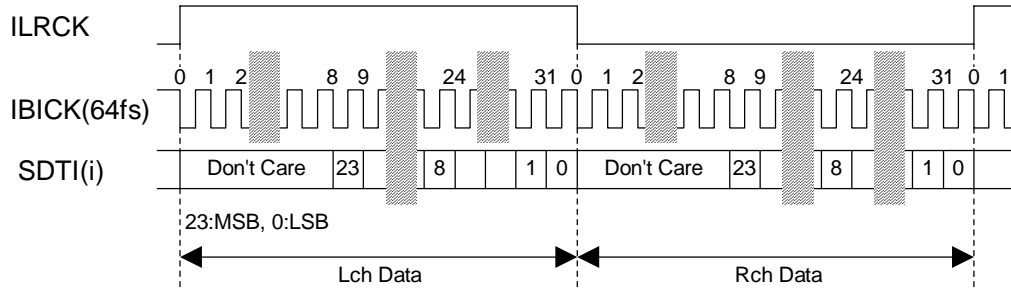


Figure 5. Mode 4 Timing

■ System Clock & Audio Interface Format for Output PORT

The output port works in master mode or slave mode. The MCLK is not needed in slave mode. The CMODE2-0 pins select the master/slave and bypass mode. The CMODE2-0 pins should be controlled when PDN pin = "L".

The ODIF1-0 pins and OBIT1-0 pins select the audio interface format for the output port. The audio data is MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of OBICK. Select the audio interface format when PDN pin = "L". When in BYPASS mode, both IBICK and OBICK are fixed to 64fs.

| Mode | CMODE2 | CMODE1 | CMODE0 | Master / Slave | OMCLK | fso |
|------|--------|--------|--------|-----------------|------------------------|-------------|
| 0 | L | L | L | Master | 256fso | 8k ~ 108kHz |
| 1 | L | L | H | Master | 384fso | 8k ~ 108kHz |
| 2 | L | H | L | Master | 512fso | 8k ~ 54kHz |
| 3 | L | H | H | Master | 768fso | 8k ~ 54kHz |
| 4 | H | L | L | Slave | Not used. Set to DVSS. | 8k ~ 216kHz |
| 5 | H | L | H | Master | 128fso | 8k ~ 216kHz |
| 6 | H | H | L | Master | 192fso | 8k ~ 216kHz |
| 7 | H | H | H | Master (Bypass) | Not used. Set to DVSS. | 8k ~ 216kHz |

Table 3. Master/Slave Control (Output PORT)

| Mode | ODIF1 | ODIF0 | SDTO Format |
|------|-------|-------|-----------------------------|
| 0 | L | L | LSB justified |
| 1 | L | H | (Reserved) |
| 2 | H | L | MSB justified |
| 3 | H | H | I ² S Compatible |

Table 4. Output Audio Interface Format 1 (Output PORT)

| Mode | Master / Slave | OBIT1 | OBIT0 | SDTO | OLRCK | OBICK | OBICK Frequency | |
|------|---|-------|-------|-------|--------|--------|---------------------------------|---------------|
| | | | | | | | MSB justified, I ² S | LSB justified |
| 0 | Slave CMODE2-0 = "HLL" | L | L | 16bit | Input | Input | ≥ 32fso | 64fso |
| 1 | | L | H | 18bit | | | ≥ 36fso | |
| 2 | | H | L | 20bit | | | ≥ 40fso | |
| 3 | | H | H | 24bit | | | ≥ 48fso | |
| 4 | Master Except CMODE2-0 = "HLL" | L | L | 16bit | Output | Output | 64fso | |
| 5 | | L | H | 18bit | | | | |
| 6 | | H | L | 20bit | | | | |
| 7 | | H | H | 24bit | | | | |

Table 5. Output Audio Interface Format 2 (Output PORT)

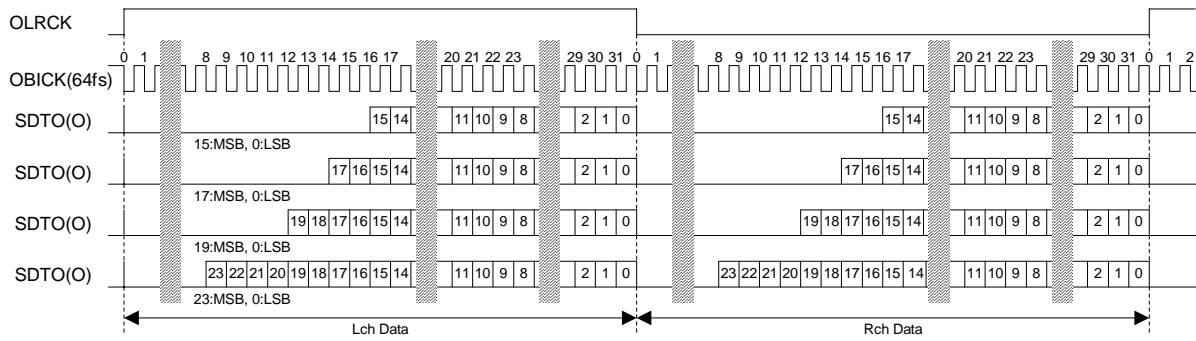


Figure 6. LSB Timing

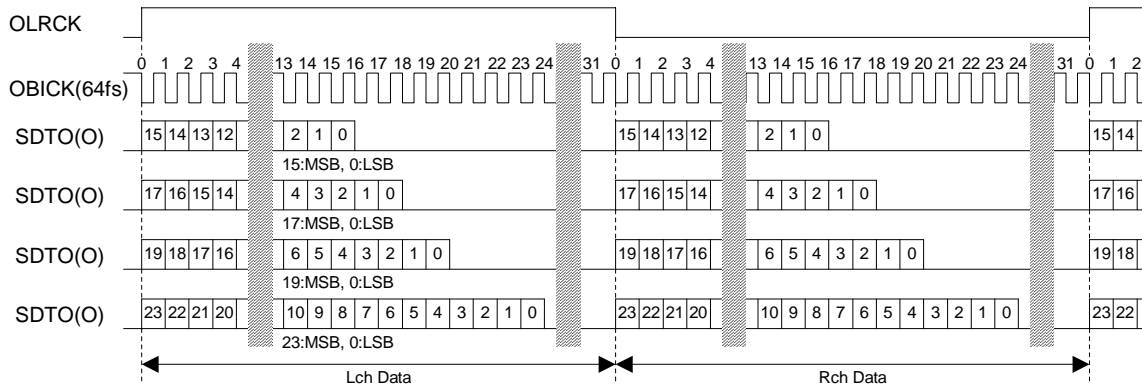


Figure 7. MSB Timing

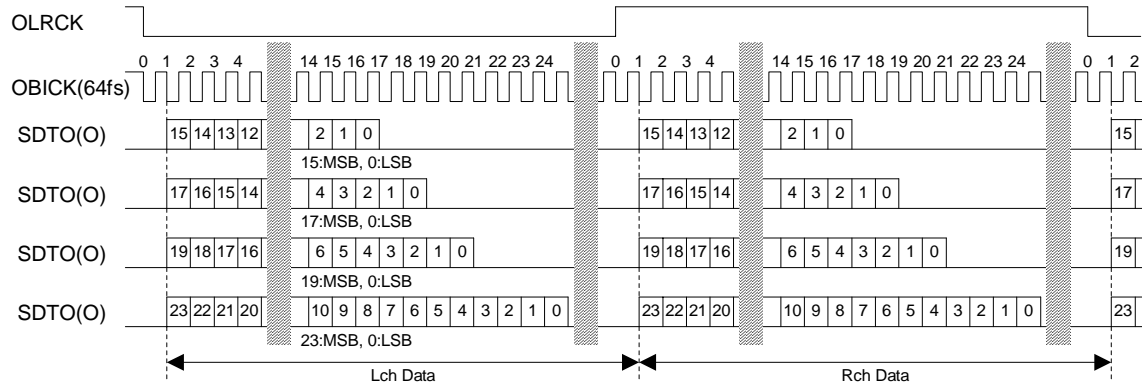


Figure 8. I²S Compatible Timing

■ Soft Mute Operation

1. Manual mode

Soft mute operation is performed in the digital domain of the SRC output. Soft mute can be controlled by SMUTE pin. When SMUTE pin goes “H”, the SRC output data is attenuated by $-\infty$ within 1024 OLRCK cycles. When the SMUTE pin goes “L” the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 OLRCK cycles. If the soft mute is cancelled before mute state after starting of the operation, the attenuation is discontinued and returned to 0dB by the same cycles. The soft mute is effective for changing the signal source.

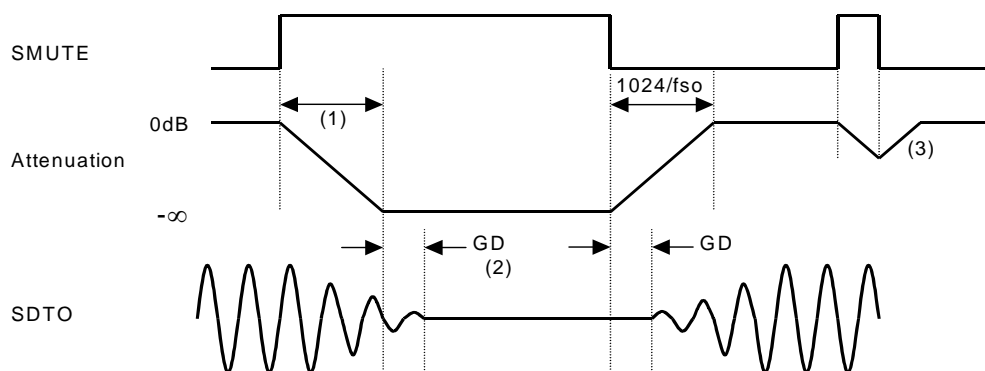


Figure 9. Soft Mute Function (Manual Mode)

- (1) The output data is attenuated by $-\infty$ during 1024 OLRCK cycles ($1024/f_{so}$).
- (2) Digital output delay from the digital input is called the group delay (GD).
- (3) If the soft mute is cancelled before attenuating to $-\infty$ after starting the operation, the attenuation is discontinued and returned to 0dB by the same number of clock cycles.

2. Semi-Auto mode

The soft mute is cancelled automatically by the setting of PLL2-0 pins (refer to Table 2), after the AK4124 detects the rising edge (PDN pin = “L” → “H”) and the mute is continued during $4410/f_{so}=100\text{ms}@f_{so}=44.1\text{kHz}$. After PDN pin = “L” → “H” and when SMUTE pin is “H”, the mute is not cancelled.

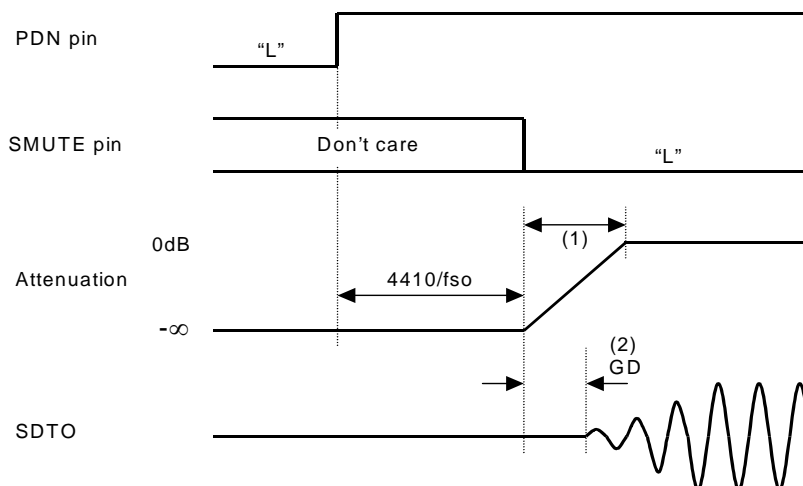


Figure 10. Soft Mute Function (Semi-Auto Mode)

- (1) The output data is attenuated by $-\infty$ during 1024 OLRCK cycles ($1024/f_{so}$).
- (2) Digital output delay from the digital input is called the group delay (GD).

■ Dither

The AK4124 has the dither circuit. The dither circuit adds the dither to the LSB of the output data set with the OBIT1-0 pins by DITHER pin = "H" regardless of the SRC mode or the SRC bypass mode.

■ System Reset

Bringing the PDN pin = "L" sets the AK4124 power-down mode and initializes the digital filter. The AK4124 should be reset once by bringing PDN pin = "L" upon power-up. When PDN pin = "L", the SDTO output is "L". The SDTO valid time is 100ms. Until then, the SDTO outputs "L".

Case 1

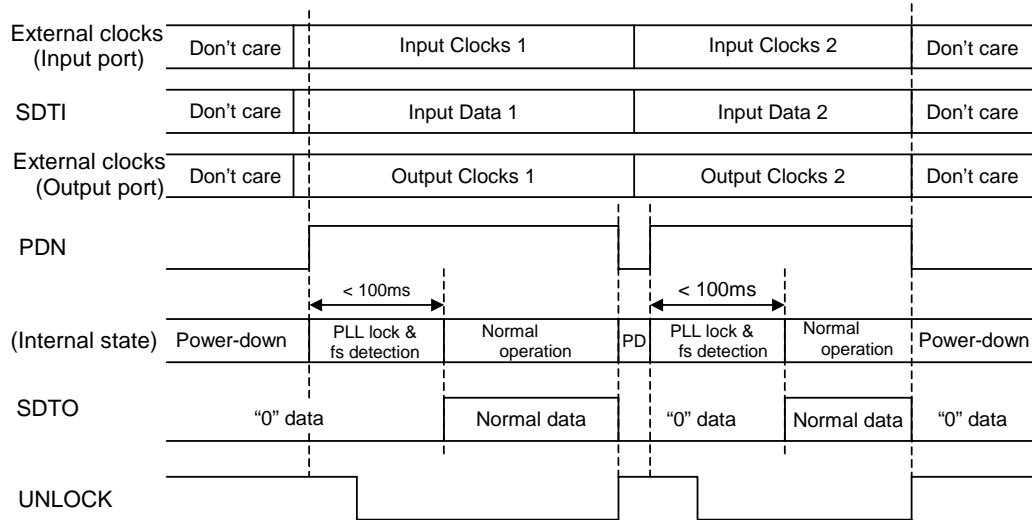


Figure 11. System Reset

Case 2

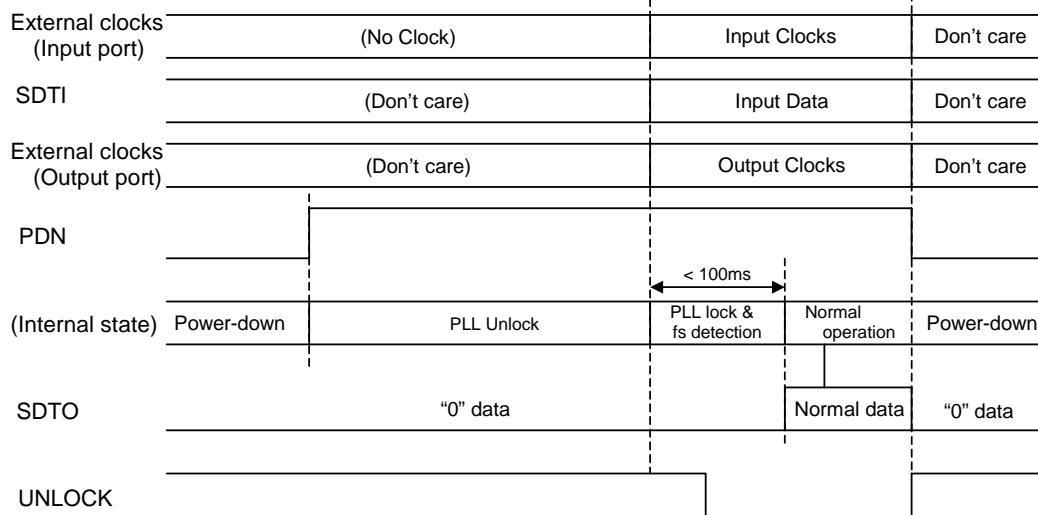


Figure 12. System Reset 2

■ Internal Reset Function for Clock Change

The change of the clock supplied to AK4124 is shown in Figure 13. When the frequency transition occurs gradually without phase change or the clock of output port is changed keeping $f_{s0}/f_{s1} > 4$, the internal reset is not executed and the SDTO takes time over 100ms to output normal data. To output normal data within 100ms, please reset by PDN pin = "L".

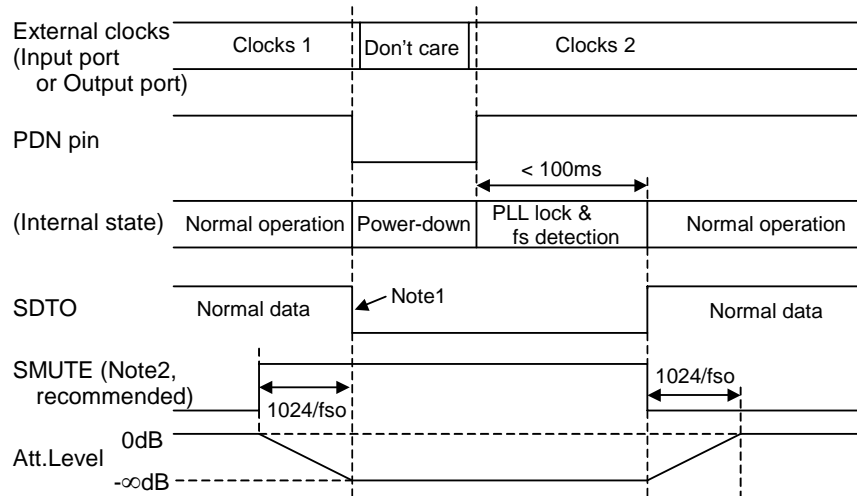


Figure 13. Sequence of changing clocks

Note 1. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to "0" from GD before PDN pin goes "L", which will cause the data on SDTO to remain "0".

Note 2. SMUTE can also be used to remove the unknown data.

■ UNLOCK pin

The UNLOCK pin outputs "L" when the internal PLL is locked. When the internal PLL is unlocked, the UNLOCK pin outputs "H". When PDN pin = "L", the UNLOCK pin outputs "H".

■ PLL Loop Filter

The C1 and R should be connected in series and attached between FILT pin and AVSS in parallel with C2. Please be careful the noise onto the FILT pin. When using IBICK, the value of an external element doesn't depend on the IBICK input frequency.

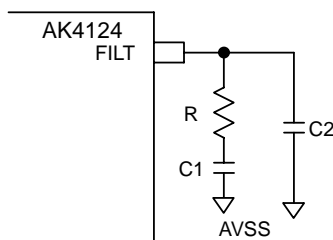


Figure 14. PLL Loop Filter

[Input PORT in slave mode]

1. When using ILRCK

| PLL2 | PLL1 | PLL0 | ILRCK | R [Ω] | C1 [μ F] | C2 [nF] |
|------|------|------|--------------|----------------|-----------------|-----------------|
| L | L | L | 8k ~ 96kHz | $1.8k \pm 5\%$ | $0.68 \pm 30\%$ | $0.68 \pm 30\%$ |
| L | L | H | 8k ~ 216kHz | $1k \pm 5\%$ | $1.0 \pm 30\%$ | $2.2 \pm 30\%$ |
| | | | 16k ~ 216kHz | $1.5k \pm 5\%$ | $0.68 \pm 30\%$ | $0.68 \pm 30\%$ |
| L | H | L | 8k ~ 216kHz | $1k \pm 5\%$ | $1.0 \pm 30\%$ | $2.2 \pm 30\%$ |
| | | | 16k ~ 216kHz | $1.5k \pm 5\%$ | $0.68 \pm 30\%$ | $0.68 \pm 30\%$ |

Table 6. PLL Loop Filter (ILRCK Mode)

- Note. The mode of between 16kHz and 216kHz the capacitor value (C1, C2) can be small.

2. When using IBICK

| PLL2 | PLL1 | PLL0 | ILRCK | R [Ω] | C1 [μ F] | C2 [nF] |
|------|------|------|-------------|----------------|-----------------|----------------|
| H | * | * | 8k ~ 216kHz | $470 \pm 5\%$ | $0.22 \pm 30\%$ | $1.0 \pm 30\%$ |

Table 7. PLL Loop Filter (IBICK Mode, *: Don't care)

Note. The IBCIK must be continuous except when the clocks are changed.

Note. IBCIK = 32fs is supported only 16bit LSB justified and I²S Compatible.

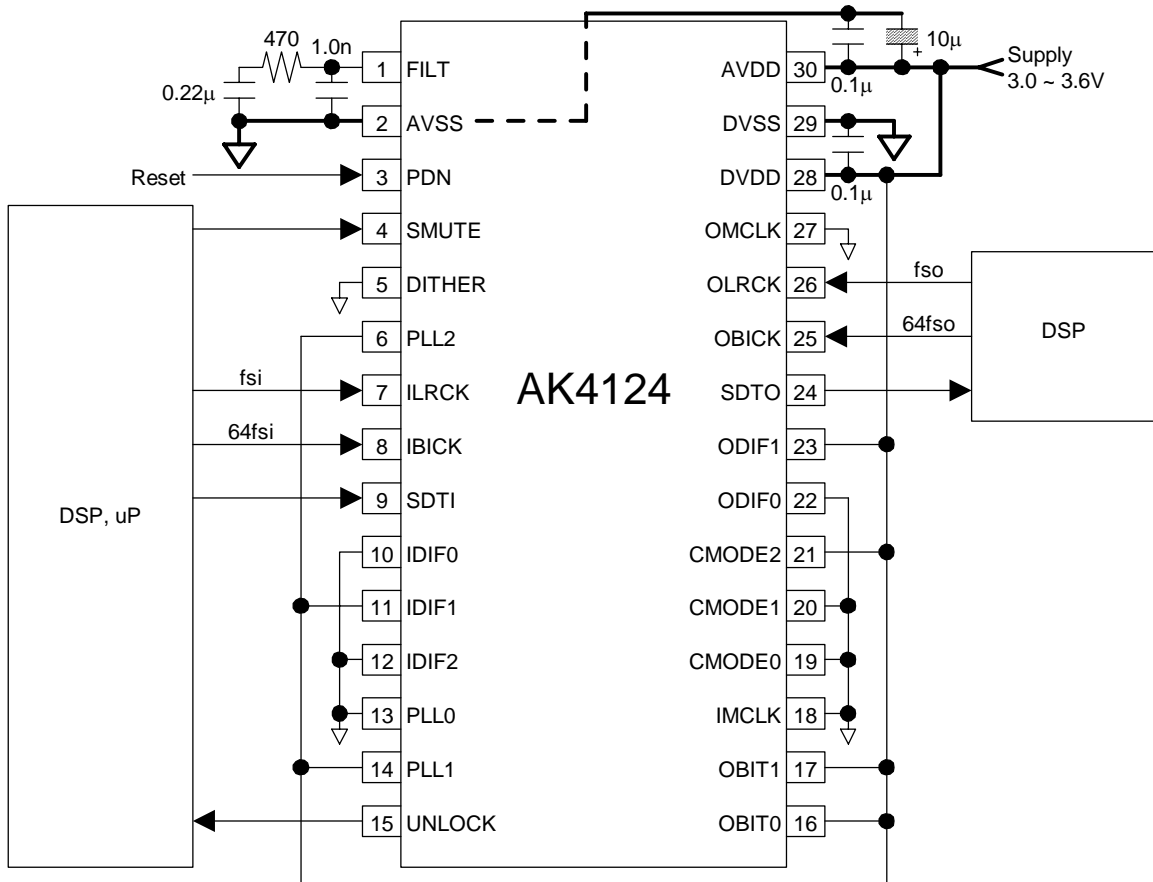
[Input PORT in master mode]

1. When IMCLK is 256fs, 384fs, 512fs or 768fs, an external element is not needed.
2. When IMCLK is 128fs or 192fs in master mode, an external element is needed in case of using IBICK.

SYSTEM DESIGN

Figure 15 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

- Input PORT : Slave Mode, IBICK lock mode (64fsi), 24bit MSB justified
- Output PORT : Slave mode, 24bit MSB justified
- Dither = OFF

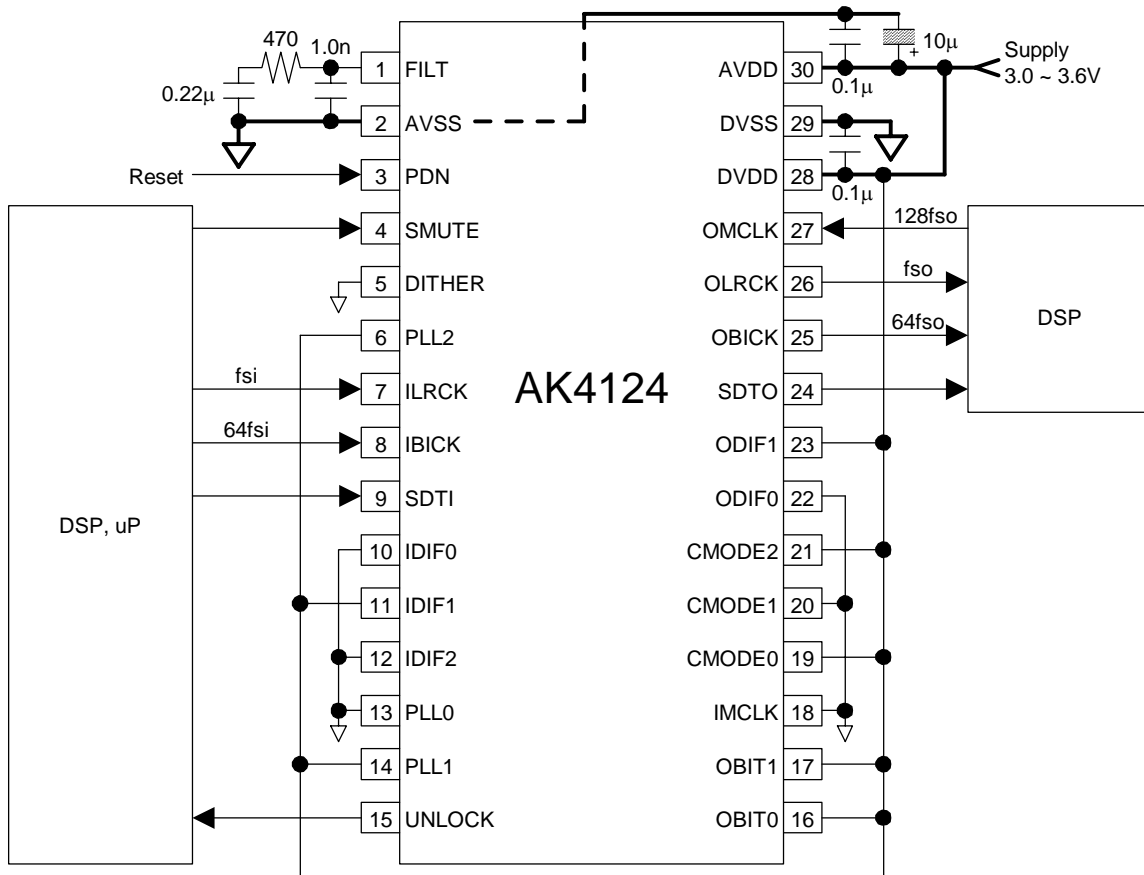


Note:

- AVSS and DVSS of the AK4124 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins should not be left floating.

Figure 15. Typical Connection Diagram (Slave mode)

- Input PORT : Slave Mode, IBICK lock mode (64fsi), 24bit MSB justified
- Output PORT : Master mode, 24bit MSB justified
- Dither = OFF



Note:

- AVSS and DVSS of the AK4124 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins should not be left floating.

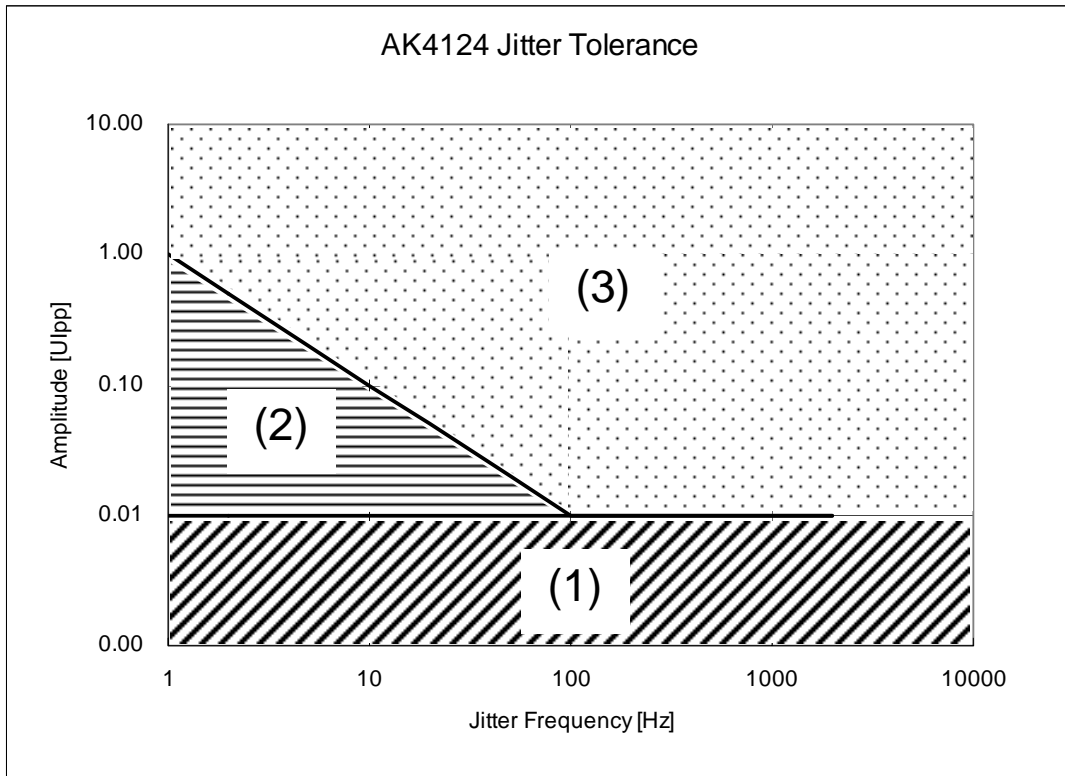
Figure 16. Typical Connection Diagram (Master mode)

1. Grounding and Power Supply Decoupling

The AK4124 requires careful attention to power supply and grounding arrangements. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. Decoupling capacitors should be as near to the AK4124 as possible, with the small value ceramic capacitor being the nearest.

2. Jitter Tolerance

Figure 17 shows the jitter tolerance to ILRCK and IBICK for AK4124. The jitter frequency and the jitter amplitude shown in Figure 17 define the jitter quantity. When the jitter amplitude is 0.01U_{ipp} or less, the AK4124 operate normally regardless of the jitter frequency.



- (1) Normal operation
- (2) There is a possibility that the distortion degrades. (It may degrade up to about -50dB.)
- (3) There is a possibility that the output data is lost.

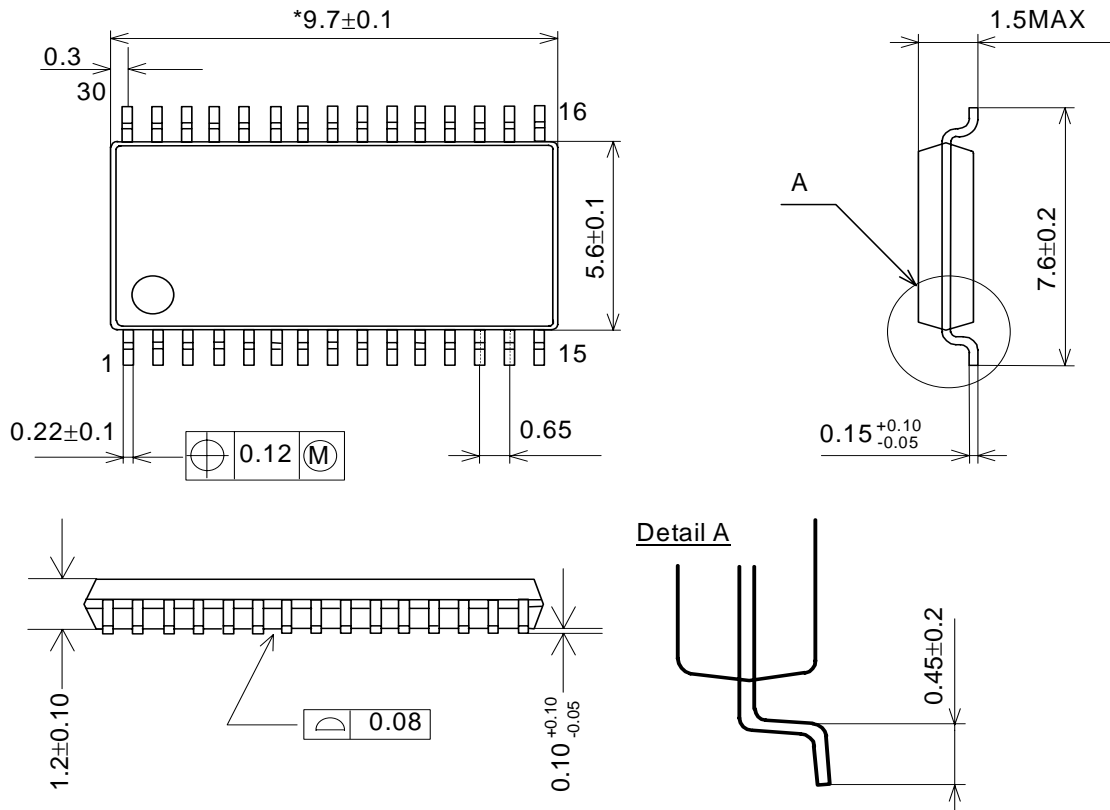
Note:

- When PLL2-0 = "L/L/L", "L/L/H", "L/H/L", the jitter amplitude is for ILRCK and 1UI (Unit Interval) is one cycle of ILRCK. When FSI = 48kHz, 1UI is 1/48kHz = 20.8μs.
- When PLL2-0 = "H/*/*" (*: Don't care), the jitter amplitude is for IBICK and 1UI (Unit Interval) is one cycle of IBICK. When FSI = 48kHz, 1UI is 1/(64 x 48kHz) = 326ns.

Figure 17. Jitter Tolerance

PACKAGE

30pin VSOP (Unit: mm)

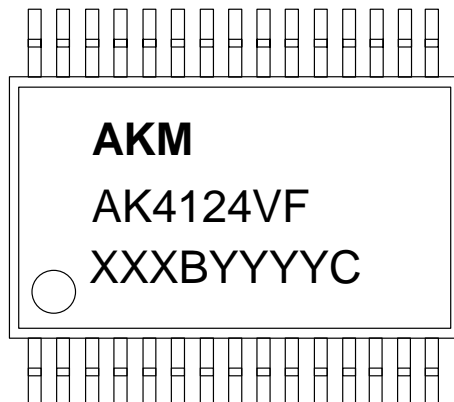


NOTE: Dimension "*" does not include mold flash.

Material & Lead finish

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXXYYYYC Date code identifier

XXXXB :Lot number (X : Digit number, B : Alpha character)
 YYYYYC : Assembly date (Y : Digit number, C : Alpha character)

Revision History

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|-----------------|----------|---------------|------|----------------------------|
| 04/01/26 | 00 | First Edition | | |
| 04/08/09 | 01 | Add Spec | 7 | Add FILTER CHARACTERISTICS |
| | | Add Spec | 21 | Add Jitter Tolerance |
| | | | | |

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