Three-Terminal Low Current Positive Voltage Regulator

Features

- 3-Ternimal Regulators
- Maximum Input Voltage : 30V
- Output Voltages of 5V,12V
- Output Current Up to 100mA
- No External Components
- Internal Thermal Overload Protection
- Internal Short-Circuit Limiting
- Output Voltage Offered in 4% tolerance
- SOP-8, SOT-89 and TO-92 Packages.

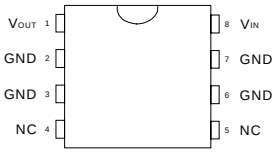
Applications

- Battery-Powered Circuitry
- Post Regulator for Switching Power Supply

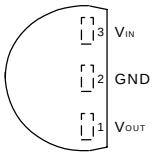
General Description

This series of fixed-voltage monolithic integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power-pass elements to make high-current voltage regulators. Each of these regulators can deliver up to 100mA of output current. The internal limiting and ternal shutdown features of these regulators make them essentially immune to overload. When used as a replacement for a Zener diode-resistor combination, an effective improvement in output impedance can be obtained together with lower-bias current.

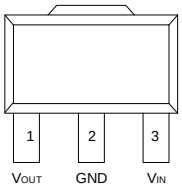
Pin Description



SOP-8 (Top View)



TO-92 (Top View)



SOT-89 (Front View)

Ordering and Marking Information

APL78L05/12 - □□-□□□

- Lead Free Code
- Handling Code
- Temp. Range
- Package Code

Package Code
E : TO-92 K : SOP-8 D : SOT-89
Temp. Range
C : 0 to 70 °C
Handling Code
TU : Tube TR : Tape & Reel PB : Plastic Bag
TB : Tape & Box
Lead Free Code
L : Lead Free Device Blank : Original Device

APL78L05/12 E : APL 78L05/12 XXXXX - XXXXX - Date Code

APL78L05/12 D/K : APL78L05/12 XXXXX - XXXXX - Date Code

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Rev. A.4 - Oct., 2003

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	30	V_{DC}
T_J	Operating Junction Temperature Range Control Section Power Transistor	 0 to 125 0 to 150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
θ_{JA}	Thermal Resistance from Junction to Ambient in Free Air SOP-8 SOT-89/TO-92	 160 180	°C/W

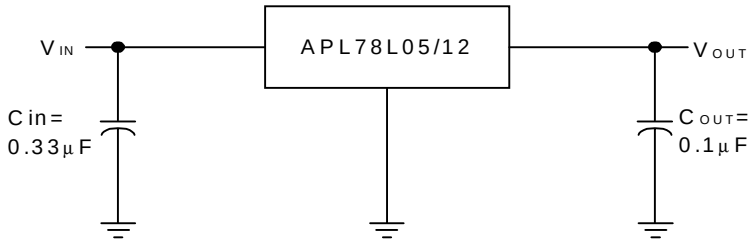
Electrical Characteristics

V_{IN}=10V, I_{OUT}=40mA, T_J=25°C, C_{IN}=0.33µF, C_{OUT}=0.1µF, unless otherwise specified

Symbol	Parameter	Test Condition	APL78L05			Unit
			Min.	Typ.	Max.	
V_O	Output Voltage		4.8	5.0	5.2	Vdc
V_O	Output Voltage (0° to +125°C)	1.0mA≤I_{OUT}≤40mA	4.75	5	5.25	Vdc
		7.0Vdc≤V_{IN}≤20Vdc				
		V_{IN}=10V, 1.0mA≤I_{OUT}≤40mA				
Reg_{line}	Line Regulation	7.0Vdc≤V_{IN}≤20Vdc		29	150	mV
		8.0Vdc≤V_{IN}≤20Vdc		26	100	
Reg_{load}	Load Regulation	1.0mA≤I_{OUT}≤100mA		9	60	mV
		1.0mA≤I_{OUT}≤40mA		5	30	
I_B	Quiescent Current			2.8	6.0	mA
ΔI_B	Quiescent Current Change	8.0Vdc≤V_{IN}≤20Vdc		0.15	1.5	mA
		1.0mA≤I_{OUT}≤40mA		0.08	0.1	
V_{IN}-V_O	Dropout Voltage	I_{OUT}=100mA		1.9		Vdc

Symbol	Parameter	Test Condition	APL78L12			Unit
			Min.	Typ.	Max.	
V_O	Output Voltage		11.5	12	12.5	Vdc
V_O	Output Voltage (0° to +125°C)	1.0mA≤I_{OUT}≤40mA	11.4	12	12.6	Vdc
		14Vdc≤V_{IN}≤27Vdc				
		V_{IN}=19V, 1.0mA≤I_{OUT}≤40mA				
Reg_{line}	Line Regulation	14.5Vdc≤V_{IN}≤27Vdc			250	mV
Reg_{load}	Load Regulation	1.0mA≤I_{OUT}≤100mA			100	mV
		1.0mA≤I_{OUT}≤40mA			50	
I_B	Quiescent Current				6.5	mA
ΔI_B	Quiescent Current Change	16Vdc≤V_{IN}≤27Vdc			1.5	mA
		1.0mA ≤I_{OUT}≤40mA				
V_{IN}-V_O	Dropout Voltage	I_{OUT}=100mA		1.9		Vdc

Application Circuit



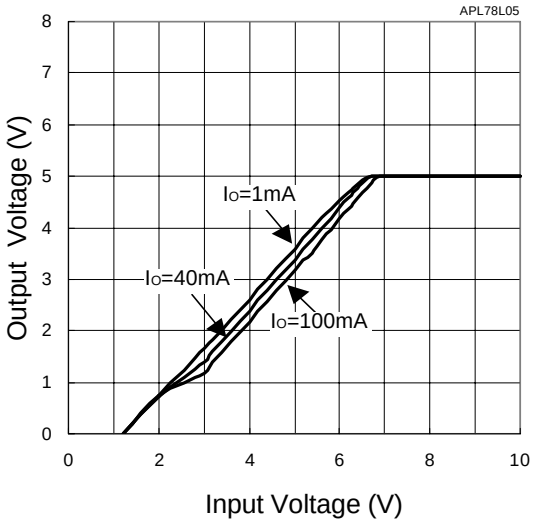
Note1 : A common ground is required between the input and the output voltage. The input voltage must remain typically 2V above the output voltage even during the low point on the input ripple voltage.

Note2 : Cin is required if regulator is located an appreciable distance from power supply filter.

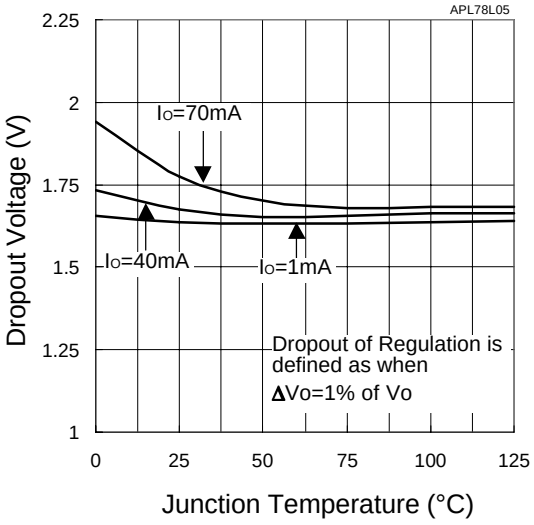
Note3 : C_{OUT} is not needed for stability; however, it does improve transient response.

Typical Characteristics

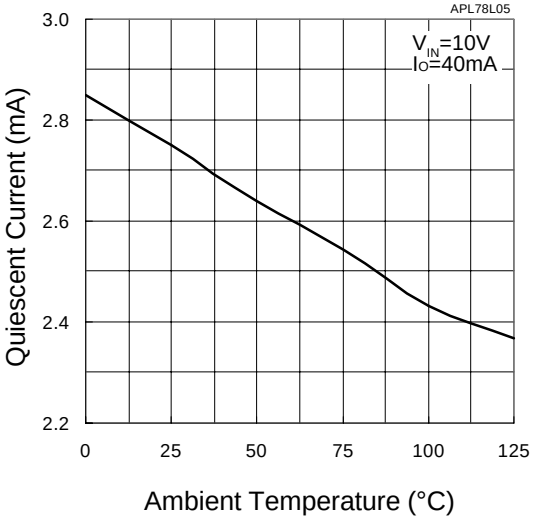
Output Voltage vs. Input Voltage



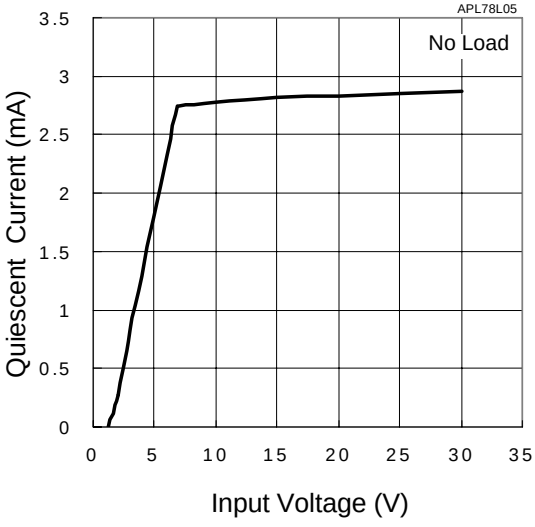
Dropout Voltage vs. Junction Temperature



Quiescent Current vs. Ambient Temperature

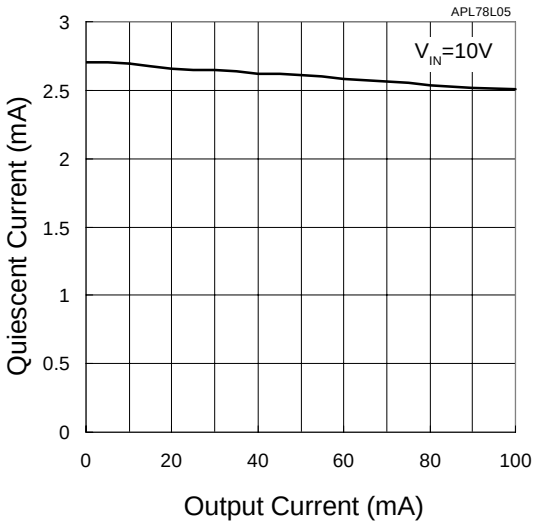


Quiescent Current vs. Input Voltage

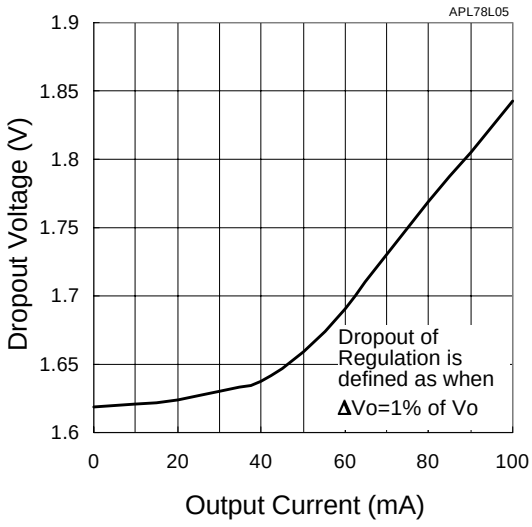


Typical Characteristics (Cont.)

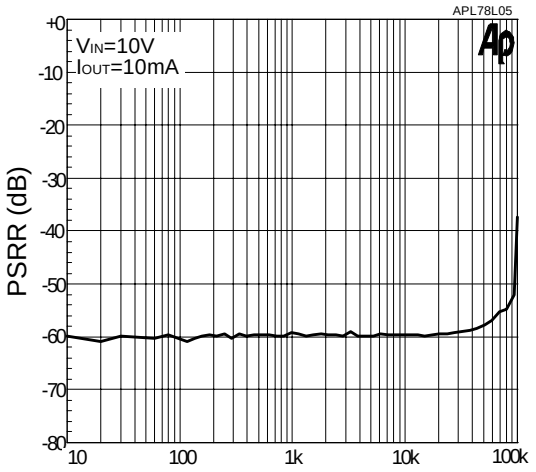
Quiescent Current vs. Output Current



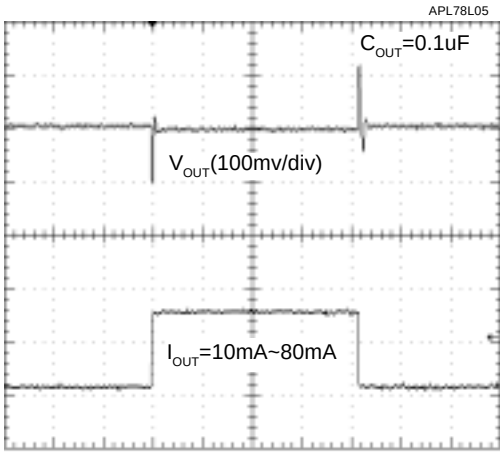
Dropout Voltage vs. Output Current



PSRR vs. Frequency

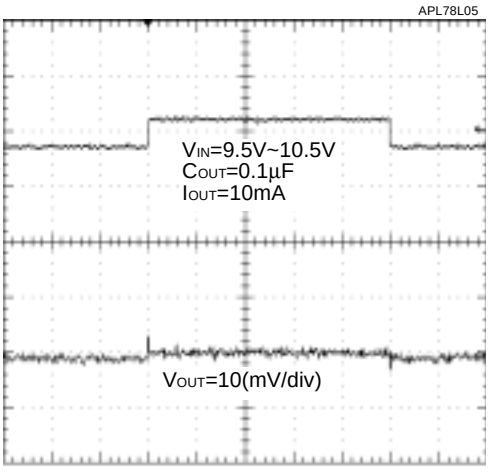


Load-Transient Response

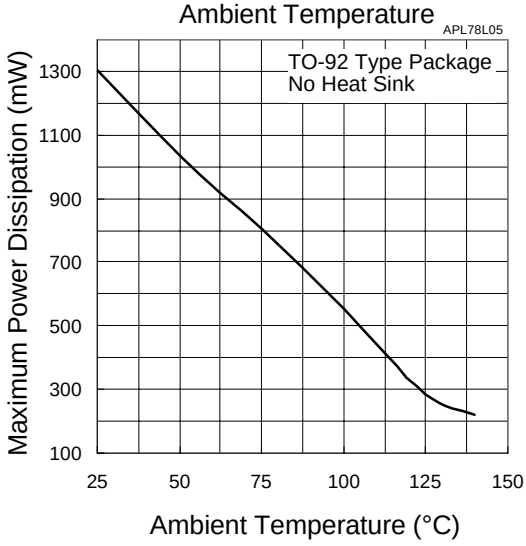


Typical Characteristics (Cont.)

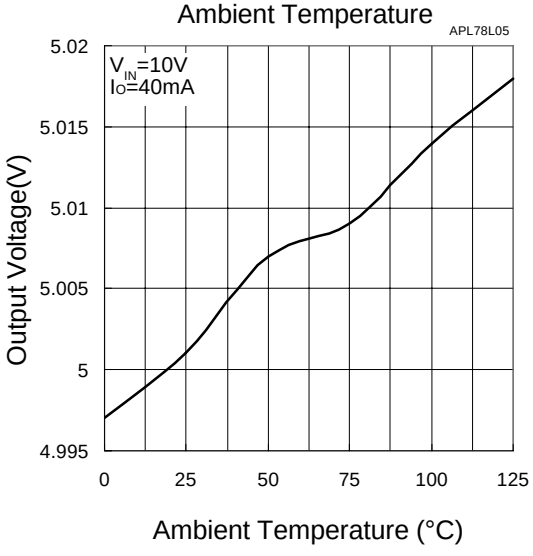
Line Transient Response



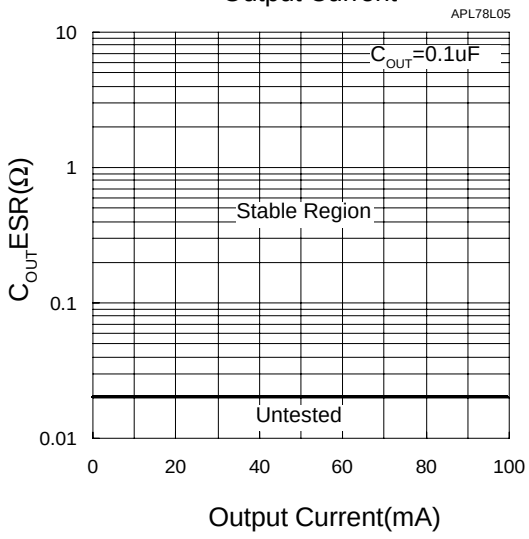
Maximum Power Dissipation vs. Ambient Temperature



Output Voltage vs. Ambient Temperature



Region of Stable ESR vs. Output Current

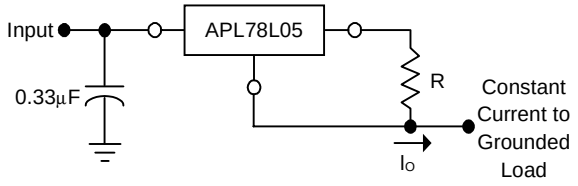


Typical Characteristics

The APL78L05/12 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 1. Current Regulator



The APL78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the APL78L05 is chosen in this application. Resistor R determines the current as follows :

$$I_O = \frac{5.0V}{R} + I_B$$

I_B =3.8mA over line and load changes

For example, a 100mA current source would require R to be a 50Ω, 1/2W resistor and the output voltage compliance would be the input voltage less 7V.

Figure 2. ±15V Tracking Voltage Regulator

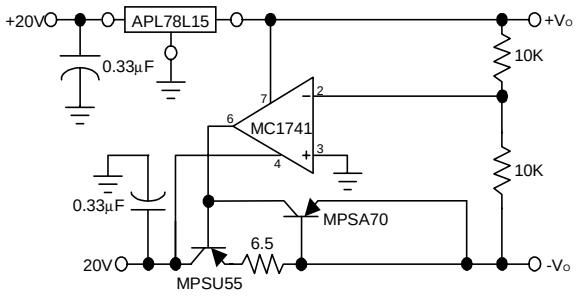
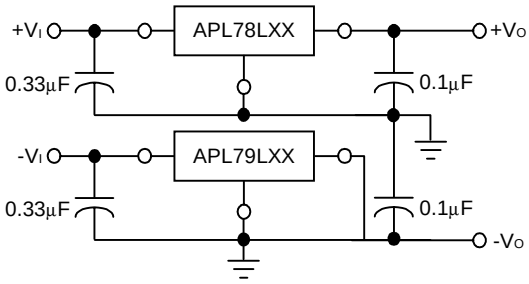
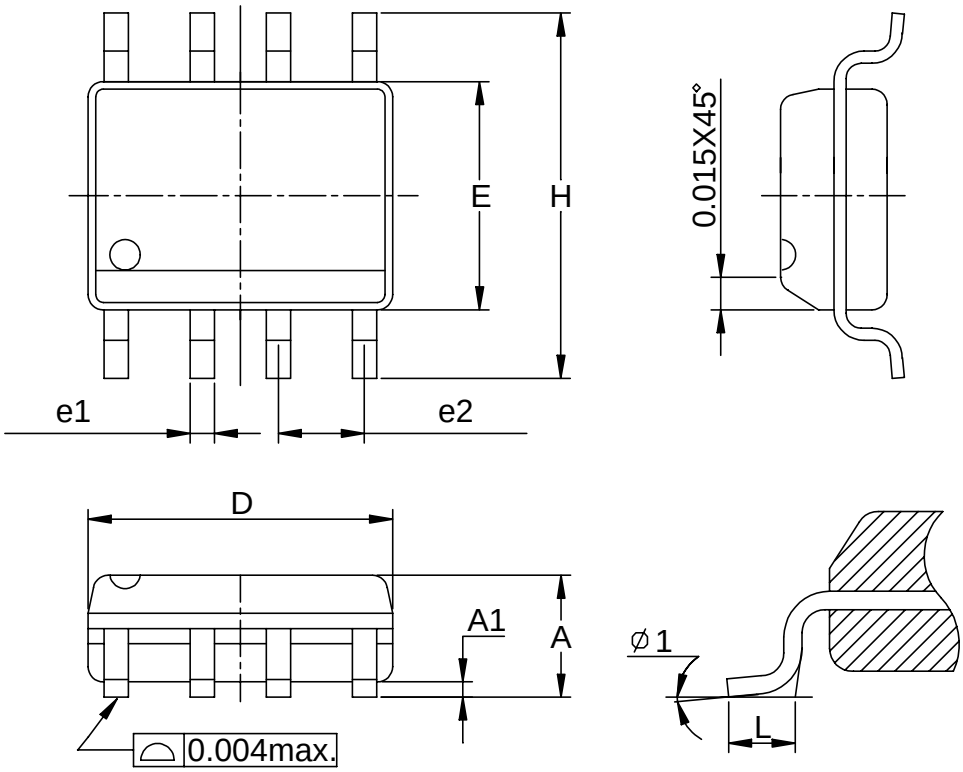


Figure 3. Positive and Negative Regulator



Packaging Information

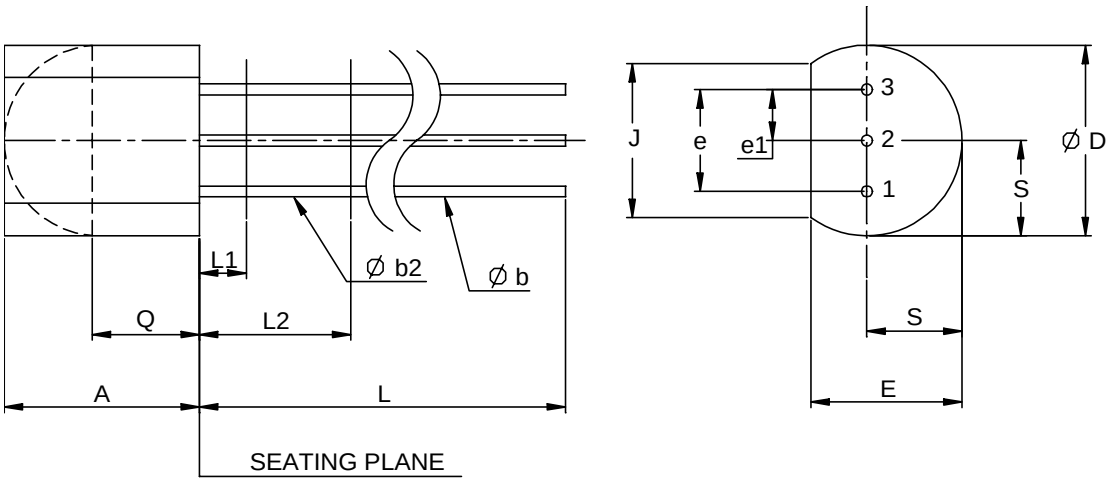
SOP-8 pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Package Information

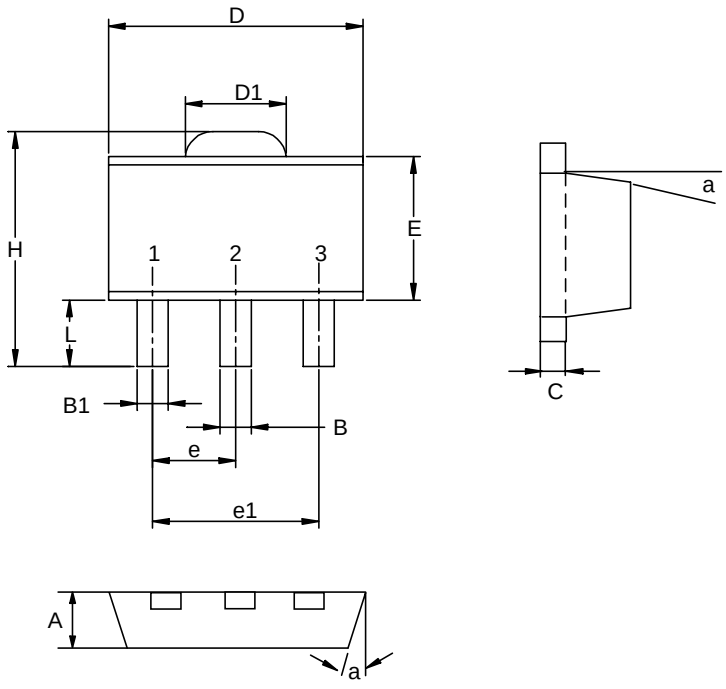
TO-92



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.58	5.33	0.170	0.210
ϕ b	0.41	0.53	0.160	0.021
ϕ b2	0.41	0.48	0.160	0.019
ϕ D	4.96	5.20	0.175	0.205
E	3.94	4.19	0.125	0.165
e	2.42	2.66	0.095	0.105
e1	1.15	1.39	0.045	0.055
J	3.43		0.135	
L	12.70		0.500	
L1		1.27		0.050
L2	6.35		0.250	
Q	2.93		0.115	
S	2.42	2.66	0.080	0.105

Package Information

SOT-89 (Reference EIAJ ED-7500A Reg stration SC-62)

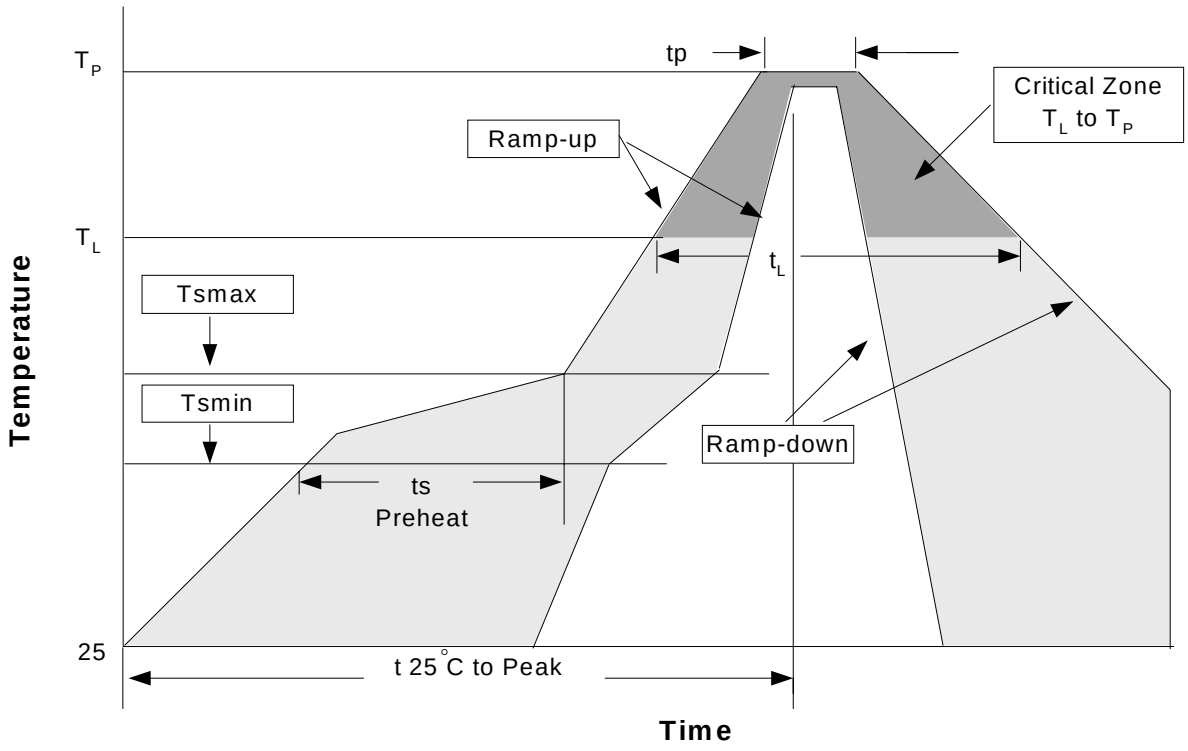


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.40	1.60	0.055	0.063
B	0.40	0.56	0.016	0.022
B1	0.35	0.48	0.014	0.019
C	0.35	0.44	0.014	0.017
D	4.40	4.60	0.173	0.181
D1	1.35	1.83	0.053	0.072
e	1.50 BSC		0.059 BSC	
e1	3.00 BSC		0.118 BSC	
E	2.29	2.60	0.090	0.102
H	3.75	4.25	0.148	0.167
L	0.80	1.20	0.031	0.047
α		10°		10°

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classificatin Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

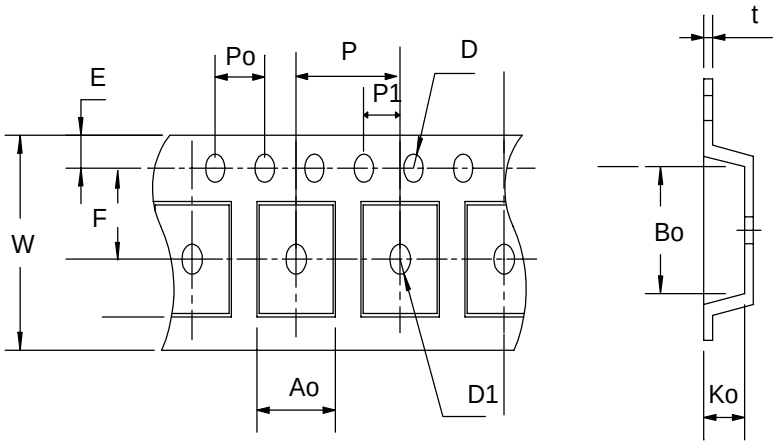
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

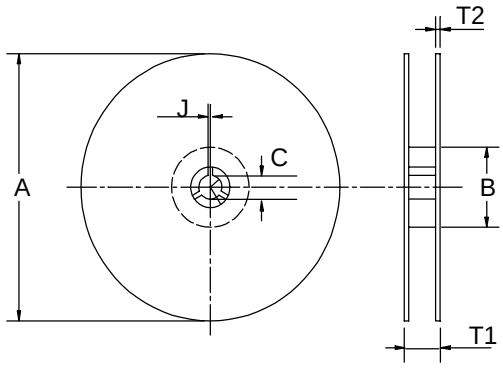
Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape & Reel Dimensions

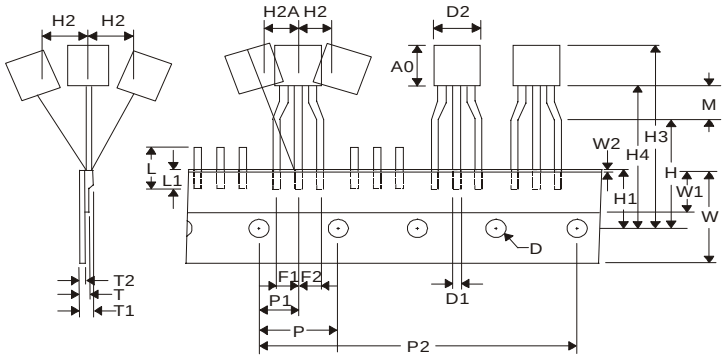


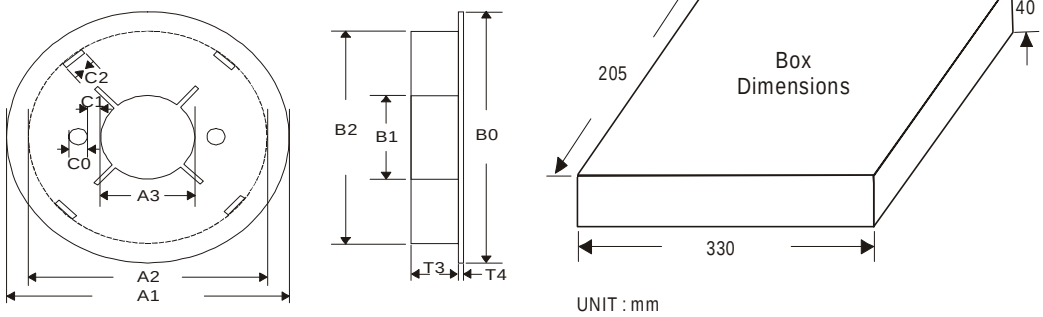
Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP-8	330±1	62 ± 1.5	12.75 + 0.1 5	2 + 0.5	12.4 +0.2	2± 0.2	12 + 0.3 - 0.1	8± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0.1	1.55±0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0.1	2.1± 0.1	0.3±0.013

(mm)





Carrier Tape & Reel Dimensions(Cont.)

Application	A	A1	A2	A3	B0	B1	B2	C0	C1
	3.18~12	90±1	76±1	30±1	90±1	31±1	76±1	5.8	3.8
	C2	H3	H4	L	L1	P	P1	P2	T
TO-92	7.8	27.0 MAX	20.0 MAX	11.0 MAX	2.5 MIN	12.7±0.2	6.35±0.4	50.8±0.5	0.55 MAX
	T1	T2	T3	T4	W	W1	W2		
	1.42 MAX	0.36~0.68	15	1.7	17.5~19	5.0~7.0	0.5 MAX		

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	9.3	2500
TO-92	17.5~19	5.0~7.0	2000

Customer Service

Anpec Electronics Corp.
Head Office :
5F, No. 2 Li-Hsin Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
7F, No. 137, Lane 235, Pac Chiao Rd.,
Hsin Tien City, Taipei Hsien, Taiwan, R. O. C.
Tel : 886-2-89191368
Fax : 886-2-89191369