AZP96

ARIZONA MICROTEK, INC.

ECL/PECL Differential Receiver

FEATURES

- Green and RoHS Compliant / Lead (Pb) Free Package available
- 250ps Propagation Delay
- High Bandwidth Output Transitions
- Operating Range of 3.0V to 5.5V
- Minimized Input Loading
- IBIS Model File Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free	AZP96NG	Q1G <Date Code>	1,2

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "Y" for year followed by "WW" for week.

DESCRIPTION

The AZP96 is a differential receiver without the input clamping networks found on similar devices such as the AZ100LVEL16. This makes it especially useful as a buffer when input loading effects must be minimized. Removal of the input clamping network means that the output state will be undefined if both inputs are left open.

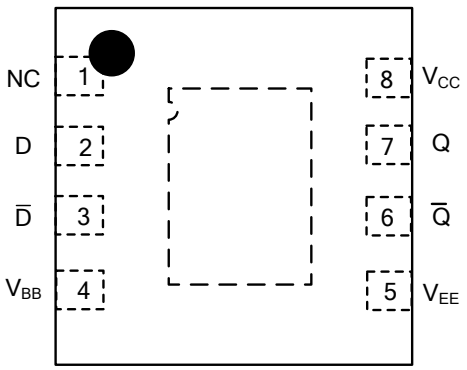
The AZP96 provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the D/$\overline{D}$ differential input pair. The input signal is then fed to the other D/$\overline{D}$ input. The V_{BB} pin can support 1.5 mA sink/source current. When used, the V_{BB} pin should be bypassed to ground via a 0.01 μF capacitor.

NOTE: Specifications in the ECL/PECL/LVPECL tables are valid when thermal equilibrium is established.

PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	Data Inputs
Q, $\overline{Q}$	Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

AZP96N
MLP 8, 2x2 mm



TOP VIEW

Bottom Center Pad may be left open or tied to V_{EE}.

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Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	PECL Power Supply (V_{EE} = 0V)	0 to +8.0	Vdc
V_I	PECL Input Voltage (V_{EE} = 0V)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply (V_{CC} = 0V)	-8.0 to 0	Vdc
V_I	ECL Input Voltage (V_{CC} = 0V)	-6.0 to 0	Vdc
I_{OUT}	Output Current --- Continuous --- Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage[1]	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Reference Voltage	-1380		-1260	-1380		-1260	-1380		-1260	-1380		-1260	mV
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{IH}	Input HIGH Current			50			50			50			50	µA
I_{EE}	Power Supply Current		18	22		18	22		18	22		18	24	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2295	2420	2275	2345	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1470	1605	1745	1490	1595	1680	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage[1]	2135		2420	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage[1]	1490		1825	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Reference Voltage[1]	1920		2040	1920		2040	1920		2040	1920		2040	mV
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{IH}	Input HIGH Current			50			50			50			50	µA
I_{EE}	Power Supply Current		18	22		18	22		18	22		18	24	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

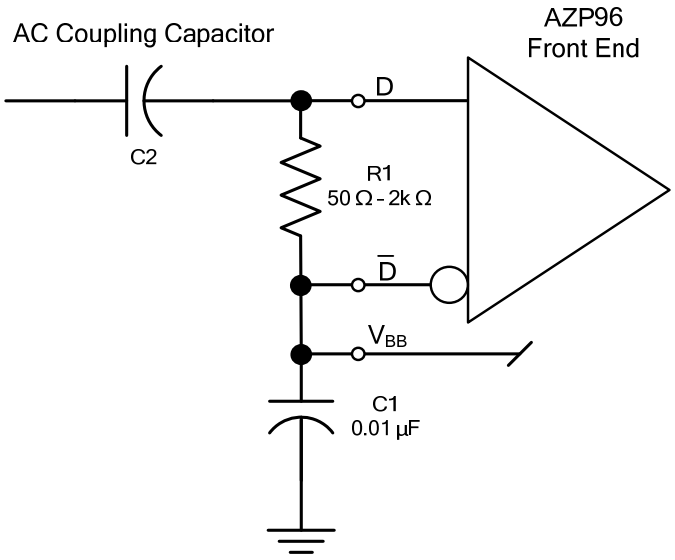
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage[1]	3835		4120	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage[1]	3190		3525	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Reference Voltage[1]	3620		3740	3620		3740	3620		3740	3620		3740	mV
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{IH}	Input HIGH Current			50			50			50			50	µA
I_{EE}	Power Supply Current		18	22		18	22		18	22		18	24	mA

1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC} = GND or V_{EE} = GND; V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay to Output (Diff)	125	250	375	175	250	325	175	250	325	205	280	355	ps
	(SE)	75	250	425	125	250	375	125	250	375	155	280	405	
t_{SKEW}	Duty Cycle Skew [1](Diff)		5			5	20		5	20		5	20	ps
V_{PP} (AC)	Minimum Input Swing[2]	150			150			150			150			mV
V_{CMR}	Common Mode Range[3]	V_{EE} +		V_{CC} -	V_{EE} +		V_{CC} -	V_{EE} +		V_{CC} -	V_{EE} +		V_{CC} -	V
	V_{PP} < 500mV	1.2		0.4	1.1		0.4	1.1		0.4	1.1		0.4	
	V_{PP} ≥ 500mV	1.5		0.4	1.4		0.4	1.4		0.4	1.4		0.4	
t_r / t_f	Output Rise/Fall Times Q (20% - 80%)	100		260	100		260	100		260	100		260	ps

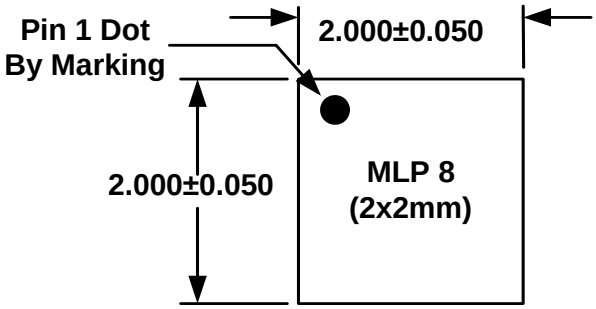
1. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
2. V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40.
3. The V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}(min) and 1V.



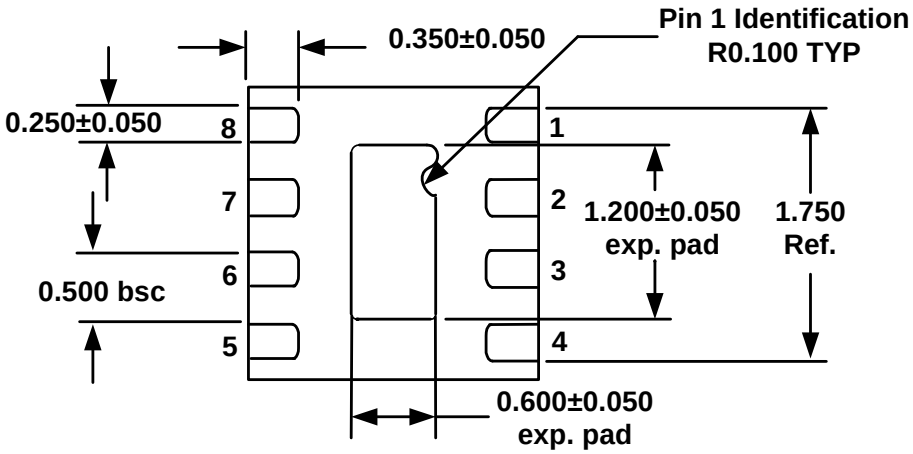
Recommended Circuit for Single-Ended Input Limiting Applications

AZP96

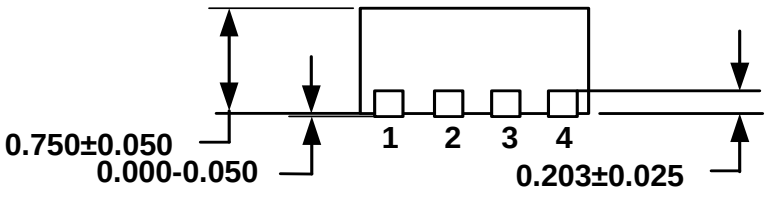
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm