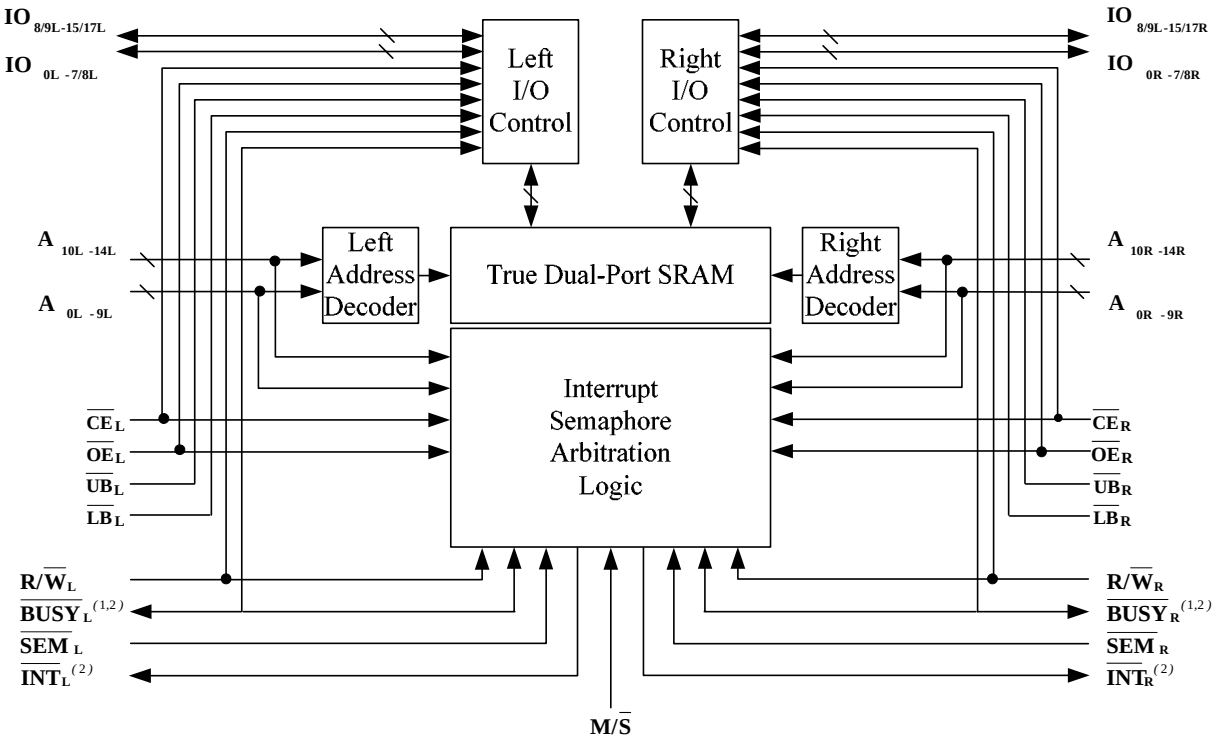
3.3V, 5V Asynchronous Dual-Port SRAM
1k/2k/4K/8K/16K/32K x 8/9/16/18-bit

Features

- True dual port memory cells up to 256/288Kb
- Fully asynchronous dual-port SRAM aimed at communications market
- Max. access time: 30 ns
- Separate upper byte and lower byte control for multiplexed bus compatibility (only for 16/18 bit devices)
- Supports byte write/read for 16/18 bit devices
- On-chip arbitration logic support 3 modes: Busy, Interrupt and Semaphore
  - Busy scheme circuit arbitrate between 2 ports
  - interrupt mechanism allow port to port communication
  - Full hardware support of semaphore to permit software handshaking between ports
- Versatile pin select for Master or Slave mode:
  $M/\overline{S} = V_{IH}$ for $\overline{BUSY}$ output flag on master; $M/\overline{S} = V_{IL}$ for $\overline{BUSY}$ input flag on slave
- Expandable data bus to 32/36 bits or more using master/slave chip select when using more than one device
- Separate upper-byte and lower-byte controls for bus matching (only for 16/18 bit devices)
- 3.3v and 5v series low power respectively
- Compatible and functionally equivalent to IDT or Cypress
- Available in 52-PLCC, 68-PLCC, 84-PLCC, 64-TQFP/STQFP, 80-TQFP, 100-TQFP

Architecture



Note 1: $\overline{LB}_R$ and $\overline{UB}_R$ are for 16/18 bit devices only.
Note 2: $I/O_{0\sim7}$ for 8/16 bit devices, $I/O_{0\sim8}$ for 9/18 bit devices, $I/O_{8\sim15}$ for 16 bit devices, and $I/O_{9\sim17}$ for 18 bit devices.
Note 3: $A_{0\sim9}$ for 1K, $A_{0\sim10}$ for 2K, $A_{0\sim11}$ for 4K, $A_{0\sim12}$ for 8K, $A_{0\sim13}$ for 16K, $A_{0\sim14}$ for 32K devices

Function Description

The asynchronous dual-port SRAMs allow fully independent access to any memory location from both ports without the need of an additional discrete logic. There are separate address, data and control signals for each port. They can be utilized as either a standalone 8/9/16/18-bit dual-port static RAM or as a MASTER/SLAVE cascade form in systems requiring 32/36-bit or greater word widths through pin $\mathbf{M/\overline{S}}$. Master and slave devices provide two independent ports with separate control, address and I/O pins that permit independent, error-free and asynchronous access for reads and writes to any location in the memory. It is the solution for applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs. Each port has independent control pins; chip enable ($\overline{\mathbf{CE}}$), write enable ($\mathbf{R/\overline{W}}$), and output enable ($\overline{\mathbf{OE}}$). In addition, a Busy, Interrupt or Semaphore logic may be provided to block the port trying to access the same cell location currently being accessed by the other port. The **AL5DAxxxx** series are high speed asynchronous CMOS dual-port SRAMs configured as

- 1K/2K x 8-bit organization (AL5DA002/3; Master; Busy Interrupt;3.3V or 5.V)
- 2Kx8-bit organization (AL5DA132; Master; Busy; 3.3V or 5.V)
- 4Kx8-bit organization (AL5DA134; 3.3V or 5.V)
- 4Kx8-bit organization (AL5DA004; Semaphore; 3.3V or 5.V)
- 4Kx8-bit organization (AL5DA138; Master/Slave; Busy Interrupt Semaphore; 3.3V or 5.V)
- 8K/16K/32Kx8-bit organization (AL5DA005/6/7; Master/Slave; Busy Interrupt Semaphore; 3.3V or 5.V)
- 2Kx9-bit organization (AL5DA013; Master; Busy Interrupt; 3.3V or 5.V)
- 4Kx9-bit organization (AL5DA139; Master/Slave; Busy Interrupt Semaphore; 3.3V or 5.V)
- 8K/16K/32Kx9-bit organization (AL5DA015/6/7; Master/Slave; Busy Interrupt Semaphore; 3.3V or 5.V)
- 2Kx16-bit organization (AL5DA023; Master; Busy; 3.3V or 5.V)
- 4K/8K/16Kx16-bit organization (AL5DA024/5/61; Master/Slave; Busy Interrupt Semaphore; 3.3V or 5.V)
- 16Kx16-bit organization (AL5DA026; Master/Slave; Busy Semaphore; 3.3V or 5.V)
- 4K/8K/16Kx18-bit organization (AL5DA034/5/6; Master/Slave; Busy Interrupt Semaphore, 3.3V or 5.V)
- 1Kx8-bit organization (AL5DA140; Slave; Busy Interrupt; 3.3V or 5.V)
- 2Kx8-bit organization (AL5DA142; Slave; Busy; 3.3V or 5.V)
- 2Kx8-bit organization (AL5DA421; Slave; Busy Interrupt; 3.3V or 5.V)
- 2Kx9-bit organization (AL5DA125; Slave; Busy Interrupt; 3.3V or 5.V)
- 2Kx16-bit organization (AL5DA143; Slave; Busy; 3.3V or 5.V)

For more information regarding **AL5DAxxxx** asynchronous Dual-Port SRAM or other AverLogic products, please contact us, your local authorized representatives or visit our web site.

Applications

- Cellular Base Stations
- Multi-protocol Routers
- Internet Appliance
- ATM
- Ethernet
- LAN/WAN Switches
- Hubs
- PBXs
- RAIDs (Storage Networks)
- Set-top Boxes
- Video Conferencing
- Graphics Accelerators
- Audio/Video Editing
- Ultrasound Imaging
- Satellite Encoders
- Cable Modems
- Flight Simulators
- High-end Printing Servers
- Call Distribution Systems
- Fiber Channel Line Boards
- Aerospace Instrumentation
- Industrial Controls
- Any circuit where data must be passed between different processors

AverLogic Technologies Corp.
E-mail: sales@averlogic.com.tw
URL: http://www.averlogic.com.tw

AverLogic Technologies, Inc.
E-mail: sales_usa@averlogic.com
URL: http://www.averlogic.com

