AK7740ET

24bit 2ch ADC + 24bit 4ch DAC with Audio DSP

1. General Description

The AK7740 is a highly integrated audio processing IC, including four 24-bit output D/A channels, a stereo 24-bit input A/D, and an audio DSP. High quality analog output performance is provided by the quad DAC with 97dB dynamic range, and the stereo ADC with 98dB dynamic range. The converters support sampling frequencies from 32kHz to 48kHz. This device includes 72kbits of SRAM audio delay that is suitable for simulated sound fields. The DSP is optimized for audio signal processing. The design allows up to 512 execution lines per audio sample cycle, with multiple functions per line. The AK7740 is ideal for sound field control applications, including echo, 3D, parametric equalization, and speaker compensation. It is housed in a 48-lead LQFP package.

2. Features

DSP:

- **Word length: 24-bit (Data RAM)**
- **Instruction cycle time: 40ns (512fs, fs=48kHz)**
- **Multiplier: 24 x 16 → 40-bit**
- **Divider: 24 / 24 → 16-bit or 24-bit**
- **ALU: 34-bit arithmetic operation (overflow margin: 4-bits)**
- **24-bit arithmetic and logic operation**
- **Shift+Register: 1, 2, 3, 4, 6, 8 and 15 bits shifted left**
- **1, 2, 3, 4, 8 , 14 and 15 bits shifted right**
- **Other numbers in parentheses are restricted. Provided with indirect shift function**
- **Program RAM: 512 x 32-bit**
- **Coefficient RAM: 512 x 16-bit**
- **Data RAM: 256 x 24-bit**
- **Offset RAM: 48 x 13-bit**
- **(6144 x 12-bit / 3072 x 24-bit / 4096 x 12-bit + 1024 x 24-bit)**
- **Internal Memory: 72kbit SRAM**
- **Sampling frequency: 32kHz to 48kHz**
- **Serial interface port for micro-controller**
- **Master clock: 512fs**
- **Master/Slave operation**
- **Serial signal input port (2 to 4 ch): 16/20/24-bit : Output port (2 ch): 24-bit**

ADC: 2 channels

- **24-bit 64x over-sampling delta sigma**
- **DR, S/N : 98dBA (full-differential Input)**
- **S/(N+D) : 89dB**
- **Digital HPF (fc = 1Hz)**
- **Single-ended or full-differential Input**

DAC: 4 channels

- **24-bit 128x over-sampling advanced multi-bit**
- **DR, S/N : 97dBA**
- **S/(N+D) : 89dB**
- **Single ended or differential output**

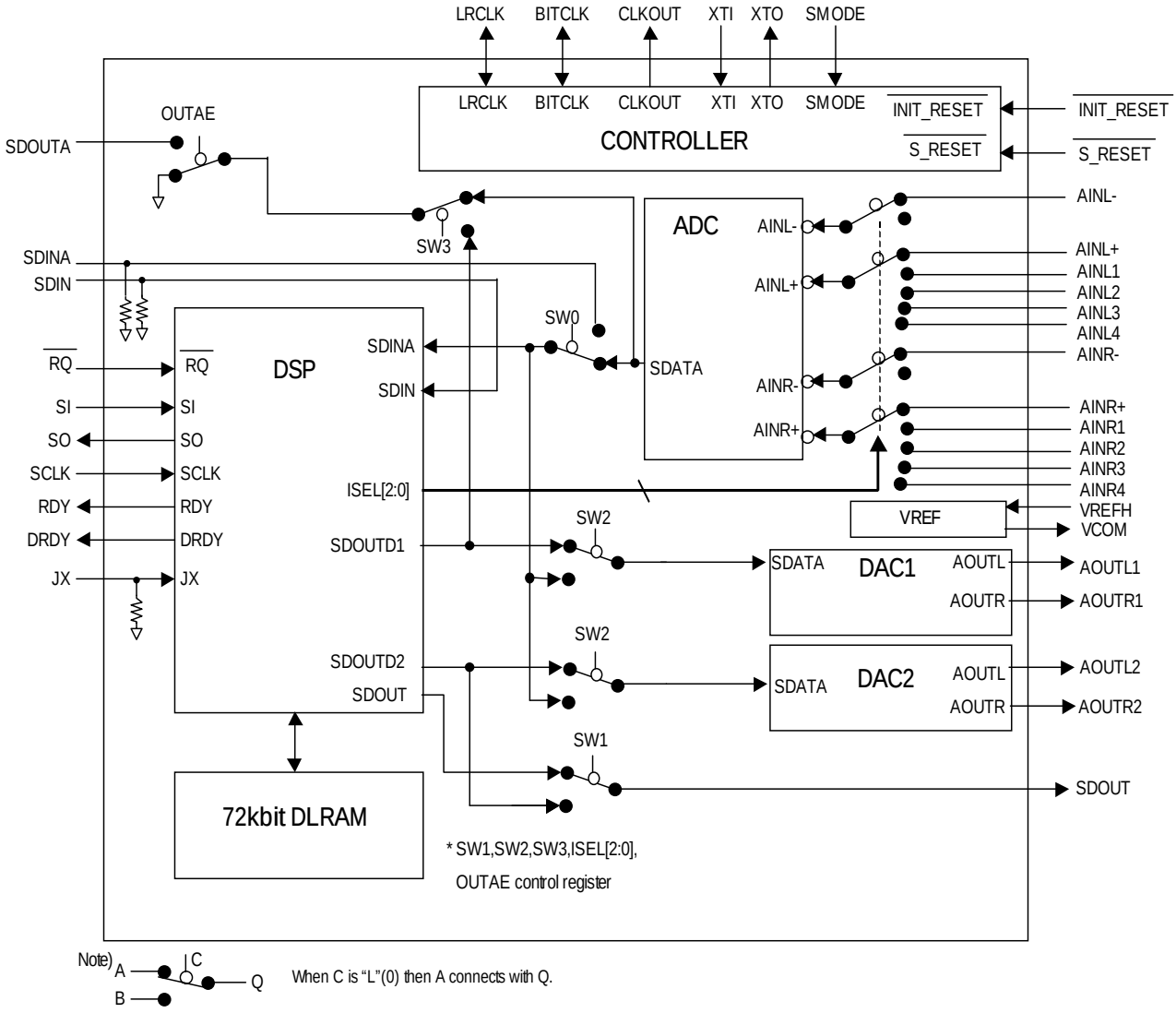
Input Selector

- **1 full-differential and 4 single-ended Input**

Other

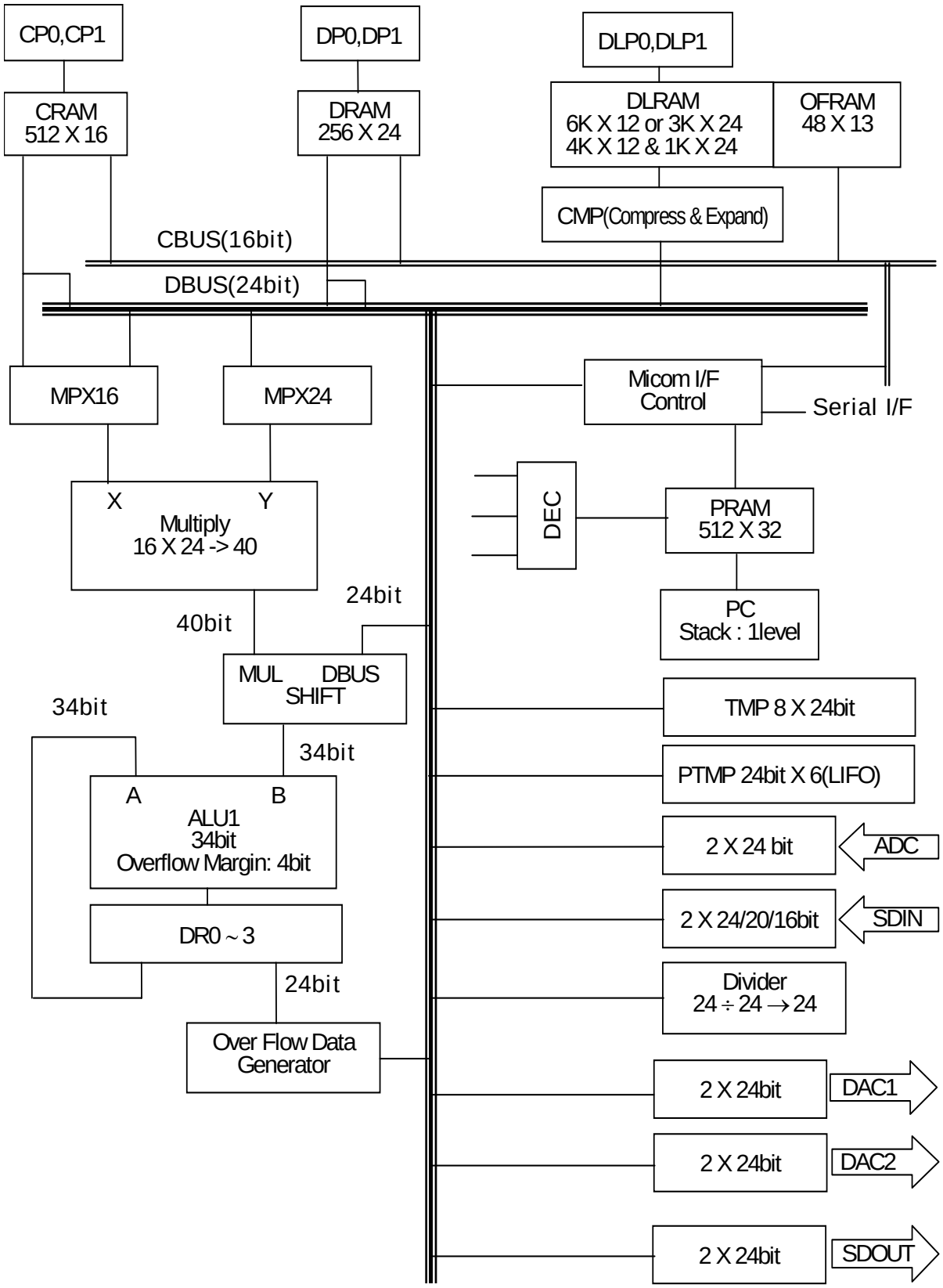
- **Power supply: +3.3V±10%**
- **Operating temperature range: -10°C~70°C**
- **Package: 48pin LQFP (0.5mm pitch)**

3. Block diagram



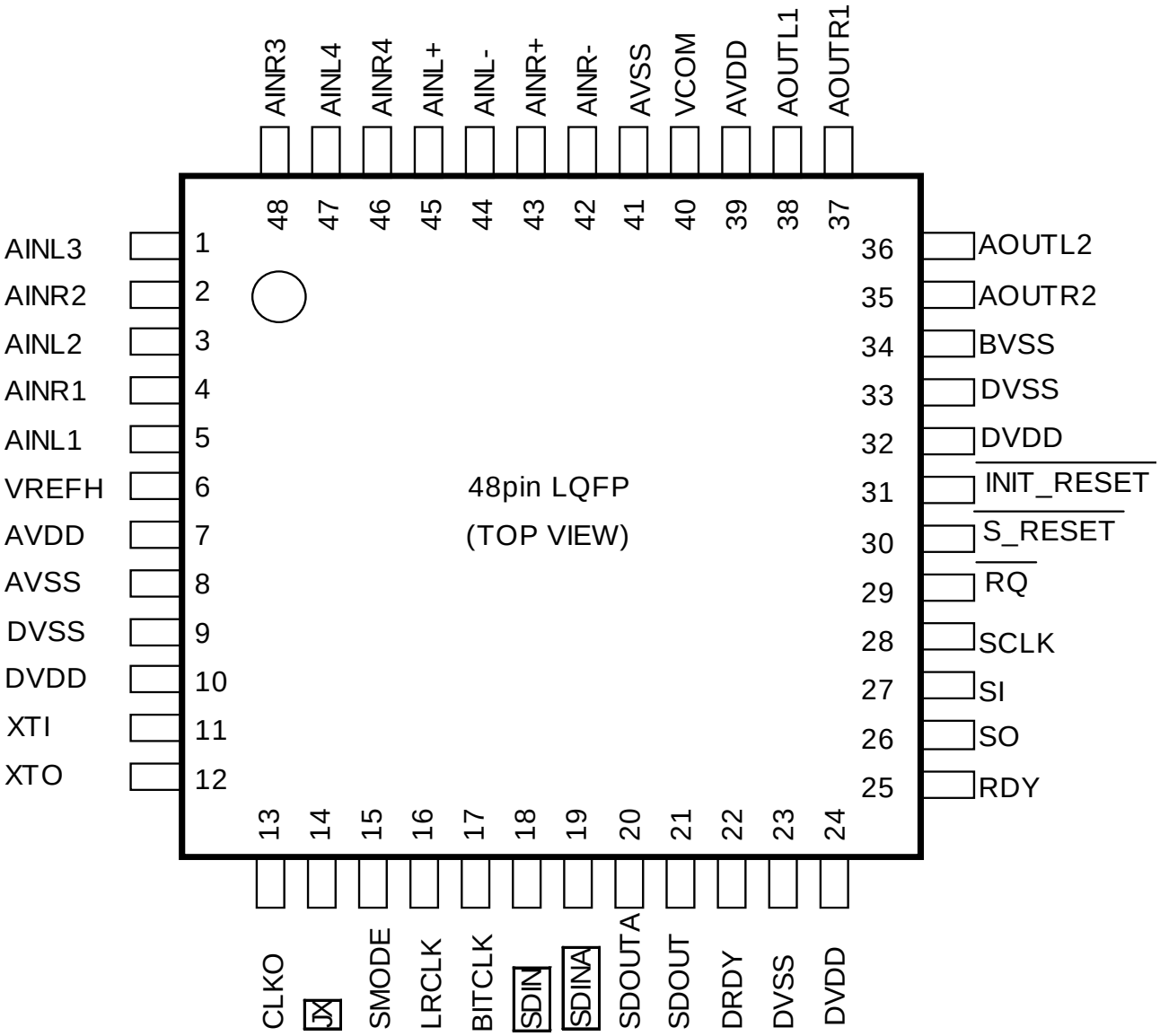
This block diagram is a simplified illustration of the AK7740; it is not a circuit diagram.

◆ **AK7740 DSP Block diagram**



4. Description of Input/Output Pins

(1) Pin layout



Note) JX, SDIN and SDINA are Pull-down pins

(2) Pin function

Pin No.	Pin name	I/O	Function	Classification
1	**AINL3**	I	**ADC single-ended analog Lch input pin 3**	Analog section
2	**AINR2**	I	**ADC single-ended analog Rch input pin 2**	
3	**AINL2**	I	**ADC single-ended analog Lch input pin 2**	
4	**AINR1**	I	**ADC single-ended analog Rch input pin 1**	
5	**AINL1**	I	**ADC single-ended analog Lch input pin 1**	
6	**VREFH**	I	**Analog reference voltage input** Connect to AVDD (pin 7), and bypass with 0.1uF and 10uF capacitors between this pin and AVSS.	
7	**AVDD**	-	**Analog power supply 3.3V typical**	Analog Power Supply
8	**AVSS**	-	**Analog ground**	
9	**DVSS**	-	**Digital ground**	Digital Power Supply
10	**DVDD**	-	**Digital power supply 3.3V typical**	
11	**XTI**	I	**Master clock input** Connect a crystal oscillator between this pin and the XTO pin, or input an external CMOS clock signal to the XTI pin.	System clock
12	**XTO**	O	**Crystal oscillator output** When a crystal oscillator is used, connect between XTI and XTO. When an external clock is used, keep this pin open	
13	**CLKO**	O	**Clock output** Outputs the XTI clock. Allows the output to be set to "L" by control register setting.	System clock
14	**JX**	I	**External condition jump (pulldown)**	Condition input
15	**SMODE**	I	**Slave/master mode selector** Sets LRCLK and BITCLK to input or output mode. SMODE="L": Slave mode (clock input mode) SMODE="H": Master mode (clock output mode)	Control
16	**LRCLK**	I/O	**LR channel select clock** SMODE="L": Slave mode: Inputs the fs clock SMODE="H": Master mode: Outputs the fs clock	System clock
17	**BITCLK**	I/O	**Serial bit clock** SMODE="L": Slave mode: Inputs 64 fs or 48 fs clocks SMODE="H": Master mode: Outputs 64 fs clocks	
18	**SDIN**	I	**DSP serial data input (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits.	Digital section Serial input data
19	**SDINA**	I	**DSP serial data input (Pulldown)** When using the ADC, leave open or connect to DVSS. Compatible with MSB justified 24 bits.	

Pin No.	Pin name	I/O	Function	Classification
20	**SDOUTA**	O	**DSP serial data output** Outputs MSB justified 24-bit data selected from ADC or SDOUTD1 by control register setting	Digital section Serial output data
21	**SDOUT**	O	**DSP serial data output** Outputs MSB justified 24-bit data	
22	**DRDY**	O	**Output data ready pin for microcontroller interface**	Microcontroller interface
23	**DVSS**	-	**Digital ground**	Power supply
24	**DVDD**	-	**Digital power supply 3.3V typical**	
25	**RDY**	O	**Data write ready output for microcontroller interface**	Microcontroller interface
26	**SO**	O	**Serial data output for microcontroller interfaces**	
27	**SI**	I	**Microcontroller interface serial data input and serial data output control** When SI does not use, leave SI="L"	
28	**SCLK**	I	**Microcontroller interface serial data clock** When SCLK is not used, leave SCLK="H"	
29	**$\overline{\text{RQ}}$**	I	**Microcontroller interface writes request pin.** $\overline{\text{RQ}}$ ="L": Microcontroller interface enable	
30	**$\overline{\text{S\_RESET}}$**	I	**System Reset**	Reset
31	**$\overline{\text{INIT\_RESET}}$**	I	**Reset (for initialization)** Input "L" to initialize the AK7740 at power-on	
32	**DVDD**	-	**Digital power supply 3.3V typical**	Power supply
33	**DVSS**	-	**Digital ground**	
34	**BVSS**	-	**Substrate ground**	Power supply
35	**AOUTR2**	O	**DAC2 Rch analog output**	Analog section
36	**AOUTL2**	O	**DAC2 Lch analog output**	
37	**AOUTR1**	O	**DAC1 Rch analog output**	
38	**AOUTL1**	O	**DAC1 Lch analog output**	
39	**AVDD**	-	**Analog power supply 3.3V typical**	Power supply
40	**VCOM**	O	**Common voltage** Connect to 0.1uF and 10uF capacitors between this pin and AVSS. Do not connect to external circuitry	Analog section
41	**AVSS**	-	**An alog ground**	Power supply
42	**AINR-**	I	**ADC Rch analog inverted input**	Analog section
43	**AINR+**	I	**ADC Rch analog non-inverted input**	
44	**AINL-**	I	**ADC Lch analog inverted input**	
45	**AINL+**	I	**ADC Lch analog non-inverted input**	
46	**AINR4**	I	**ADC single-ended analog Rch input 4**	
47	**AINL4**	I	**ADC single-ended analog Lch input 4**	
48	**AINR3**	I	**ADC single-ended analog Rch input 3**	

5. Absolute Maximum Rating

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground)

Item	Symbol	min	max	Unit
Power supply voltage				
Analog (AVDD)	VA	-0.3	4.6	V
Digital (DVDD)	VD	-0.3	4.6	V
|AVSS (BVSS)-DVSS| Note 1)	ΔGND		0.3	V
Input current (except for power supply pin)	IIN	-	±10	mA
Analog input voltage AINL+,AINL-,AINR+,AINR-,AINL1, AINR1,AINL2,AINR2,AINL3,AINR3, AINL4,AINR4,VREFH	VINA	-0.3	VA+0.3	V
Digital input voltage	VIND	-0.3	VD+0.3	V
Operating ambient temperature	Ta	-10	70	°C
Storage temperature	Tstg	-65	150	°C

Note 1) AVSS(BVSS) should be at the same level as DVSS

WARNING: Operation at or beyond these limits may result in permanent damage of the device.
Normal operation is not guaranteed when these limits are exceeded

6. Recommended Operating Conditions

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Items	Symbol	min	typ	max	Unit
Power supply voltage					
AVDD	VA	3.0	3.3	3.6	V
DVDD	VD	3.0	3.3	VA	V
Reference voltage (VREF)					
VREFH Note 1)	VRH		VA		V

Note 1) VREFH normally connects to AVDD.

Note: The analog input voltage and output voltage are proportional to VREFH voltage.

7. Electric Characteristics

(1) Analog characteristics

(Unless otherwise specified, Ta = 25°C; AVDD, DVDD = 3.3V; VREFH = AVDD;
BITCLK = 64 fs; Signal frequency 1kHz;
Measurement bandwidth = 20Hz to 20kHz @ 48kHz;
DSP section in reset state; ADC with all differential inputs)

	Parameter	Min	Typ	Max	Unit
ADC Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (-1dB) (Note1)	80	89		dB
	Dynamic range fs = 48kHz (A filter) (Note2)	90	98		dB
	S/N fs = 48kHz (A filter)	90	98		dB
	Inter-channel isolation (f =1kHz) (Note3)	90	110		dB
	DC accuracy				
	Inter-channel gain mismatching		0.1	0.3	dB
	Analog input				
	Input voltage (Differencial) (Note4)	±1.85	±2.00	±2.15	Vp-p
	Input Voltage (Single-ended) (Note5)	1.85	2.00	2.15	Vp-p
	Input impedance (Note6)	15	33		kΩ
DAC Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (0dB)	80	89		dB
	Dynamic range fs = 48kHz (A filter) (Note2)	90	97		dB
	S/N fs = 48kHz (A filter)	90	97		dB
	Inter-channel isolation (f =1kHz) (Note7)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching (Note7)		0.2	0.5	dB
	Analog output				
	Output voltage (Note8)	1.85	2.00	2.15	Vp-p
	Load resistance	10			kΩ

Note:

1. Specification only guaranteed for differential inputs
2. Indicates S/(N+D) when -60dB signal is applied
3. Specified for L and R of each input selector
4. Applies to AINL+, AINL-, AINR+ and AINR-
   Fullscale (ΔAIN = (AIN+) - (AIN-)) can be represented by (±FS = ±(VREFH-AVSS)×(2.0/3.3))
5. Applies to AINL1,AINR1,AINL2,AINR2,AINL3,AINR3,AINL4 and AINR4
   Fullscale single-ended input is (FS=(VREFH-AVSS) × (2.0/3.3))
6. Applies to AINL1, AINR1, AINL2, AINR2, AINL3, AINR3, AINL4, AINR4, AINL+, AINL-, AINR+ and AINR-
7. Specified for L and R of each DAC.
8. Fullscale output voltage when VREFH=AVDD

(2) DC characteristics

(VDD=AVDD=DVDD=3.0~3.6V,Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
High level input voltage	VIH	80%VDD			V
Low level input voltage	VIL			20%VDD	V
High level output voltage Iout=-100μA	VOH	VDD-0.5			V
Low level output voltage Iout=100μA	VOL			0.5	V
Input leak current Note 1)	Iin			±10	μA
Input leak current (pull-down) Note 2)	Iid		22		μA
Input leak current (XTI pin)	Iix		24		μA

Note:

1. Pins with pull-down resistors and the XTI pin are not included
2. Pull-down pins are JX, SDIN and SDINA. The pull-down resistor value is 156kΩ
3. For input/output levels in this datasheet: the low level will be represented as "L" or 0, and the high level as "H" or 1. In principle, "0" and "1" will be used to represent the bus (serial/parallel) such as registers.

(3) Current consumption

(AVDD=DVDD=3.0V~3.6V, Ta=25°C; master clock (XTI)=24.576MHz=512fs[fs=48kHz];
When operating 4 DAC channels with a 1kHz sine wave full-scale input to each of ADC analog input pin)

Power supply					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Power supply current					
1) During operation					
a) AVDD			34		mA
b) DVDD	Note 1)		31		mA
c) Total (a+b)			65	90	mA
2) $\overline{\text{INIT\_RESET}}$ ="L"	Note 2)		5		mA
Power consumption					
1)During operation					
a) AVDD			112		mW
b) DVDD	Note 1)		102		mW
c) Total (a+b)			214	324	mW
2) $\overline{\text{INIT\_RESET}}$ ="L"	Note 2)		17		mW

Note:

1) Varies slightly depending on sampling frequency and the content of the DSP program.
2) This is a reference value when using a crystal oscillator. Most of the supply current during the initial reset state is in the oscillator section; the value varies slightly depending on the type of crystal oscillator and external circuit.

(4) Digital filter characteristics

Values described below are design values, cited for reference.

4-1) ADC Section:

(Ta=25°C; AVDD,DVDD =3.0V~3.6V; fs=48kHz; HPF=off)

Parameter	Symbol	Min	Typ	Max	Unit
Pass band (-0.02dB)	PB	0		21.768	kHz
(-6.0dB)		0	24.00		kHz
Stop band (Note 1)	SB	26.5			kHz
Pass band ripple (Note 2)	PR			±0.005	dB
Stop band attenuation (Note3,4)	SA	80			dB
Group delay distortion	ΔGD			0	us
Group delay (Ts=1/fs)	GD		29.3		Ts

Note: : HPF response is not included

1. The stop band is from 26.5kHz to 3.0455MHz when fs = 48kHz.
2. The pass band is from DC to 21.5kHz from DC when fs = 48kHz.
3. When fs = 48kHz, the modulator samples the analog input at 3.072MHz. The input signal is not attenuated by the digital filter in multiple bands (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3...) of the sampling frequency.

4-2) DAC section

(Ta=25°C; AVDD,DVDD =3.0V~3.6V; fs=48kHz)

Parameter	Symbol	Min	Typ	Max	Unit
Digital filter					
Pass band ±0.07dB (Note 1)	PB	0		21.7	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 1)	SB	26.2			kHz
Pass band ripple	PR			±0.07	dB
Stop band attenuation	SA	47			dB
Group delay (Note 2)	GD	-	15		Ts
Digital filter+SCF					
Amplitude characteristics 0~20.0kHz			±0.5		dB

Note:

1. Pass band and stop band frequencies are proportional to "fs" (system sampling rate), and are equal to PB = 0.4535fs (@-0.06dB) and SB = 0.546fs, respectively.
2. Calculated delay time in the digital filter from setting the 24-bit data of both channels on the input data register to the output of analog signal.

(5) Switching characteristics

5-1) System clock

(AVDD=DVDD=3.0V~3.6V,Ta=-10~70°C,CL=20pF)

Parameter	Symbol	Min	Typ	Max	Unit
Master clock (XTI)					
a) With crystal oscillator					
384fs: frequency	fMCLK	12.288	18.432	19	MHz
512fs: frequency	fMCLK	16.384	24.576	25	MHz
b) With external clock:					
Duty factor (≤18.432MHz) (>18.432MHz)		40 45	50 50	60 55	%
:Frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	10.0 16 16	24.576	25	MHz ns ns
Clock rise time Clock fall time	tCR tCF			6 6	ns ns
LRCLK sampling frequency	fs	32	48 1	50	kHz fs
Slave mode :clock rise time Slave mode :clock fall time	tLR tLF			6 6	ns ns
BITCLK Note 1)	fBCLK	48	64		fs
Slave mode: High level width Slave mode: Low level width	tBCLKH tBCLKL	150 150			ns ns
Slave mode :clock rise time Slave mode :clock fall time	tBR tBF			6 6	ns ns

Note 1) 48fs mode can only be applied in slave mode.

5-2) Reset

(AVDD=DVDD=3.0V~3.6V,Ta=-10~70°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
$\overline{\text{INIT\_RESET}}$ Note 1)	tRST	150			ns
$\overline{\text{S\_RESET}}$	tRST	150			ns

Note 1) "L" is acceptable when power is turned on, but "H" requires a stable master clock input.

5-3) Audio interface

(AVDD=DVDD=3.0V~3.6V,Ta=-10~70°C,CL=20pF)

Parameter	Symbol	Min	Typ	Max	Unit
Slave mode					
BITCLK frequency	fBCLK	48	64		fs
BITCLK low level width	tBCLKL	150			ns
BITCLK high level width	tBCLKH	150			ns
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK "↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			80	ns
Delay time from BITCLK to serial data output	tBSOD			80	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns
Master mode					
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		%
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK"↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			80	ns
Delay time from BITCLK to serial data output	tBSOD			80	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns

5-4) Microcontroller interface

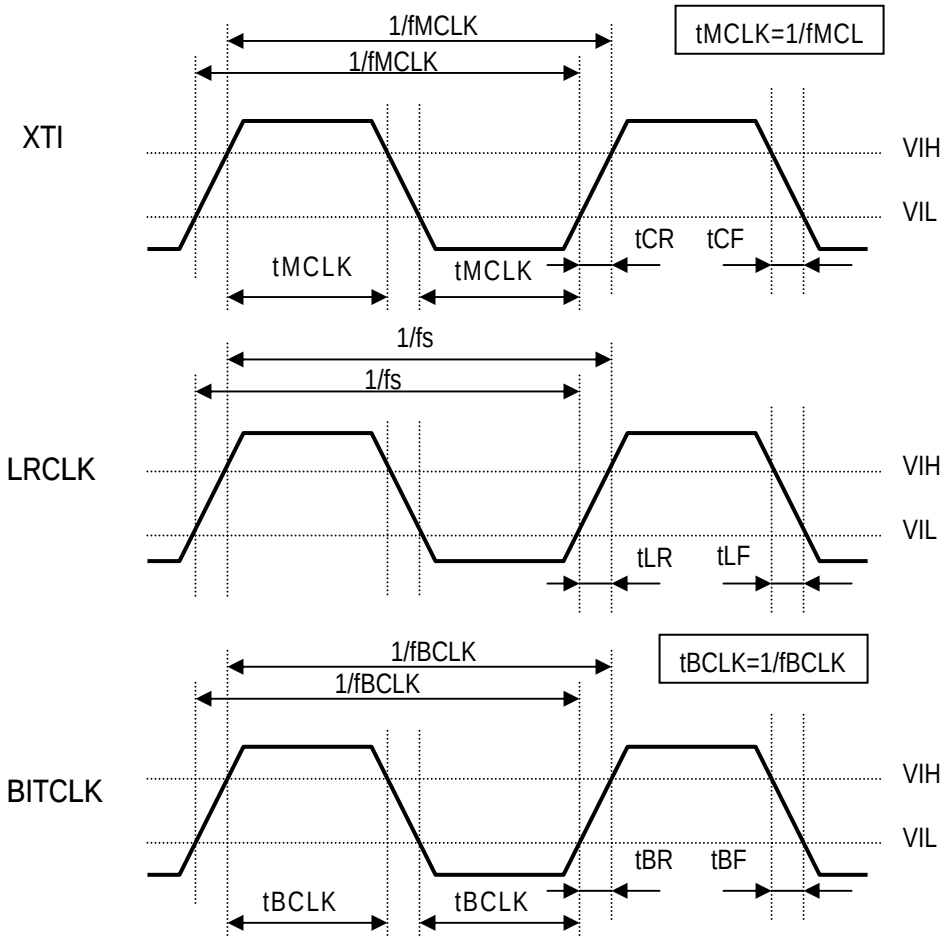
(AVDD=DVDD=3.0V~3.6V,Ta=-10~70°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcontroller interface signal					
$\overline{RQ}$ Fall time	tWRF			8	ns
$\overline{RQ}$ Rise time	tWRR			8	ns
SCLK fall time	tSF			8	ns
SCLKrise time	tSR			8	ns
SCLK low level width	tSCLKL	30			ns
SCLK high level width	tSCLKH	30			ns
Microcontroller to AK7740					
Time from $\overline{RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	200			ns
Time from $\overline{RQ}$ "↑" to $\overline{RESET}$ "↑" Note 1)	tWRE	200			ns
$\overline{RQ}$ high level width	tWRQH	200			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	200			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	6×tMCLK			ns
SI latch setup time	tSIS	100			ns
SI latch hold time	tSIH	100			ns
AK7740 to microcontroller					
Time from SCLK"↑" to DRDY"↓"	tSDR			3×tMCLK	ns
Time from SI"↑"to DRDY"↓"	tSIDR			3×tMCLK	ns
SI high level width	tSIH	3×tMCLK			ns
Delay time from SCLK"↓" to SO output	tSOS			100	ns
AK7740 to microcontroller (RAM DATA read-out)					
SI latch setup time (SI="H")	tRSISH	30			ns
SI latch setup time (SI="L")	tRSISL	30			ns
SI latch hold time	tRSIH	30			ns
Time from SCLK"↓" to SO	tSOD			100	ns

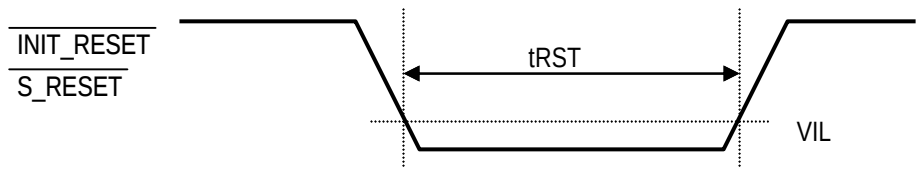
Note 1) Except for external jump code set at reset state.

(6) Timing waveform

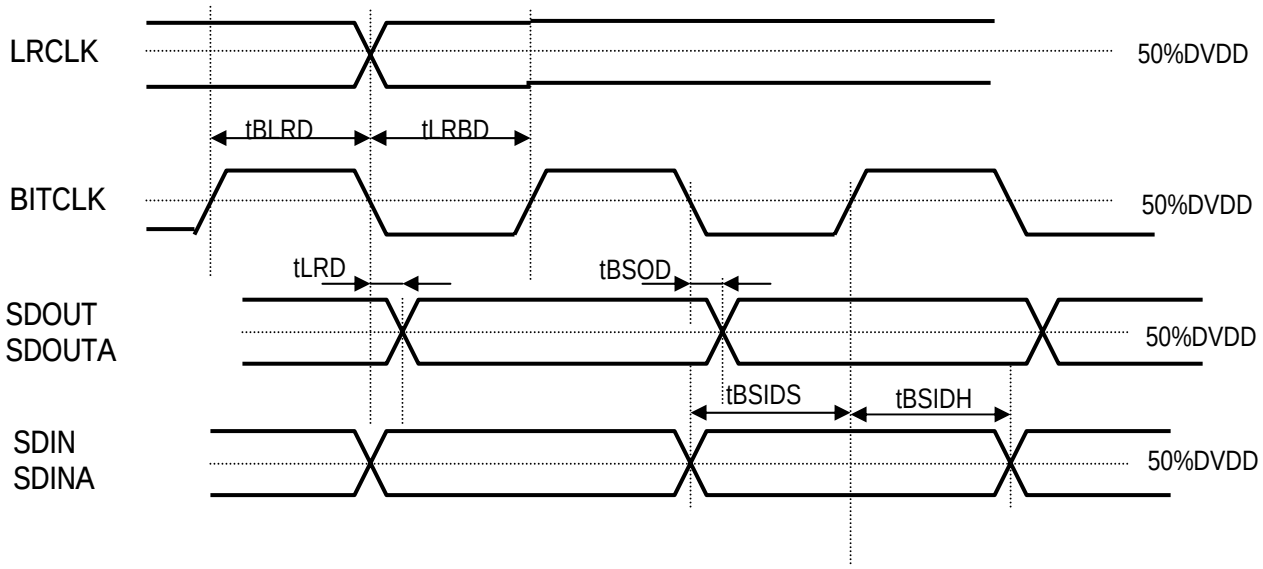
6-1) System clock



6-2) Reset signal

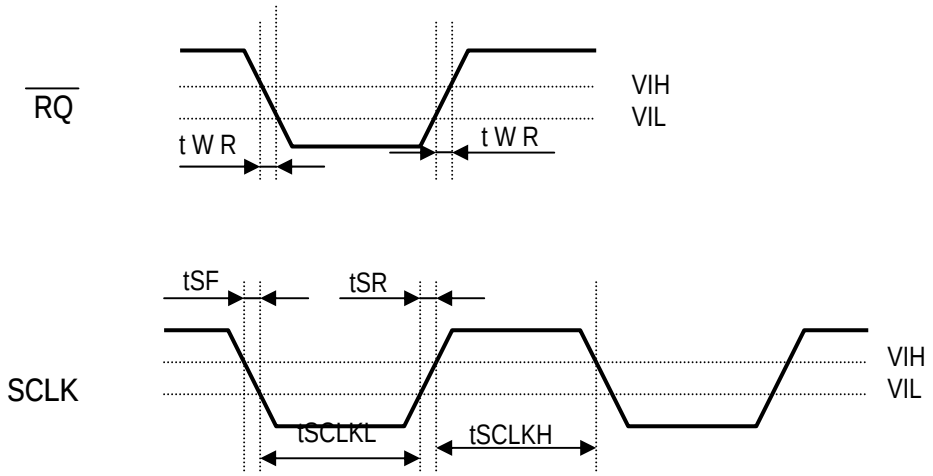


6-3) Audio interface

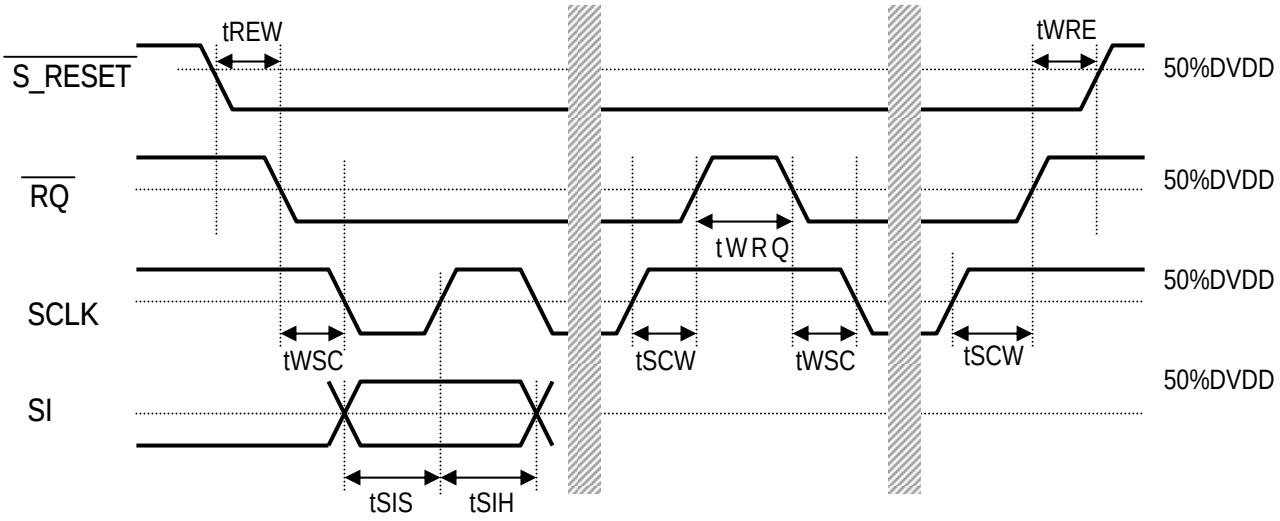


6-4) Microcontroller interface

* Microcontroller interface signals



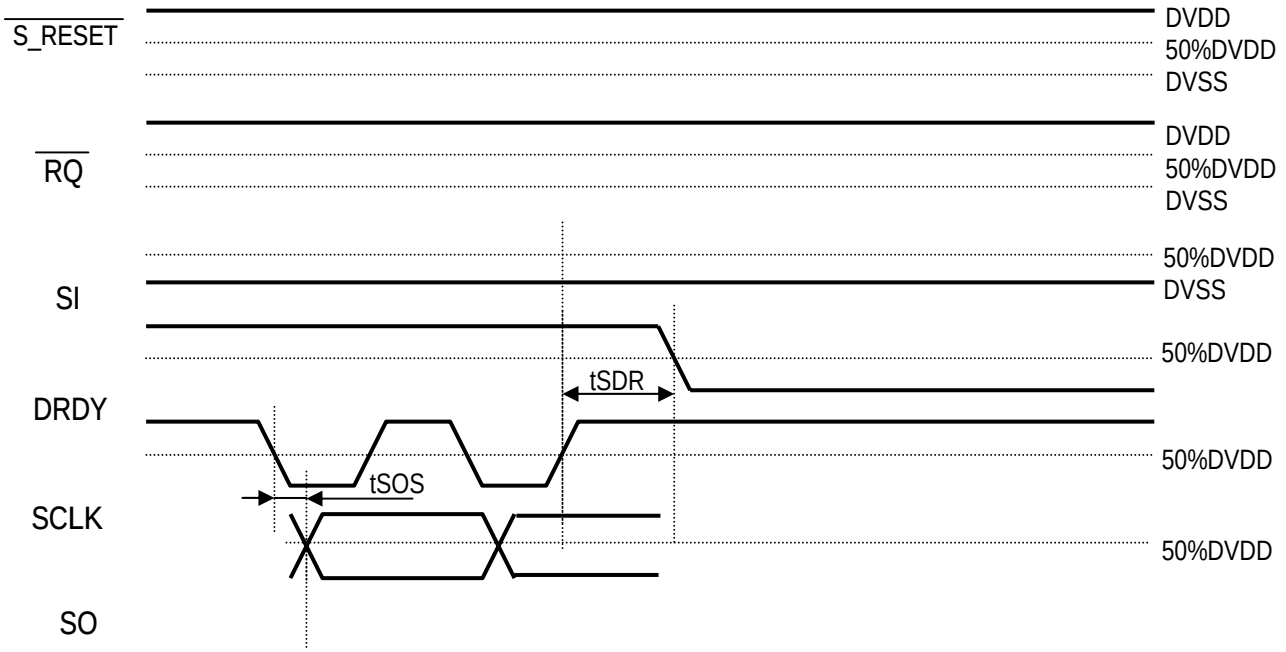
* Microcontroller to AK7740



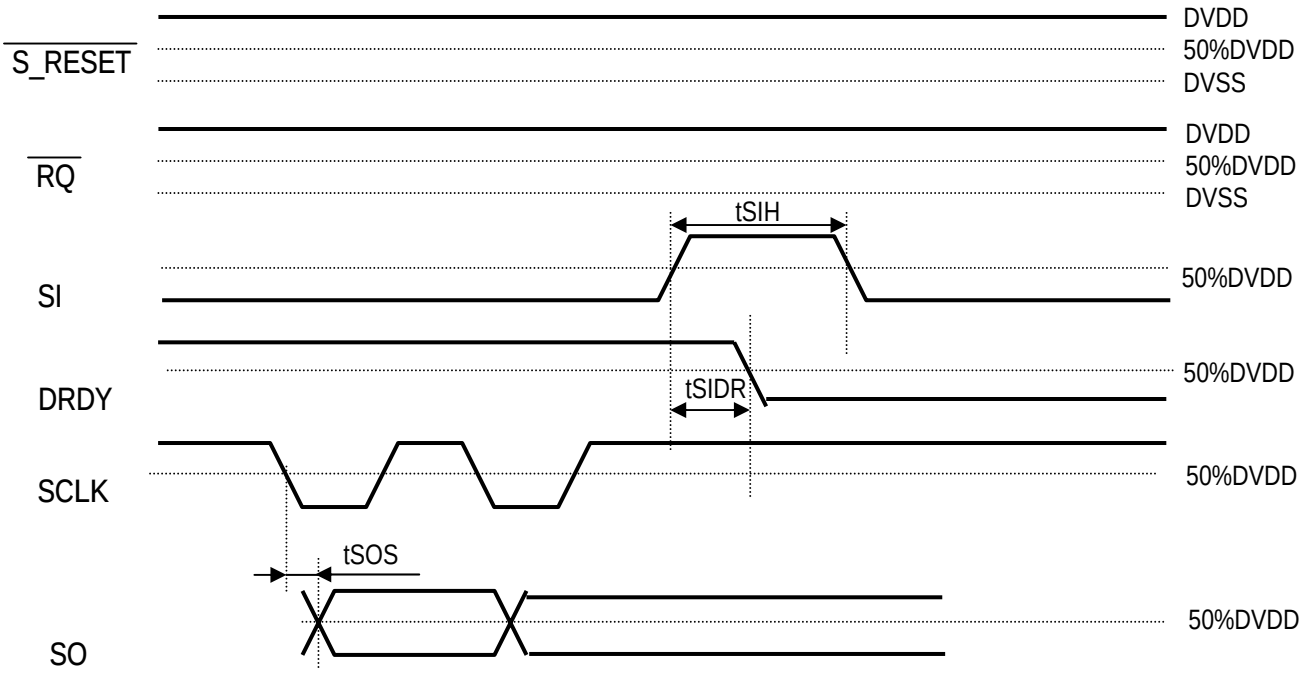
NOTE : Timing for RUN state is the same except that $\overline{\text{RESET}}$ is set to a "H"
$\overline{\text{RESET}}$ represents system reset in normal use.

- AK7740 to microcontroller (DBUS data)

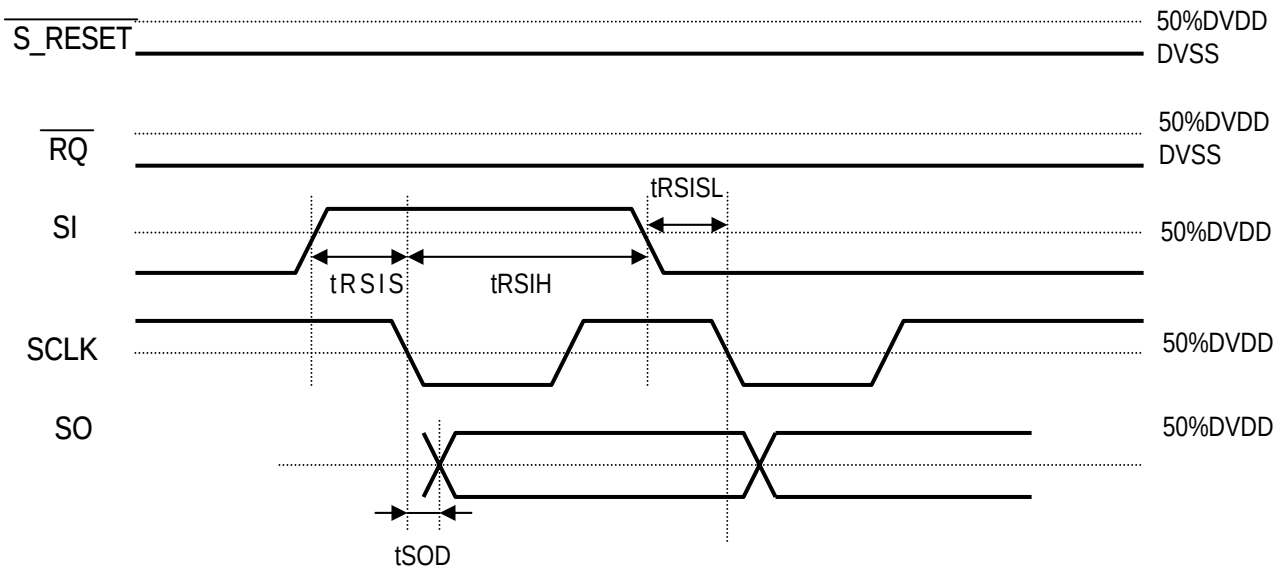
1) DBUS data for 24-bit data output.



2) DBUS data for less than 24-bits data output (when using SI)



- AK7740 to microcontroller (RAM DATA read-out)



Functional Description

(1) Various setting

1-1) SMODE : slave and master mode selector pin

Sets LRCLK and BITCLK to either input or output.

a) Slave mode :SMODE="L" LRCLK (1fs) and BITCLK (64fs or 48fs) are inputs.

b) Master mode: SMODE="H" LRCLK (1fs) and BITCLK (64fs) are outputs.

Note) SMODE is required to be fixed “L” or “H”. After releasing initial reset ($\overline{\text{INIT\_RESET}}$ =”L”→”H”), this pin may only change during a system reset state ($\overline{\text{S\_RESET}}$ ="L") . In slave mode, phase matching between internal and external clocks start when system reset is released (see (8.(4)), resetting). **Do not change SMODE** during normal operation.

(2) Control registers

The control registers can be set via the microcontroller interface in addition to the control pins.These registers consist of four parts, and each register contains 8-bits. For details about writing to the control registers, see the description of the microcontroller interface.This section describes the control register maps.

TEST: for TEST (input 0,X: input data ignored, but a 0 should be written).

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	CKS1	CKS0	DIF	DIF1	DIF0	DISCK	SELCKO	X	00h
64h	74h	CONT1	DATARAM	RM	BANK[1]	BANK[0]	CMP_N	SS[1]	SS[0]	X	00h
68h	78h	CONT2	SW2	SW1	SW0	PSDA2	PSDA1	TEST	TEST	X	00h
6Ch	7Ch	CONT3	ISEL[2]	ISEL[1]	ISEL[0]	SW3	OUTAE	PSAD	TEST	X	00h

Data can be loaded into the control registers only when $\overline{\text{S\_RESET}}$ = "L". Do not attempt to change any value in the control register when $\overline{\text{S\_RESET}}$ = "H”.

1. CONT0 can be set only when system reset ($\overline{\text{S\_RESET}}$ = "L").
2. CONT1~3 should be set when system reset ($\overline{\text{S\_RESET}}$ = "L"), otherwise noise will be output.

   Prior to changing the input selector (CONT3: ISEL[2:0], clocks should be applied and the ADC should be in normal operation mode. The ADC is powered up by setting CONT3:PSAD = 0. Spontaneous changes to the input selector may result in output noise (generated in the ADC data), so an external mute circuit after the DAC output may be required.
3. Default setting is the same value that is initialized by initial reset ($\overline{\text{INIT\_RESET}}$ =”L”).

2-1) CONT0 : clock and interface selector

This register is enabled only during system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	CKS1	CKS0	DIF	DIF1	DIF0	DISCK	SELCKO	X	00h

① D7,D6:CKS1 CKS0 master clock select

Mode	CKS1(D7)	CKS0(D6)	
1	0	0	512fs
2	0	1	384fs(Program steps of DSP are also limited 384 steps)
3	1	0	TEST
4	1	1	TEST

② D5:DIF audio interface selector

0: MSB-justified

1: I^2S compatible (all input / output pins are I^2S compatible)

③ D4, D3:DIF1, DIF0 SDIN input mode selector

Mode	D4	D3	
1	0	0	MSB justified (24bit)
2	0	1	LSB justified (24bit)
3	1	0	LSB justified (20bit)
4	1	1	LSB justified (16bit)

Note) When D5 = 1, the state is I^2S compatible independent of mode setting, but set this register to Mode 1.

④ D2:DISCK LRCLK,BITCLK output control

0: Normal Operation

1: Sets BITCLK = "L" and LRCLK = "H" int master mode. (for I^2S compatible setting, it changes to LRCLK="L".) This setting is only available for analog input and analog output. When this mode is selected, SDIN and SDOUT are not available.

⑤ D1:SELCKO CLKO output selector.

0: CLKO outputs the same frequency as XTI.

1: CLKO outputs "L" level. After setting CONT0 (when the last clock of SCLK rises), CLKO frequency will change.

⑥ D0: Always 0

Note) Underlined settings for ①~⑤ indicates default.

2-2) CONT1: RAM control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
64h	74h	CONT1	DATARAM	RM	BANK[1]	BANK[0]	CMP_N	SS[1]	SS[0]	X	00h

① D7: DATARAM addressing mode selector

0:Ring addressing mode

1:Linear addressing mode

DATARAM has 256-word x 24-bit with two address pointers (DP0, DP1).

Ring addressing mode: increments starting address by one every sample.

Linear addressing mode: starting address is always the same: DP0 = 00h and DP1 = 80h.

② D6:RM: decompress bit mode

0: SIGN bit

1: Random data

When the compress and decompress function is selected (D3:CMP_N = 0), this bit determines the content o f the decompressed LSB bits.

③ D5,D4:BANK[1:0] DLRAM setting

Mode	D5	D4	Memory
0	0	0	24bit 3kword (RAM A)
1	0	1	12bit 6kword (RAM A)
2	1	0	12bit 4kword (RAM A),24bit 1kword (RAM B)
3	1	1	24bit 1kword (RAM A),12bit 4kword (RAM B)

Note) In mode 0 or 1, both pointer 0 and 1 are available for both RAM A and B.
In mode 2 or 3, pointer 0 is available for RAM A and pointer 1 is available for RAM B.

④ D3:CMP_N 12bitDLRAM compress & decompress selector

In mode 1,2 or 3, this register turns the compress / decompress function ON or OFF.

0: Compress & decompress function ON

When writing to DLRAM the DBUS data is compressed to 12-bits, and when reading from DLRAM, the data is decompressed to 16-bits.

1: Compress & decompress function OFF

12-bits of DBUS data is always written to DLRAM, and 12-bit data is read from the DLRAM and 000h is added for the LSB bits.

⑤ D2,D1:SS[1:0] DLRAM setting of sampling timing (only for RAM A)

Mode	D2	D1	RAM A mode selected by BANK[1:0]
0	0	0	Update every sampling time
1	0	1	Update every 2 sampling time
2	1	0	Update every 4 sampling time
3	1	1	Update every 8 sampling time

Note) When the mode 1,2 or 3 is selected, it comes out aliasing.

⑥ D0: Input always 0

Note) Underlined settings for ①~⑤ indicates default.

2-3) CONT2 : DAC ,DSP control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
68h	78h	CONT2	SW2	SW1	SW0	PSDA2	PSDA1	TESTT	TEST	X	00h

① D7,D6,D5: SW2, SW1, SW0 internal path setting

SW2(D7)	SW1(D6)	SW0(D5)	
0	0	0	Normal operation

These settings are reserved for test; set these values to "0" (refer to the block-diagram).

② D4:PSDA2 DAC2 power down control

0:Normal operation
1:DAC2 power down
If not using DAC2, set this value to "1", and DAC2 will RESET.
When changing to normal operation, set this value to "0" at system reset.

③ D3:PSDA1 DAC1 power down control

0:Normal operation
1:DAC1 power down
In the case of not using DAC1, set this value to "1" and DAC1 will be in RESET.
When changing to normal operation, set this value to "0" at system reset.

④ D2:TEST

0:Normal operation
1:Test mode (Do NOT use this mode)

⑤ D1:TEST

0:Normal operation
1:Test mode (Do NOT use this mode)

⑥ D0: Always input 0

Note): Underlined settings for ①~⑥ indicates default.

2-4) CONT3: ADC control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
6Ch	7Ch	CONT3	ISEL[2]	ISEL[1]	ISEL[0]	SW3	OUTAE	PSAD	TEST	X	00h

① D7,D6,D5:ISEL[2:0] analog input selector setting

ISEL[2](D7)	ISEL[1](D6)	ISEL[0](D5)	Analog input pin
0	0	0	AINL-,AINL+,AINR-,AINR+
1	0	0	AINL1,AINR1
1	0	1	AINL2,AINR2
1	1	0	AINL3,AINR3
1	1	1	AINL4,AINR4

② D4: SW3 internal path setting

0:Normal operation (ADC SDATA select)
1:DSP SDOUTD1 select

③ D3:OUTAE SDOUT disable

0:SDOUTA="L"
1:Output data selected by SW3

④ D2:PSAD ADC power down

0:Normal operation
1:ADC power down

When not using the ADC, set this value to "1", and the ADC will be in RESET.
The digital output data of the ADC will 00000h in power down mode.
When changing to normal operation, set this value to "0" at system reset.

⑤ D1:TEST

0:Normal operation
1:TESTmode (Do NOT use this mode)

⑥ D0: Always input 0

Note) Underlined settings of ①~⑤ indicates default.

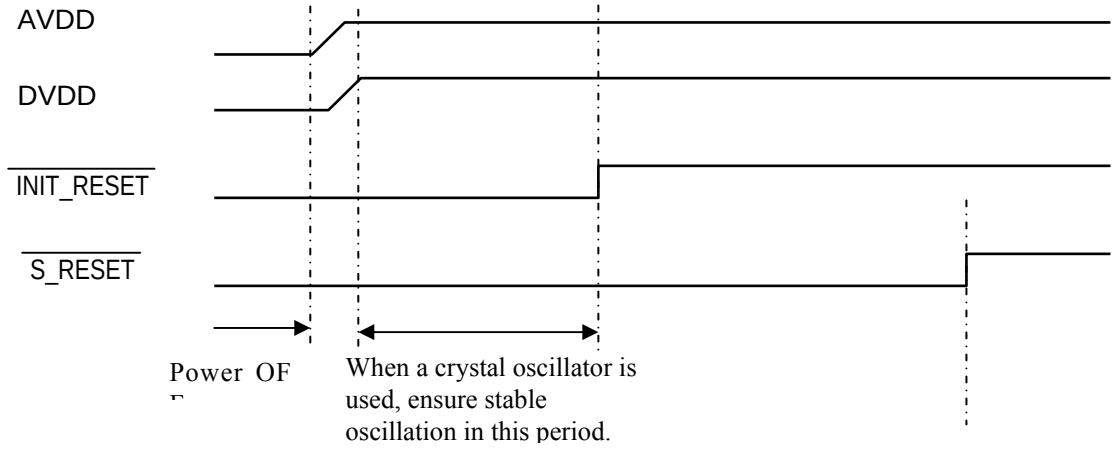
(3) Power supply startup sequence

Turn on the power by setting $\overline{\text{INIT\_RESET}}$ = “L” and $\overline{\text{S\_RESET}}$ = “L”. This sets up VREF (analog reference level). Then initizlize the control registers by setting $\overline{\text{INIT\_RESET}}$ = “H”.

Note 1) Only set $\overline{\text{INIT\_RESET}}$ during power-up.
Note 1): Set $\overline{\text{INIT\_RESET}}$ = "H" after starting oscillation when a crystal oscillator is used.
This setting time may differ depending on the crystal oscillator and its external circuit.

NOTE: Do not stop the system clock (slave mode: XTI, LRCLK, BITCLK, master mode: XTI) except when $\overline{\text{S\_RESET}}$ = "L". If these clock signals are not supplied, excess current will flow due to dynamic logic that is used internally, and an operation failure may result.

Do not set $\overline{\text{S\_RESET}}$ = "H" during $\overline{\text{INIT\_RESET}}$ = "L". This will stop the oscillator or cause it to be unstable.



Power supply startup sequence

(4) Resetting

The AK7740 has two reset pins: $\overline{\text{INIT\_RESET}}$ and $\overline{\text{S\_RESET}}$.

The $\overline{\text{INIT\_RESET}}$ pin sets up VREF and initializes the AK7740, as shown in "Power supply startup sequence section 3)."

The system is reset when $\overline{\text{S\_RESET}}$ ="L". (Description of "reset" is for "system reset".)

Under of system reset, program write operation executes normally (except for write operation during running).
The ADC and DAC sections are also reset during system reset. (The ADC output is MSB first 00000h and the DAC output is AVDD/2). However, VREF will be active and LRCLK and BITCLK in the master mode will be inactive.

Release system reset by setting $\overline{\text{S\_RESET}}$ to "H", which will activate the internal counter. This counter generates LRCLK and BITCLK in the master mode. When the system reset is released in slave mode, internal timing will be actuated in synchronization with "↑" of LRCLK (when the standard input format is used). Timing between the external and internal clocks is adjusted at this time. If the phase difference between LRCLK and internal timing is within ±1/16 of the input sampling cycle (1/fs) during the operation, the operation is performed with the internal timing remaining unchanged. If the phase difference exceeds this range, the phase is adjusted by synchronization with "↑" of LRCLK (when the standard input format is used). This circuit prevents failure of synchronization with the external circuit. For some time after returning to the normal state after loss of synchronization, normal data will not be valid. Change the frequency of the clock, SMODE or analog input selector while the system is in reset.

When $\overline{\text{S\_RESET}}$ is set to "H", the reset state is cancelled, and the internal DRAM is cleared from the rising edge of LRCLK. It takes 8fs (167usec at fs = 48kHz) to clear the internal DRAM.

The ADC section can output 516 cycles LRCLK after its internal counter starts. (The internal counter starts at the first rising edge of LRCLK in master mode. In slave mode, it starts at the end of 2-LRCLK after release of system reset.) The AK7740 is in normal operation mode when $\overline{\text{S\_RESET}}$ is set to "H".

When $\overline{\text{INIT\_RESET}}$ or $\overline{\text{S\_RESET}}$ changes, the status of the DAC section also changes to power down or release mode, which causes a click noise at the output. The SMUTE function does not mute this click, ao an external mute circuit is required to avoid any click noise.

(5) System clock

The required system clock is XTI (384fs/512fs), LRCLK (fs) and BITCLK (64fs) in the slave mode, and it is XTI (384 fs/512 fs) in the master mode. LRCLK corresponds to the standard digital audio rate (32 kHz, 44.1 kHz, and 48 kHz).

Fs	XTI(Master Clock)		BITCLK
	512fs	384fs	64fs
32.0kHz	16.3840MHz	12.2880MHz	2.0480MHz
44.1kHz	22.5792MHz	16.9344MHz	2.8224MHz
48.0kHz	24.576MHz	18.4320MHz	3.0720MHz

5-1) Master clock (XTI pin)

The master clock is produced by connecting a crystal oscillator between the XTI pin and XTO pin or by inputting an external clock into the XTI pin while the XTO pin is left open.

5-2) Slave mode

The required system clock is XTI, LRCLK (1 fs) and BITCLK (48/64fs).
The master clock (XTI) and LRCLK must be synchronized, but the phase is not critical.

5-3) Master mode

The required system clock is XTI (384fs/512fs). When the master clock (XTI) is input, LRCLK (1fs) and BITCLK (64fs) will be outputted from the internal counter synchronized with the XTI. LRCLK and BITCLK will not be active during initial reset ($\overline{\text{INIT\_RESET}}$ ="L") and system reset ($\overline{\text{S\_RESET}}$ ="L").

(6) Audio data interface (internal connection mode)

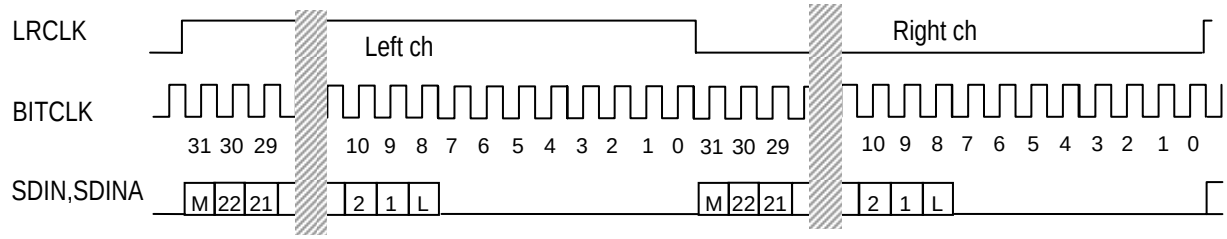
The serial audio data pins SDIN, SDINA, SDOUT and SDOUTA are interfaced with an external system, using LRCLK and BITCLK. The control registers (CONT2 and CONT3) set the audio interface parameters. The default data format is MSB-first two's complement. The data format can be changed to I^2S compatible mode by setting the control register CONT0:DIF (D5) to "1" (all input/output audio data pin interfaces are in I^2S compatible mode.)

The input SDIN and SDINA formats are MSB justified 24-bit at initialization. Setting the control registers CONT0: DIF1 (D4), DIF0 (D3) will cause SDIN to be compatible with LSB justified 24-bit, 20-bit and 16-bit. (SDINA is fixed to 24-bit MSB justified only) (Note: CONT0 DIF(D5)=0). Individual setting of SDIN and SDINA is not allowed. The output SDOUT is fixed at 24-bit MSB justified only.

In slave mode, BITCLK corresponds to both 64fs and 48fs. 64fs is the recommended BITCLK. 64fs examples are illustrated here:

6-1) Standard input format (DIF = 0: default set value)

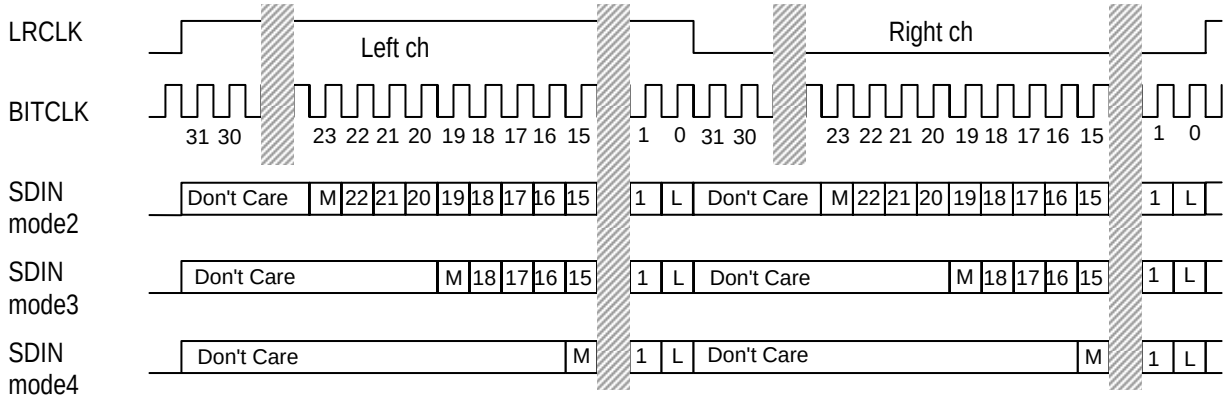
a) Mode 1 (DIF1, DIF0 = 0,0: default set value)



M : MSB, L : LSB

* For MSB-justified 20-bit data into SDIN, SDINA input four "0" following the LSB.

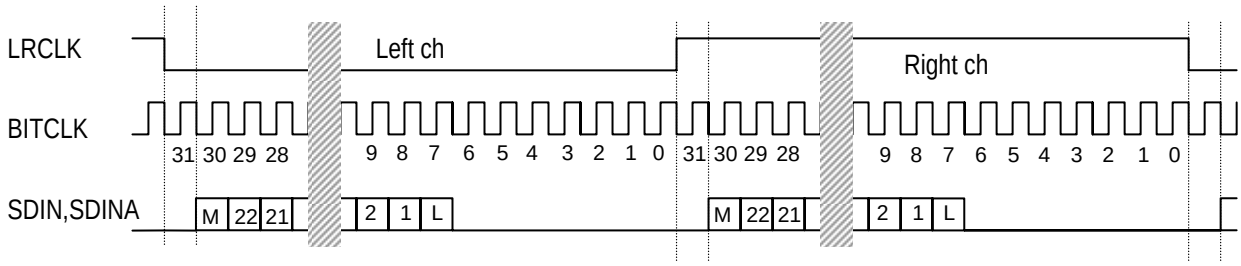
b) Mode 2, Mode 3, Mode 4



M : MSB, L : LSB

SDIN Mode 2: (DIF1, DIF0) = (0, 1) LSB justified 24-bit
SDIN Mode 3: (DIF1, DIF0) = (1, 0) LSB justified 20-bit
SDIN Mode 4: (DIF1, DIF0) = (1, 1) LSB justified 16-bit

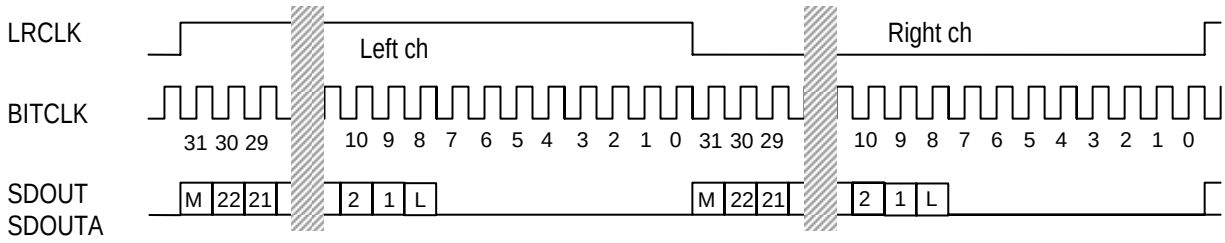
6-2) I²S compatible input format (DIF=1)



M : MSB, L : LSB

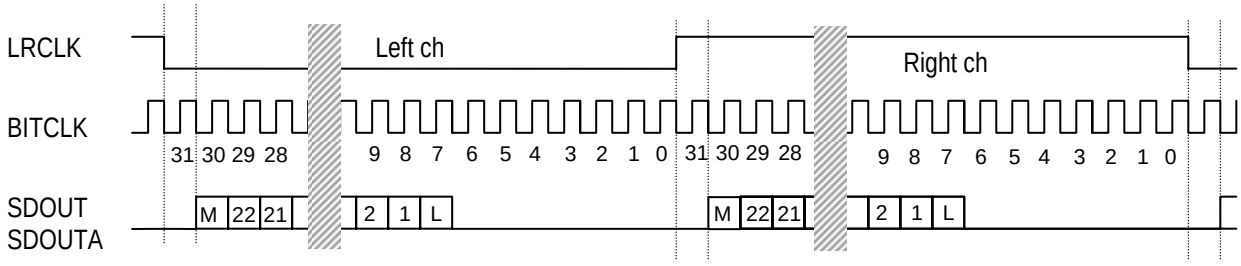
Mode 1: (DIF1(D4), DIF0(D3)) = (0, 0) must be set.

6-3) Standard output format (DIF=0: default set value)



M : MSB, L : LSB

6-4) I²S compatible output format (DIF=1)



M : MSB, L : LSB

(7) Interface with microcontroller

The microcontroller interface consists of six control signals; $\overline{RQ}$ (request), SCLK (serial data input clock), SI (serial data input), SO (serial data output), RDY (ready) and DRDY (data ready). Both write and read operations are enabled during system reset and run modes. During reset , writing to the control register, program RAM, coefficient RAM, offset RAM, external conditional jump code, and reading from the program RAM, coefficient RAM and offset RAM, are enabled. During the run phase, writing of coefficient RAM, offset RAM and external conditional jump code, and reading of data on the DBUS (data bus) from the SO, are enabled. The data is MSB first serial I/O.

To transfer data to the microcontroller, start by setting $\overline{RQ}$ "L", which enables a data read from the DBUS. The AK7740 reads SI data when SCLK rises, and outputs to SO when SCLK falls. The data format is command followed by address.

When $\overline{RQ}$ changes to "H", then one command is finished. New command requests require setting $\overline{RQ}$ to "L" again. When the DBUS data is read, leave $\overline{RQ}$ ="H" (command code input is not required).

Command Code List

Conditions for use	Code name	Command code		Note:
		WRITE	READ	
RESET phase	CONT0	60h	70h	For the function of each bit, See the description of Control Registers
	CONT1	64h	74h	
	CONT2	68h	78h	
	CONT3	6Ch	7Ch	
	PRAM	C0h	C1h	
	CRAM	A0h	A1h	
	OFRAM	90h	91h	
	External condition jump	C4h	-	
	Test	82h	-	Reserved for test
RUN phase	CRAM rewrite preparation	A8h	-	Must occur before CRAM rewrite
	CRAM rewrite	A4h	-	
	OFRAM rewrite preparation	98h	-	Must occur before OFRAM rewite
	OFRAM rewrite	94h	-	
	External condition jump	C4h	-	Same command as RESET

NOTE: Do not send any other command codes.
If there is no communication with the microcontroller, set the SCLK to "H" and the SI to "L" for use.

7-1) Write during reset phase

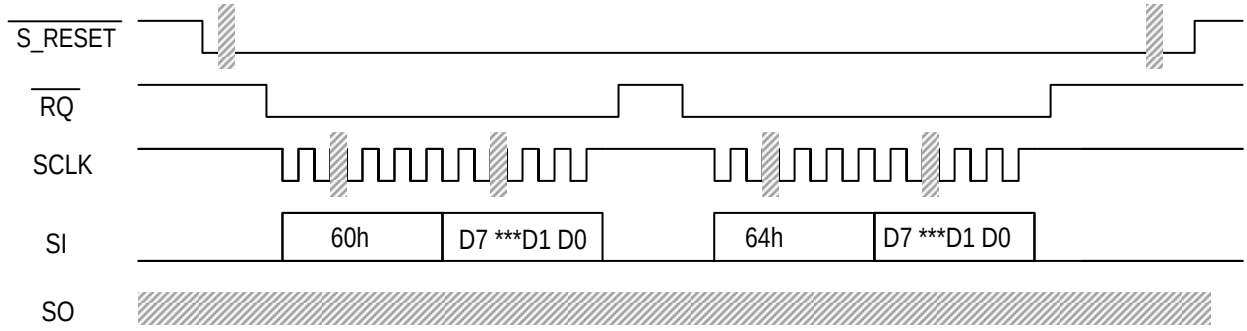
7-1-a) Control register write (during reset phase)

The data is comprised of two bytes that perform control register write operations (during reset phase). When the current data has been entered, the new data is sent when the 16th cycle of SCLK.

Data transfer procedure

① Command code	60h,64h,68h,6Ch
② Control data	(D7 D6 D5 D4 D3 D2 D1 D0)

For the function of each bit, see the description of control registers, (section 2).



Note) It must be set always 0 to D0

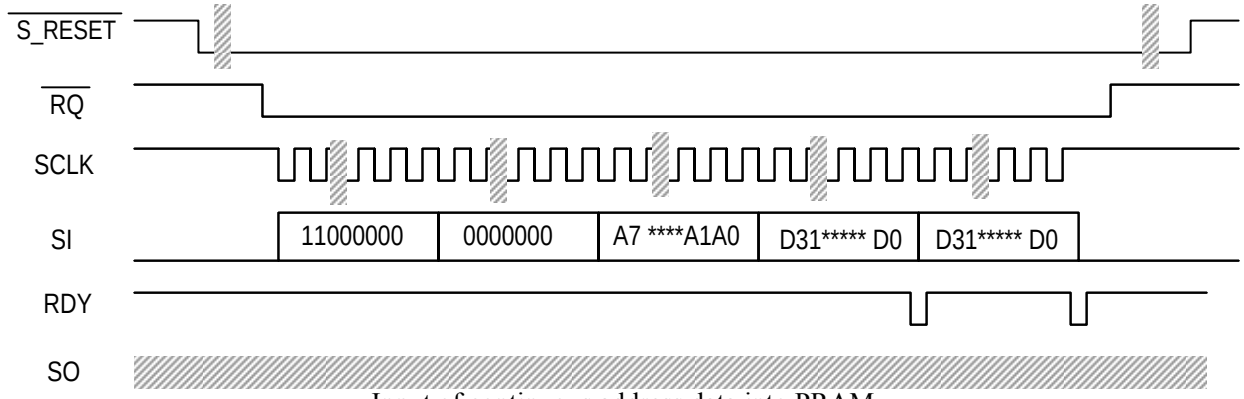
Control registers write operation

7-1-b) Program RAM writes (during reset phase)

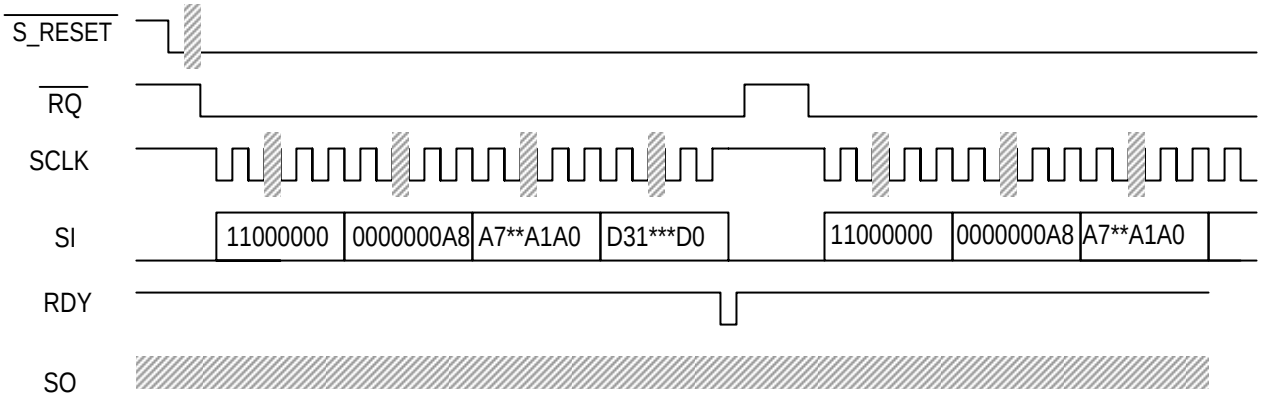
Write to the Program RAM during the reset phase with data consisting of a set of seven bytes. When all data has been transferred, the RDY terminal is set "L". Upon completion of the PRAM write, RDY returns “H” to allow the next data bit input. When writing data of continuous addresses, input the data as they are (no command code or address is required). To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" again. Then input the command code, address and data in that order.

Data transfer procedure

① Command code	C0h (1 1 0 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 0 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D31 . . . . . D24)
⑤ Data	(D23 . . . . . D16)
⑥ Data	(D15 . . . . . D8)
⑦ Data	(D7 . . . . . D0)



Input of continuous address data into PRAM



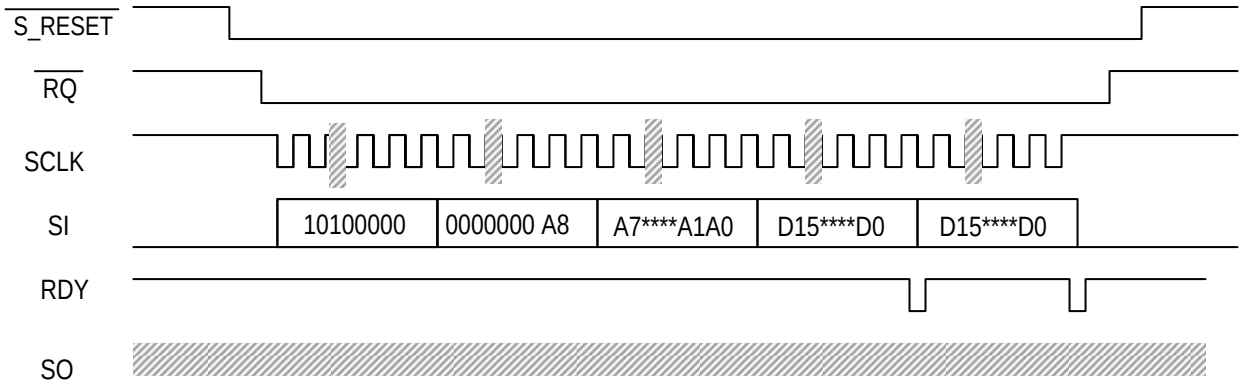
Input of discontinuous address data into PRAM

7-1-c) Coefficient RAM write (during reset phase)

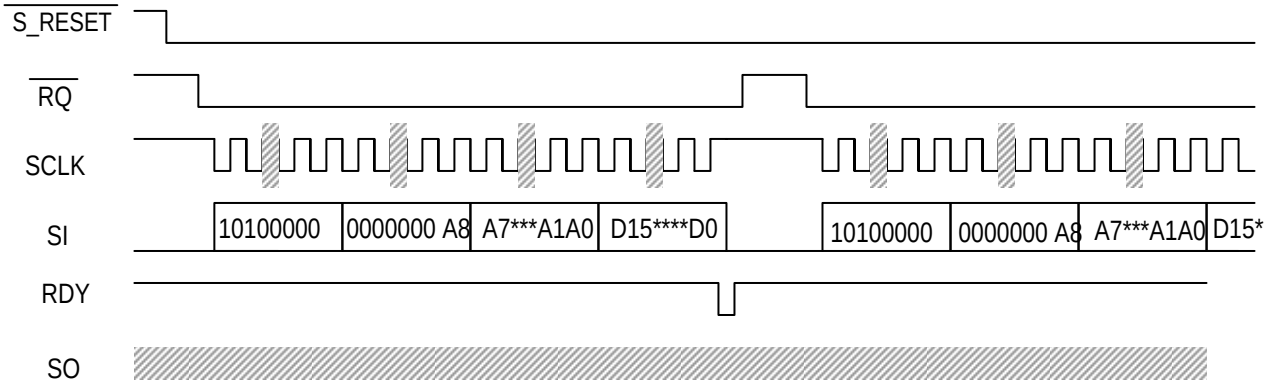
The data comprising a set of five bytes is used to perform coefficient RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes "H". Upon completion the CRAM write, RDY goes to "H" to allow the next data to be inputted. When writing data of continuous addresses, input the data as they are (no command code or address is required). To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L". Then input the command code, address and data in that order.

Data transfer procedure

① Command code	A0h (1 0 1 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 0 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D15 . . . . . D8)
⑤ Data	(D7 . . . . . D0)



Input of continuous address data into CRAM



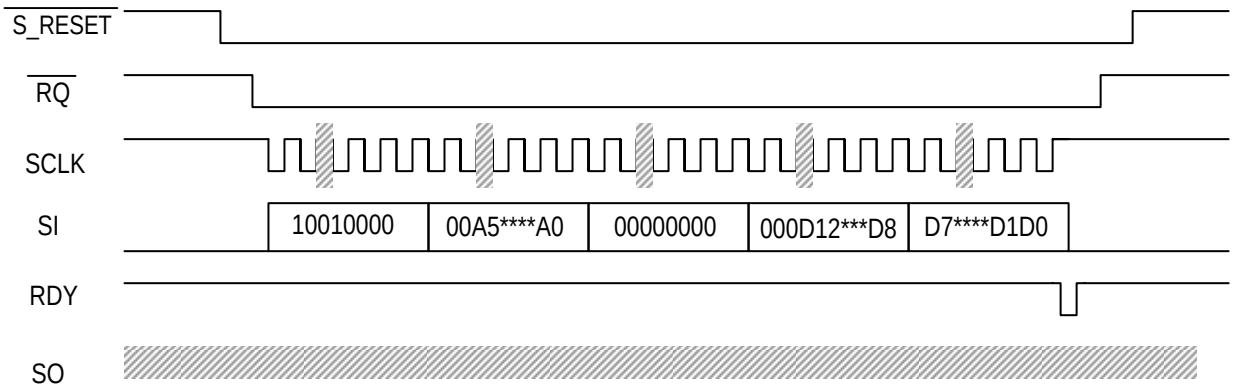
Input of discontinuous address data into CRAM

7-1-d) Offset RAM write (during reset phase)

The data comprising a set of five bytes is used to perform offset RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the OFRAM, RDY goes to "H" to allow the next data to be input. When data of continuous addresses are written, input the data as they are. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L". Then input the command code, address and data in that order.

Data transfer procedure

① Command code	90h	(1 0 0 1 0 0 0 0)
② Address		(0 0 A5 A4 .. . . A0)
③ Data		(0 0 0 0 0 0 0 0)
④ Data		(0 0 0 D12 D11 * * . D8)
⑤ Data		(D7 . . . . . D0)

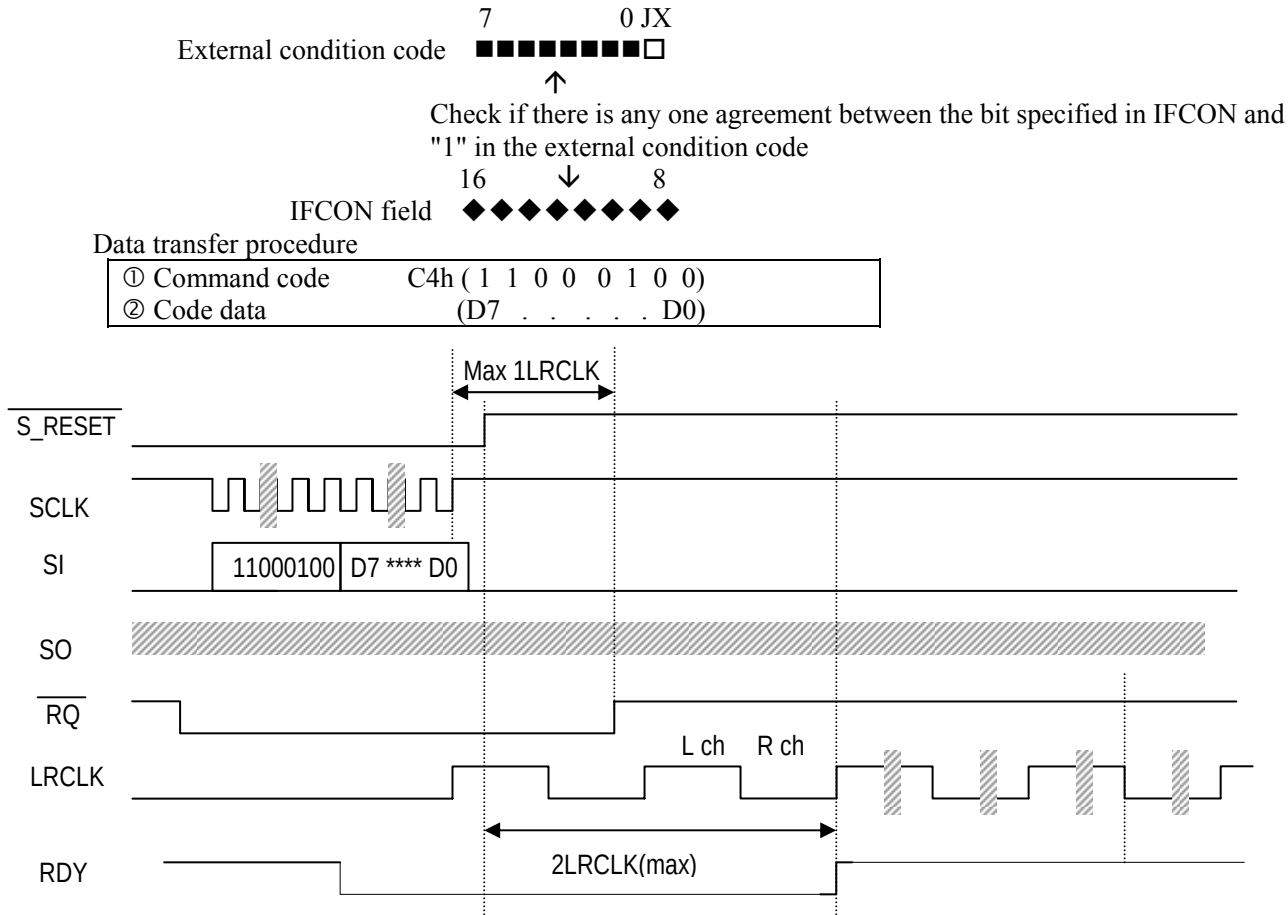


Input of data into OFRAM

7-1-e) External conditional jump code write (during reset phase)

The data comprising a set of two bytes is used to perform an external conditional jump code write operation. Input the data during either the reset or operation phase, and the input data are set to the specified register at the leading edge of the LRCLK. When all data bits have been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between "1" of each bit of external condition code eight bits (soft set), plus one bit (hard set) at the external input terminal JX and "1" of each bit of the IFCON field. The data during the reset phase can be written only before release of the reset, after all data has been transferred. $\overline{RQ}$ Transition from "L" to "H" in the write operation during the reset phase must be executed after three LRCLK in slave mode or one LRCLK in master mode, respectively, from the trailing edge of LRCLK after release of the reset. Then RDY goes to "H" after capturing the rise of the next LRCLK. Write operations from the microcontroller are disabled until RDY goes to "H". The IFCON field provides external conditions written on the program. It resets to 00h by $\overline{INIT\_RESET}$ ="L", however, it remains previous condition even $\overline{S\_RESET}$ ="L".

Note: LRCLK phase is inverted in the I^2S-compatible mode.



Timing for external conditional jump write operation (during reset phase)

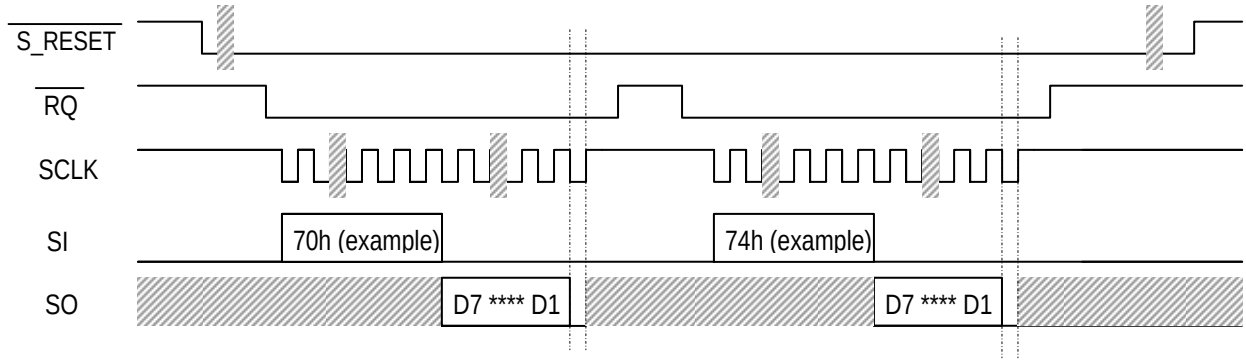
7-2) Read during reset phase

7-2-a) Control register data read (during reset phase)

To read data written into the control registers, input the command code and 16 bits of SCLK. After the command code input, the data D7 to D1 outputs from SO synchronized with the falling edge of SCLK. D0 is invalid, so ignore this bit.

Data transfer procedure

① Command code 70h,74h,78h,7Ch



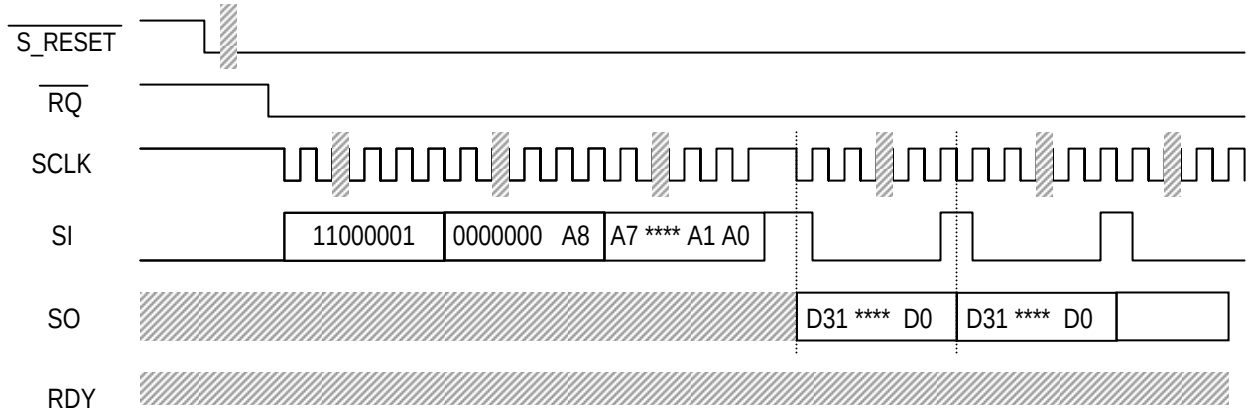
Reading of Control Register data

7-2-b) Program RAM read (during reset phase)

To read data written into PRAM, input the command code and the address to be read out. After that, set SI to "H" and SCLK to "L". The data is clocked out from SO synchronized with the falling edge of SCLK (ignore the RDY operation that will occur in this case). If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

①Command code input C1h (1 1 0 0 0 0 0 1)
②Read address input MSB (0 0 0 0 0 0 0 A8)
③Read address input LSB (A7 . . . . A0)



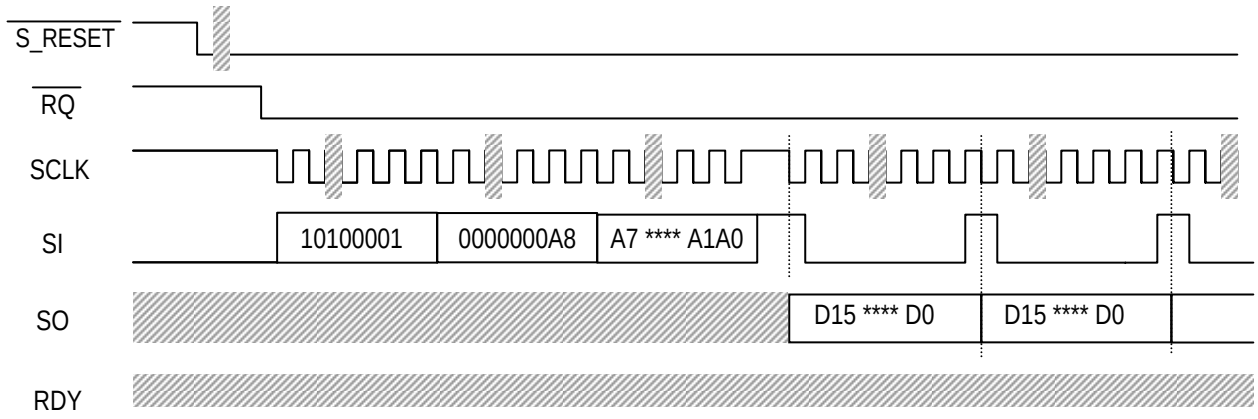
Reading of PRAM data

7-2-c) CRAM data read (during reset phase)

To read out the coefficient data, input the command code and the address to be read out. After that, set SI to "H" and SCLK to "L". The data is clocked out from SO synchronized with the falling edge of SCLK.If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

① Command code A1h	(1 0 1 0 0 0 0 1)
② Address upper	(0 . . . . . A8)
③ Address lower	(A7 . . . . . A0)



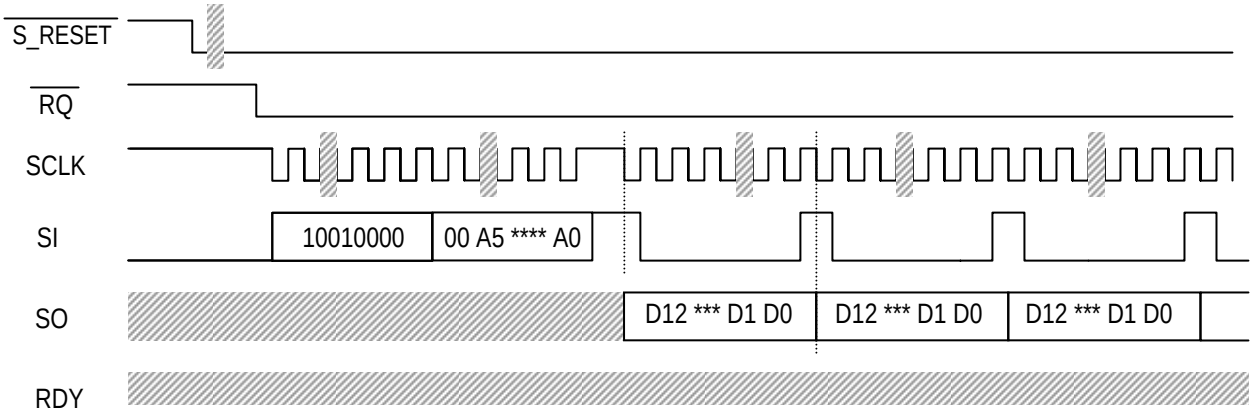
Reading of CRAM data

7-2-d) OFRAM data read (during reset phase)

Read out the offset data during the reset phase. To read it, input the command code and the address to be read. After that, set SI to "H" and SCLK to "L". This completes preparation for outputting the data. Set SI to "L", and the data is clocked out synchronized with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

① Command code	91h (1 0 0 0 1 0 0 0 1)
② Address	(0 0 A5 . . . . A0)



Reading of OFRAM data

7-3) Write during RUN phase

7-3-a) CRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite CRAM (coefficient RAM) during program execution. After inputting the command code, input a maximum of 16 data bytes to rewrite to a continuous address. Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

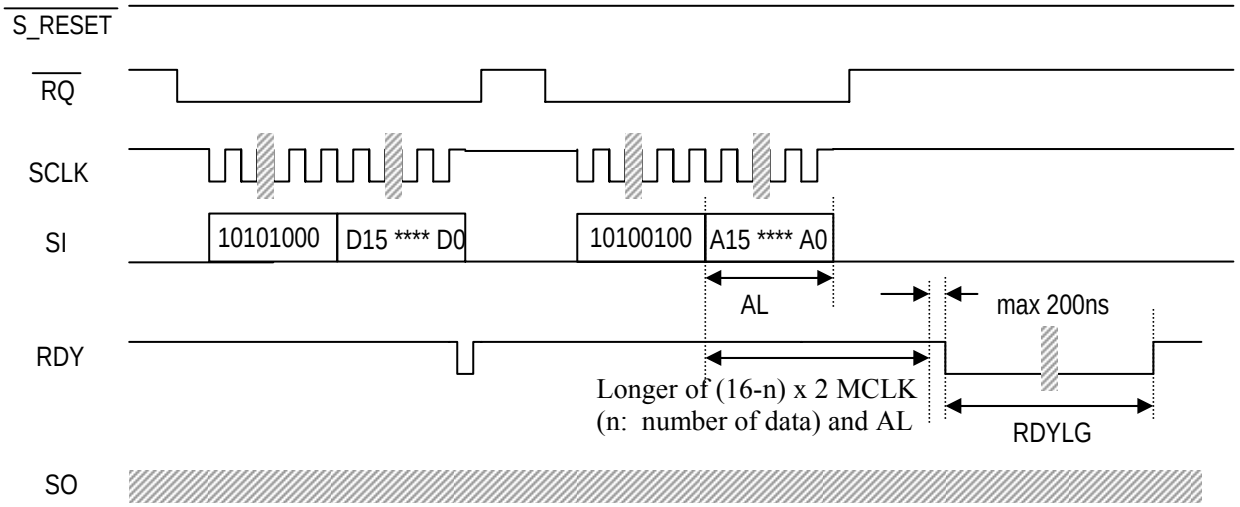
Coefficient RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↑ ↓ ↓ ↓

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	A8h	(1 0 1 0 1 0 0 0)
	② Data		(D15 . . . . D8)
	③ Data		(D7 . . . . . D0)
* Rewrite	① Command code	A4h	(1 0 1 0 0 1 0 0)
	② Address upper		(0 0 0 0 0 0 0 A8)
	③ Address lower		(A7 . . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

CRAM rewriting preparation and writing

7-3-b) OFRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite OFRAM (offset RAM) during program execution. After inputting the command code, input a maximum of 16 data bytes to rewrite to a continuous address. Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

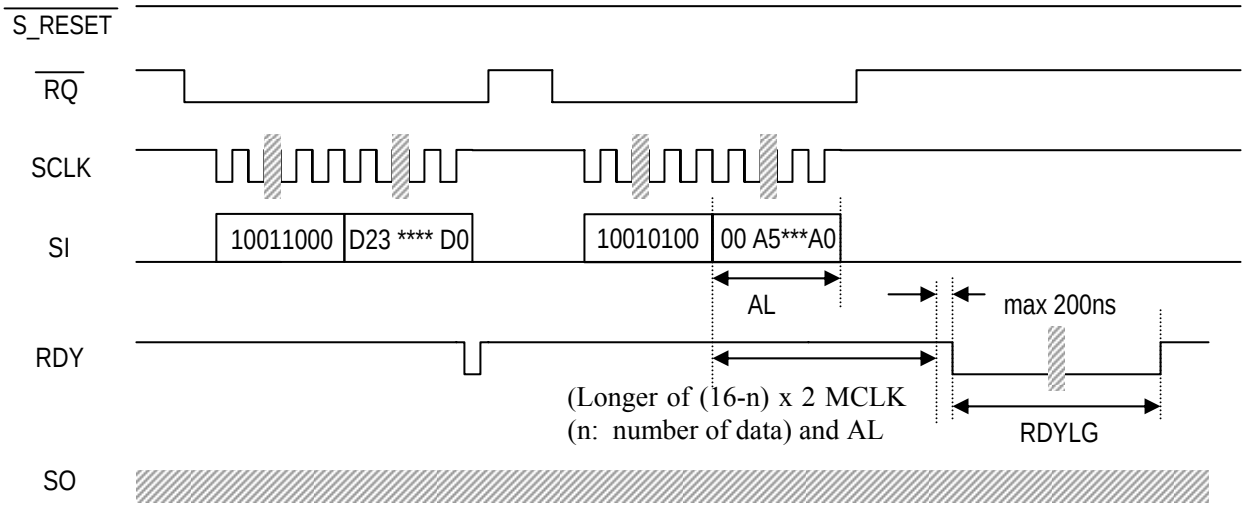
Offset RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↓ ↓ ↓ ↓

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	98h (1 0 0 0 1 1 0 0 0)
	② Data	(D23 . . . . . D16)
	③ Data	(D15 . . . . . D8)
	④ Data	(D7 . . . . . D0)
* Rewrite	① Command code	94h (1 0 0 0 1 0 1 0 0)
	② Address	(0 0 A5A4 . . . A0)



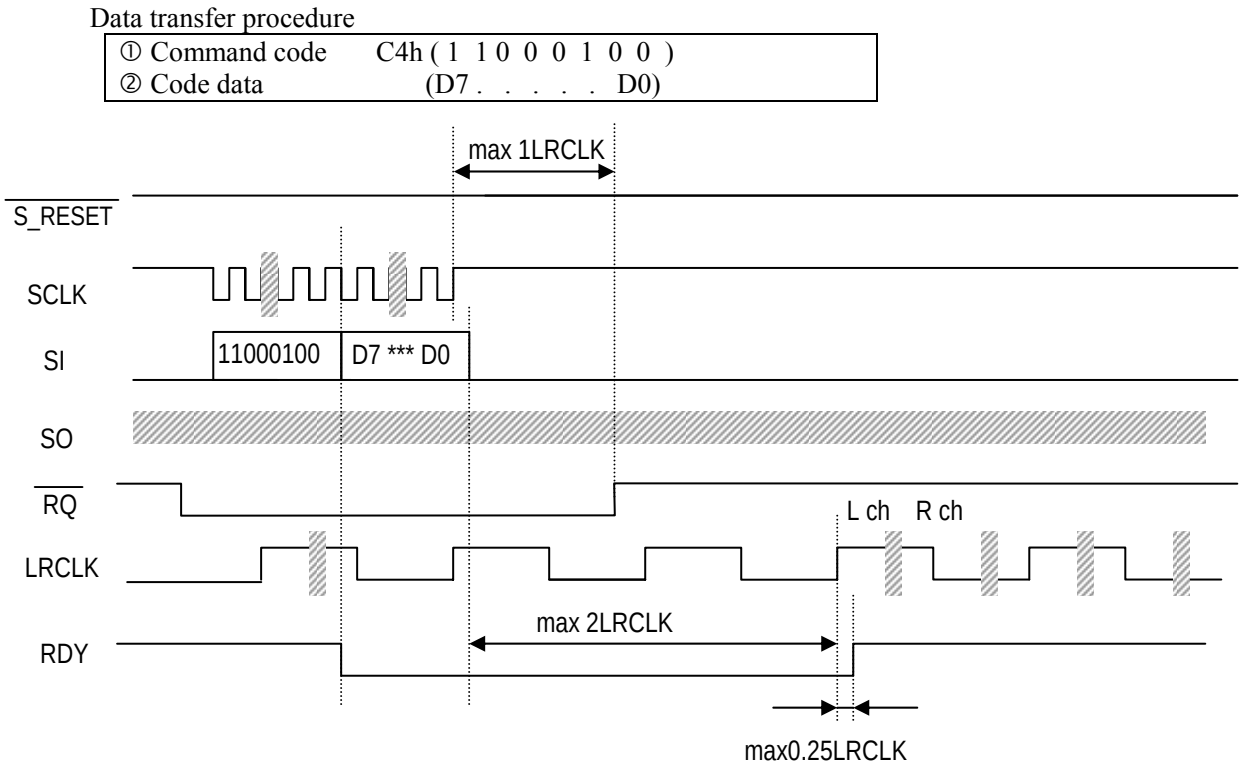
Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

OFRAM rewriting preparation and writing

7-3-c) External conditional jump code rewrite (during RUN phase)

Data comprising a set of two bytes is used to write the external conditional jump code. Data can be input during both the reset and operation phases, and input data is set to the specified register at the rising edge of LRCLK. When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between each bit of the 8-bit external condition code and "1"of each bit of the IFCON field. A write operation from the microcontroller is disabled until RDY goes to "H".

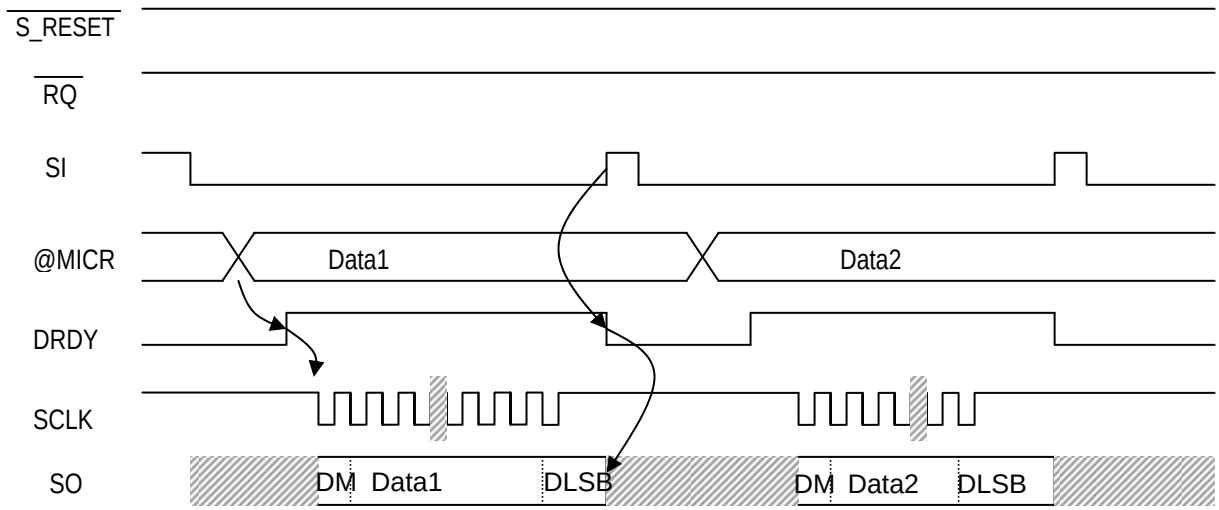
Note: The LRCLK phase is inverted in the I^2S-compatible mode.



External condition jump write timing (during RUN phase)

7-4) Read-out during RUN phase (SO output)

SO outputs data on DBUS (data bus) from the DSP section. Data is set when the @MICR command is executed in the DSP program. Setting the data allows DRDY to go to "H", and data is output synchronized with the falling edge of SCLK. When SI goes "H", DRDY goes to "L" to wait for the next command. Once DRDY goes "H", the data from the last @MICR command immediately before DRDY went "H" is held until SI goes "H", and subsequent commands will be rejected. A maximum of 24 bits are output from SO. After the required number of data (not exceeding 24 bits) is taken out by SCLK, setting SI to “H” can output the next data.



SO read (during RUN phase)

The SI pin controls clearing the output buffer (MICR). When reading this data, be aware that state changes on SI are asynchronous to the audio sampling clock, which may result in noise in the audio sugnal.

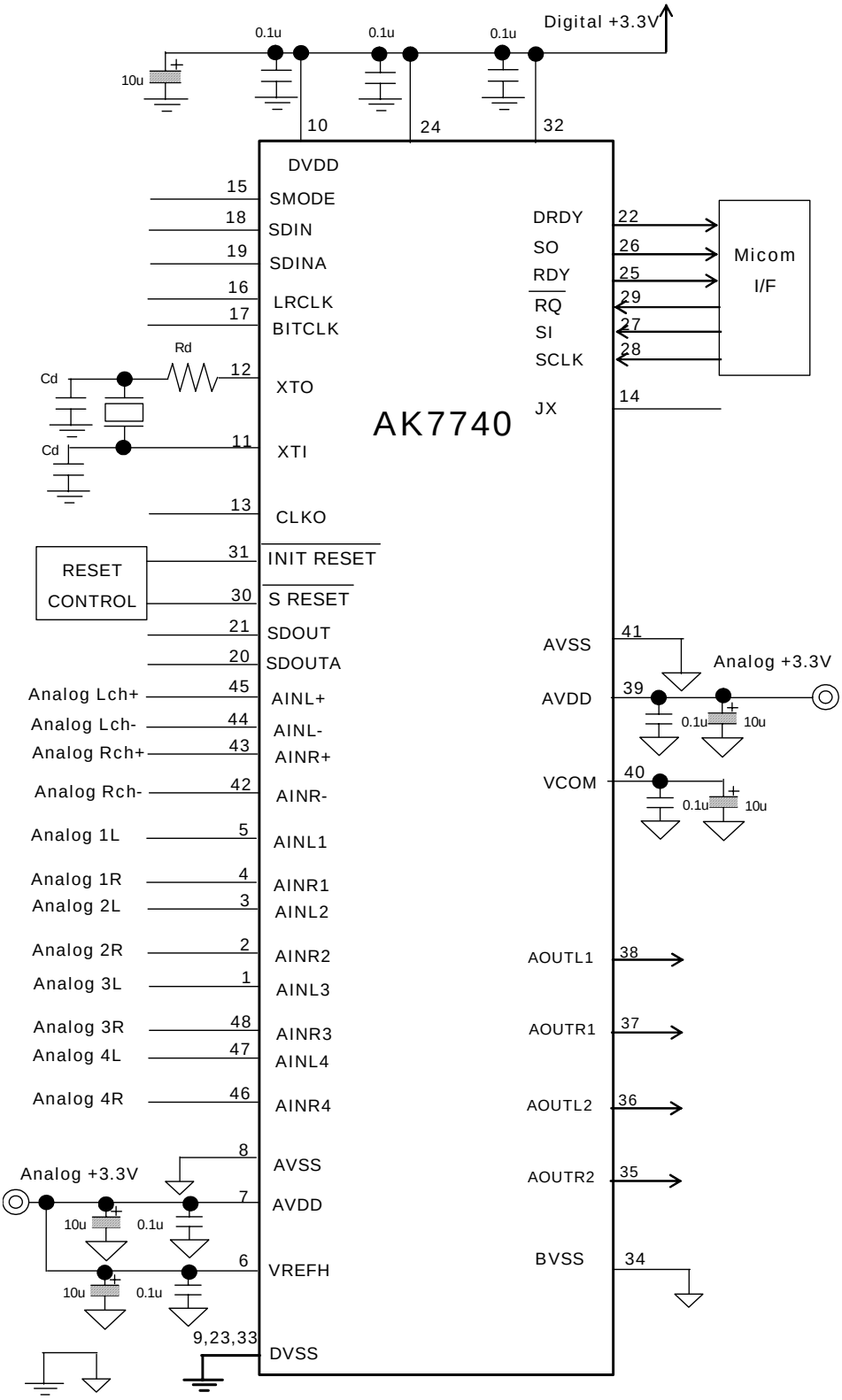
(8) ADC section high-pass filter

The AK7740 incorporates a digital high-pass filter (HPF) for cancelling DC offset in the ADC section. The HPF cut-off frequency is 1 Hz (fs = 48 kHz). This cut-off frequency is proportional to the sampling frequency (fs).

	48kHz	44.1kHz	32kHz
Cut-off frequency	0.93Hz	0.86Hz	0.62Hz

9. System Design

9-1) Connection example



9-2) Peripheral circuit

9-2-3) Ground and power supply

To minimize digital noise coupling, AVDD and DVDD should be individually de-coupled at the AK7740. System analog power is supplied to AVDD. Generally, power supply and ground wires must be connected separately according to the analog and digital systems. Connect them at a position close to the power source on the PC board. Decoupling capacitors, and ceramic capacitors of small values in particular, should be connected at positions as close as possible to the AK7740.

9-2-4) Reference voltage

The input voltage difference between the VREFH pin and the AVSS pin determines the full scale of analog input, while the potential difference between the VREFH pin and the AVSS pin determines the full scale of the analog output. Normally, connect AVDD to VREFH, and connect 0.1μF ceramic capacitors from them to AVSS. To shut out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor in particular should be connected at a position as close as possible to the pin. To avoid coupling to the AK7740, digital signals and clock signals in particular should be kept as far away as possible from the VREFH pin.

VCOM is used as the common voltage of the analog signal.To filter out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor in particular should be connected at a position as close as possible to the pin. Do not lead current from the VCOM pin.

9-2-5) Analog input

Analog input signals are applied to the modulator through the differential or single-ended input pins of each channel selected by the input selector. When using differential inputs, the voltage is equal to the differential voltage between AIN+ and AIN- (ΔVAIN=(AIN+)-(AIN-)), and the input range is ±FS = ±(VREFH-AVSS)×(2.0/3.3). When VREFH = 3.3V and AVSS = 0V, the input range is within ±2.0Vpp. When using single-ended inputs, the input range is FS = (VREFH-AVSS) × (2.0/3.3). When VREFH = 3.3V and AVSS = 0V, the input range is within 2.0Vpp. The output code format is given in terms of 2's complements.

When fs = 48 kHz, the AK7740 samples the analog input at 3.072 MHz. The digital filter eliminates noise from 30 kHz to 3.042 MHz. However, noise is not rejected in the bandwidth close to 3.072 MHz. Most audio signals do not have large noise near 3.072 MHz, so a simple RC filter is sufficient. A/D converter reference voltage is applied to the VREFH and AVSS pins.

The analog source voltage to the AK7740 is +3.3V (typical). Voltage of AVDD+0.3V or more, voltage of AVSS-0.3 V or less, and current of 10mA or more must not be applied to the analog input pins (AINL+, AINL-, AINR+, AINR-, AINL1, AINR1, AINL2, AINR2, AINL3, AINR3, AINL4, AINR4 and VREFH). Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. Accordingly, if the surrounding analog circuit voltage is ±15V, the analog input pins must be protected from signals with the absolute maximum rating or more.

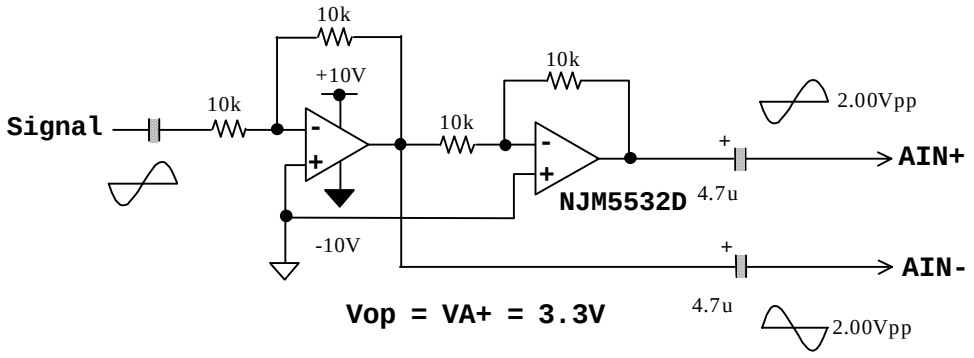


Fig. 1 Example of input buffer circuit (differential input)

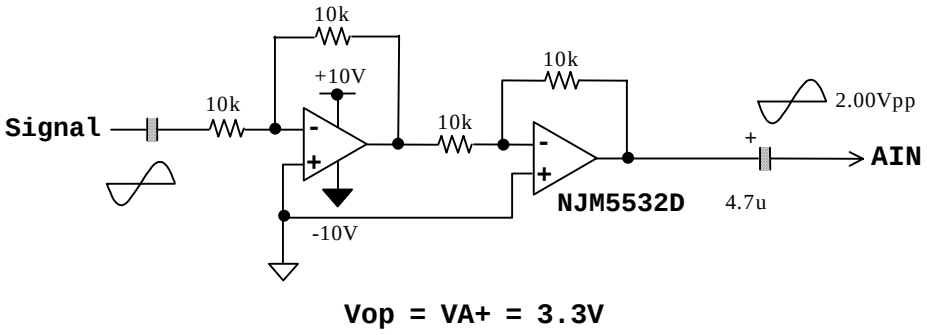


Fig. 2 Example of input buffer circuit (single ended input)

An analog signal can be applied to the AK7740 in single ended mode. In this case, apply the analog signal (the full scale is 2.0Vpp when the internal reference voltage is used). However, use of a low saturation operational amplifier is recommended if the operational amplifier is driven by the 3.3-volt power supply.

9-2-6) Analog output

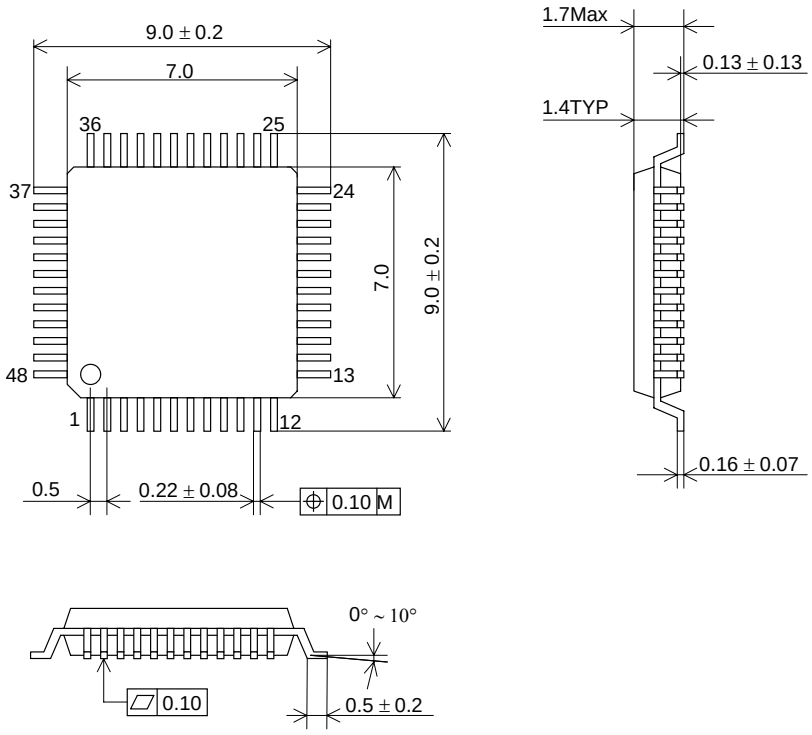
Analog output is single-ended, and the output range is 2.00Vpp (typical) with respect to VCOM voltage. The out-of-band noise (from the noise shaper) produced by the internal ΔΣ modulator is reduced by the internal switched capacitor filter (SCF) and continuous time filter (CTF). It is not necessary to add an external filter for normal applications. The input code format is given in terms of two's complement with the positive full-scale output for the 7FFFFFH (@24bit) input code, and the negative full-scale output for the 800000H (@24bit) input code. VCOM voltage is output as an ideal value for 000000H (@24bit) input code.

9-2-7) Connection to digital circuit

To minimize noise resulting from the digital circuit, connect low voltage logic to the digital output. The applicable logic family includes the 74LV, 74LV-A, 74ALVC and 74AVC series.

10. Package

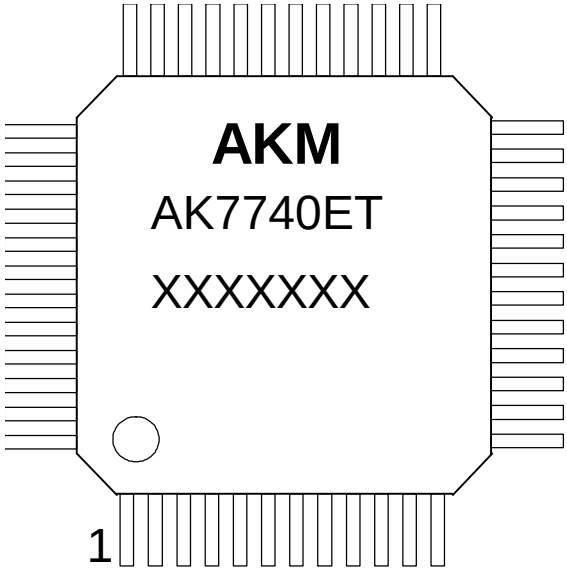
48pin LQFP(Unit:mm)



- Material & Lead finish

Package:	Epoxy
Lead-frame:	Copper
Lead-finish	Soldering plate

11. Marking



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK7740ET
4) Asahi Kasei Logo