15.625MHZ TO 62.5MHZ, 1:4 LVCMOS/ LVTTL ZERO DELAY CLOCK BUFFER

ICS86004

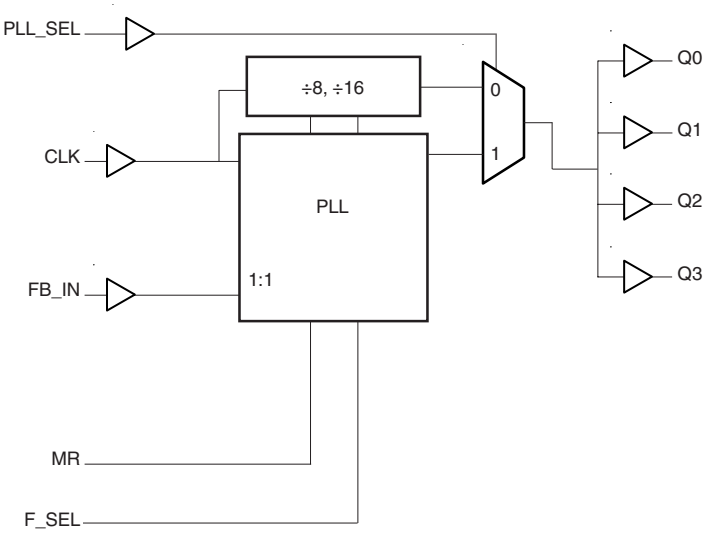
General Description

The ICS86004 is a high performance 1:4 LVCMOS/LVTTL Clock Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS86004 has a fully integrated PLL and can be configured as zero delay buffer and has an input and output frequency range of 15.625MHz to 62.5MHz. The VCO operates at a frequency range of 250MHz to 500MHz. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output divider.

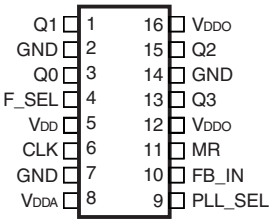
Features

- Four LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Single LVCMOS/LVTTL clock input
- CLK accepts the following input levels: LVCMOS or LVTTL
- Output frequency range: 15.625MHz to 62.5MHz
- Input frequency range: 15.625MHz to 62.5MHz
- VCO range: 250MHz to 500MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- Fully integrated PLL
- Cycle-to-cycle jitter: 65ps (maximum)
- Output skew: 65ps (maximum)
- Full 3.3V or 2.5V, or 3.3V core/2.5V output operating supply
- 0°C to 70° ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

Block Diagram



Pin Assignment



ICS86004
16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 3, 13, 15	Q1, Q0, Q3, Q2	Output		Clock outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
2, 7, 14	GND	Power		Power supply ground.
4	F_SEL	Input	Pulldown	Frequency range select input. See Table 3A and 3B. LVCMOS/LVTTL interface levels.
5	V_{DD}	Power		Core supply pin.
6	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
8	V_{DDA}	Power		Analog supply pin.
9	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as input to the dividers. When LOW, selects the reference clock (PLL Bypass). When HIGH, selects PLL (PLL Enabled). LVCMOS/LVTTL interface levels.
10	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay". Connect to one of the outputs. LVCMOS/LVTTL interface levels.
11	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
12, 16	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, V_{DDO} = 3.465V			23	pF
		V_{DD}, V_{DDA}, V_{DDO} = 2.625V			17	pF
R_{OUT}	Output Impedance	3.3V ± 5%	5	7	12	Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE, PLL_SEL = 1

Input	Input/Output Frequency Range (MHz)	
F_SEL	Minimum	Maximum
0	31.25	62.5
1	15.625	31.25

TABLE 3B. CONTROL INPUT FUNCTION TABLE, PLL_SEL = 0

Input	Output
F_SEL	
0	Ref ÷8
1	Ref ÷16

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				98	mA
I_{DDA}	Analog Supply Current				17	mA
I_{DDO}	Output Supply Current				8	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDA}$ = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				98	mA
I_{DDA}	Analog Supply Current				17	mA
I_{DDO}	Output Supply Current				8	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				88	mA
I_{DDA}	Analog Supply Current				14	mA
I_{DDO}	Output Supply Current				6	mA

TABLE 4D. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	CLK, MR, FB_IN, F_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		PLL_SEL	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK, MR, FB_IN, F_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		PLL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.465V	2.6			V
			V_{DDO} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.465V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information Section, *Output Load Test Circuit diagrams.*

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.1		6.1	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V	-500		500	ps
*t*sk(o)	Output Skew; NOTE 3, 4	PLL_SEL = 0V			65	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4			50	65	ps
t_L	PLL Lock Time				1	mS
t_R / t_F	Output Rise/Fall Time		0.4		1	ns
odc	Output Duty Cycle		49		51	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at V_{DDO}/2.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.25		6.25	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 2.5V	-500		500	ps
*t*sk(o)	Output Skew; NOTE 3, 4	PLL_SEL = 0V			65	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4				65	ps
t_L	PLL Lock Time				1	mS
t_R / t_F	Output Rise/Fall Time		0.4		1	ns
odc	Output Duty Cycle		48		52	%

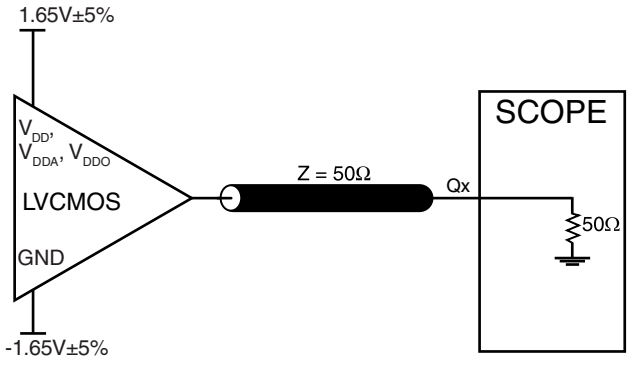
All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

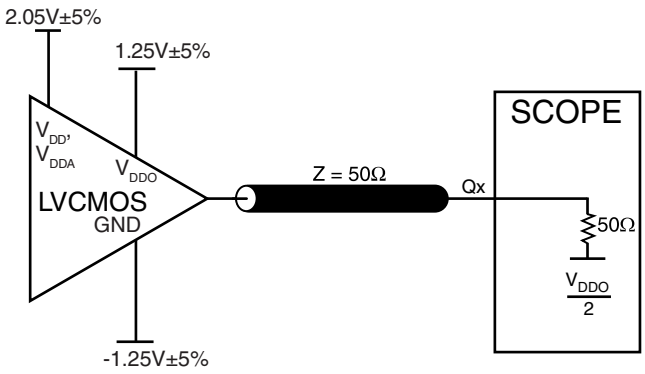
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.5		6.5	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 2.5V	-500		500	ps
*t*sk(o)	Output Skew; NOTE 3, 4	PLL_SEL = 0V			65	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4				70	ps
t_L	PLL Lock Time				1	mS
t_R / t_F	Output Rise/Fall Time		0.4		1	ns
odc	Output Duty Cycle		48		52	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

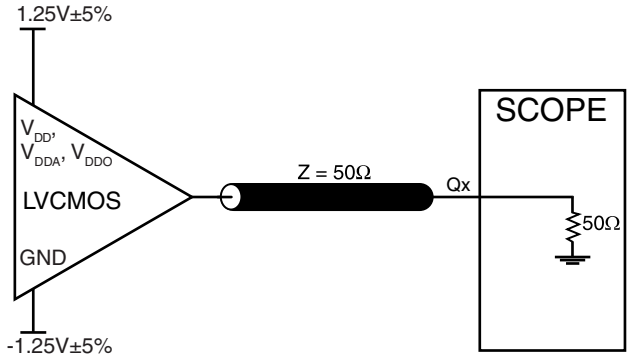
PARAMETER MEASUREMENT INFORMATION



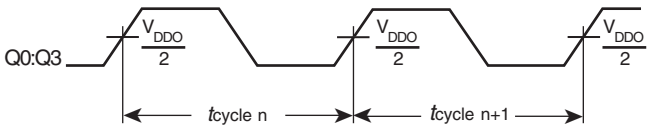
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

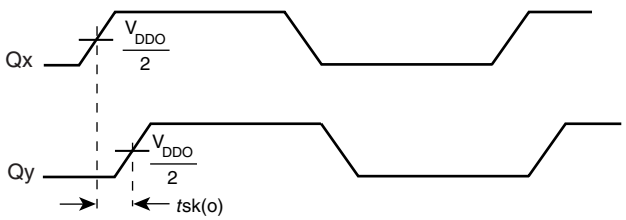


2.5VCORE/ 2.5V OUTPUT LOAD AC TEST CIRCUIT

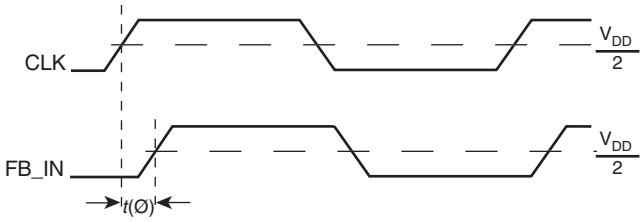


$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

CYCLE-TO-CYCLE JITTER

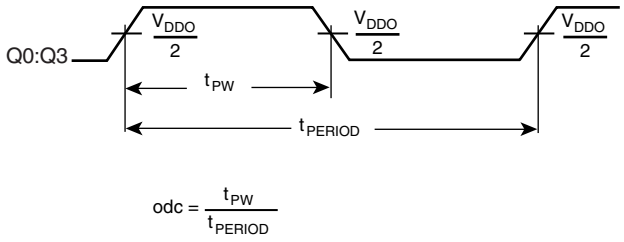


OUTPUT SKEW



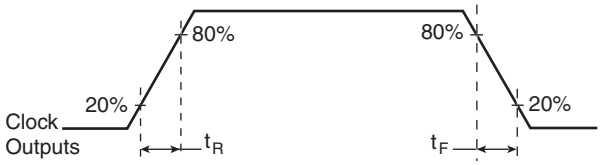
$t(Ø)_{mean}$ = Static Phase Offset
(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

STATIC PHASE OFFSET

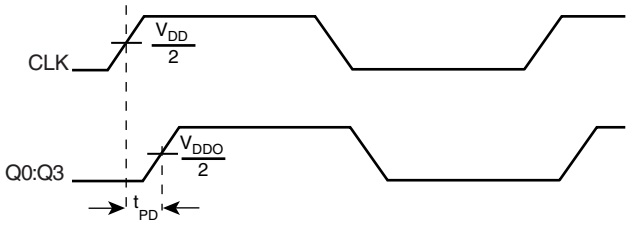


$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS86004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

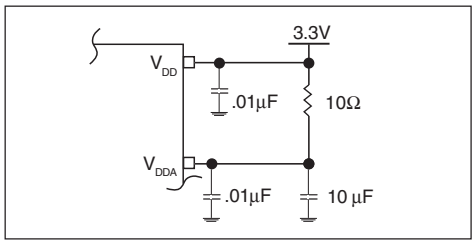


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

SCHEMATIC EXAMPLE

Figure 2 shows a schematic example of using an ICS86004. It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the V_{DDA} pin as possible.

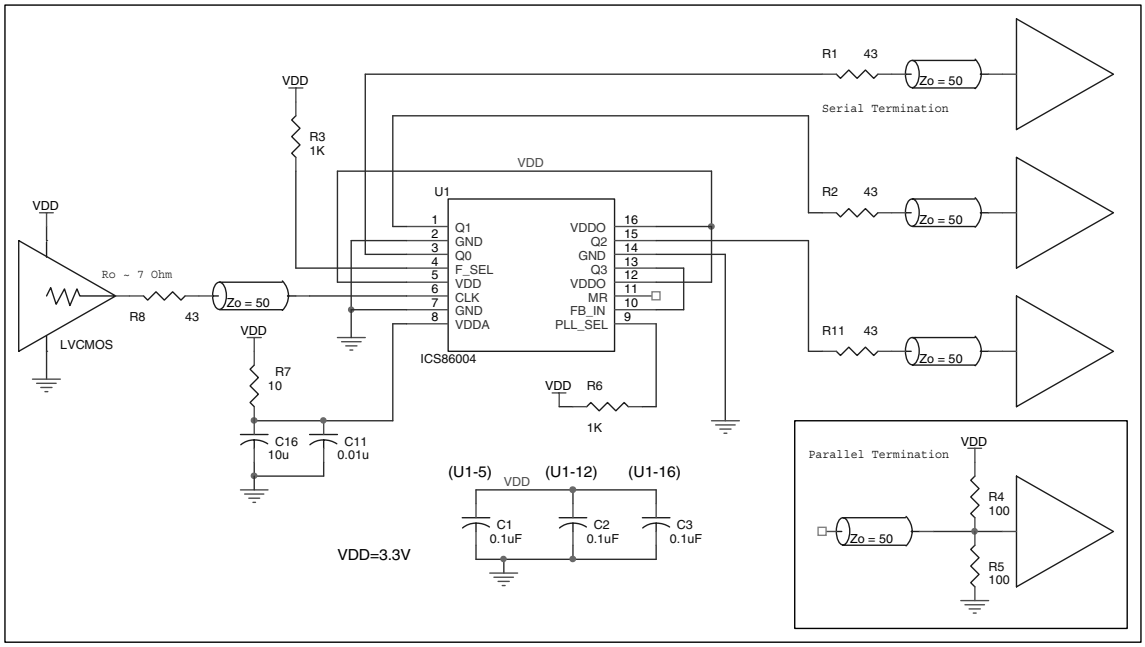


FIGURE 2. ICS86004 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS86004 is: 2496

Package Outline - G Suffix 16 Lead TSSOP

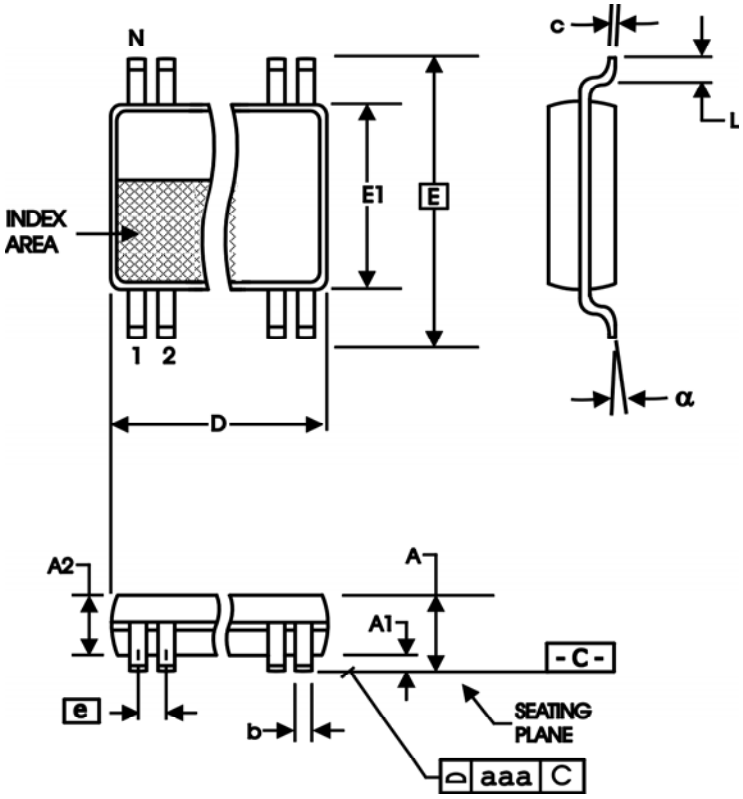


Table 6. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS86004BG	86004BG	16 Lead TSSOP	Tube	0°C to 70°C
ICS86004BGT	86004BG	16 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
ICS86004BGLF	86004BGL	16 Lead "Lead-Free" TSSOP	Tube	0°C to 70°C
ICS86004BGLFT	86004BGL	16 Lead "Lead-Free" TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		1	Pin Assignment - corrected package body dimensions from 4.4mm x 3.0 mm x 0.92mm to 4.4mm x5.0 mm x 0.925mm.	3/31/06
	T7	12	Ordering Information Table - corrected marking from ICS86004BG from 86004BG. Added lead-free marking.	
B	4A	3	3.3V Power Supply Table - changed VD_{DA} max from 3.465V to V_{DD}, changed I_{DDO} from 79mA max. to 8mA max.	6/21/06
	4B	3	3.3V/2.5V Power Supply Table - changed VD_{DA} max from 3.465V to $V_{DD,}$ changed I_{DDO} from 79mA max. to 8mA max.	
	4C	3	2.5V Power Supply Table - changed V_{DDA} max from 3.465V to $V_{DD,}$ changed I_{DDO} from 79mA max. to 6mA max.	

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For Sales
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480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com