ACT412

Rev 1, 30-Oct-13

ActivePSR™ Quasi-Resonant PWM Controller

FEATURES

- **Patented Primary Side Regulation Technology**
- **Quasi-Resonant Operation**
- **Adjustable up to 120kHz Switching Frequency**
- **+/-5% Output Voltage Regulation**
- **Constant Power Operation Mode for Fast Start-up and Motor Drive Applications**
- **Integrated Line and Primary Inductance Compensation**
- **Built-in Soft-Start Circuit**
- **Line Under-Voltage, Thermal, Output Over-voltage, Output Short Protections**
- **Current Sense Resistor Short Protection**
- **Transformer Short Winding Protection**
- **Less than 100mW Standby Power**
- **Complies with Global Energy Efficiency and CEC Average Efficiency Standards**
- **Tiny SOT23-6 Packages**

APPLICATIONS

- **AC/DC Adaptors/Chargers for E-Shaver, Motor Driver, ADSL, Network Power, Cell Phone**
- **Big Capacitive Load Application**

GENERAL DESCRIPTION

The ACT412 is a high performance peak current mode PWM controller which applies *ActivePSR*™ and *ActiveQR*™ technology. ACT412 achieves accurate voltage regulation without the need of an opto-coupler or reference device.

The ACT412 is designed to achieve less than 100mW Standby Power. By applying frequency fold back and *ActiveQR*™ technology, ACT412 exceeds the latest ES2.0 efficiency standard.

ACT412 integrates comprehensive protection. In case of over temperature, over voltage, short winding, short current sense resistor, open loop and overload conditions, it would enter auto restart mode including cycle-by-cycle current limiting.

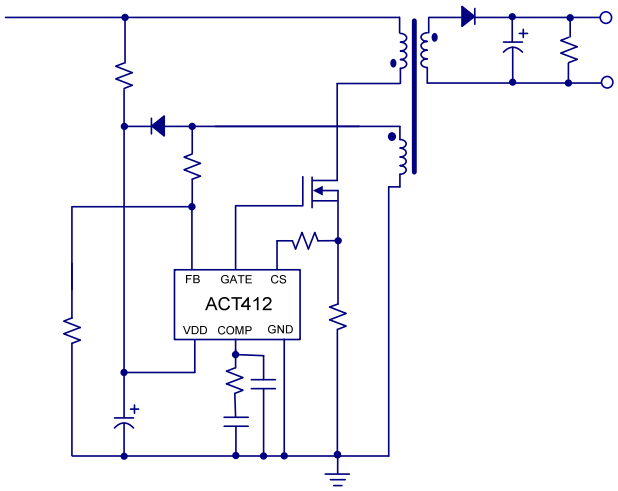
ACT412 is to achieve no overshoot and very short rise time even with big capacitive load (10000μF) with the built-in fast and soft start process, .

The Quasi-Resonant (QR) operation mode can effectively improve efficiency, reduce the EMI noise and further reduce the components in input filter.

ACT412 is idea for application up to 36 Watt.

Figure 1:

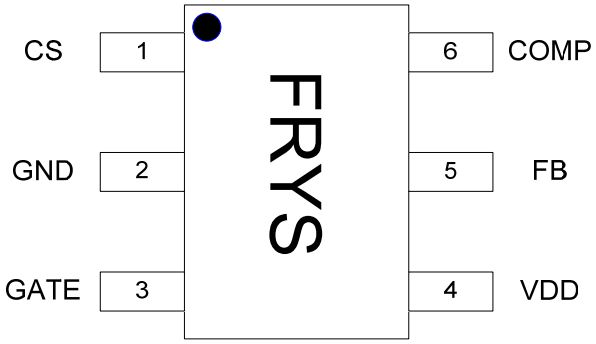
Simplified Application Circuit



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT412US-T	-40°C to 85°C	SOT23-6	6	TUBE & REEL	FRYS

PIN CONFIGURATION



SOT23-6
ACT412US

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CS	Current Sense Pin. Connect an external resistor (R_{CS}) between this pin and ground to set peak current limit for the primary switch.
2	GND	Ground.
3	GATE	Gate Drive. Gate driver for the external MOSFET transistor.
4	VDD	Power Supply. This pin provides bias power for the IC during startup and steady state operation.
5	FB	Feedback Pin. Connect this pin to a resistor divider network from the auxiliary winding.
6	COMP	Compensation Pin.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
FB, CS, COMP to GND	-0.3 to + 6	V
VDD, GATE to GND	-0.3 to + 22	V
Maximum Power Dissipation (SOT23-6)	0.45	W
Operating Junction Temperature	-40 to 150	˚C
Junction to Ambient Thermal Resistance (θ_{JA})	220	˚C/W
Operating Junction Temperature	-40 to 150	˚C
Storage Temperature	-55 to 150	˚C
Lead Temperature (Soldering, 10 sec)	300	˚C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 18V, L_M = 0.5mH, R_{CS} = 0.75Ω, V_{OUT} = 13V, N_P = 68, N_S =12, N_A = 17, T_A = 25°C, unless otherwise specified,12V0.4A application)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising from 0V	11.11	12.35	13.58	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling after Turn-on	4.8	5.4	6	V
VDD Over Voltage Protection	V_{DDOVP}	V_{DD} Rising from 0V	18.45	20.5	22.55	V
Start Up Supply Current	I_{DDST}	V_{DD} = 11V, before VDD Turn-on		5	10	μA
IDD Supply Current	I_{DD}	V_{DD} = 12V, after VDD Turn-on (no switching)		0.55	1	mA
IDD Supply Current at Fault Mode	I_{DD}	V_{DD} = 12V, after VDD Turn-on, fault = 1		0.25		mA
Feedback						
Effective FB Reference Voltage	V_{FBREF}		2.23	2.25	2.28	V
FB Sampling Blanking Time	T_{FB_BLK}	Light load	0.38	0.45	0.52	μs
		Heavy Load	1.1	1.3	1.5	μs
Time needed for FB Sampling (After blanking)	T_{FB_SAMP}	FB sampling	0.5	0.65	0.75	μs
		CC and Knee point detecting	0.22	0.25	0.29	μs
FB Leakage Current	I_{BVFB}	V_{FB} = 3V			1	μA
Current Limit						
CS Current Limit Threshold	V_{CSLIM1}	V_{OUT} = 12V		0.5		V
	V_{CSLIM2}	V_{OUT} = 6V		0.75		V
CS Minimum Current Limits Threshold	V_{CSMIN}			300		mV
CS to GATE Propagation Delay				60		ns
Leading Edge Blanking Time	$T_{CSBLANK}$	Light Load		150		ns
		Heavy Load		636		ns

ELECTRICAL CHARACTERISTICS CONT'D

(V_{DD} = 18V, L_M = 0.5mH, R_{CS} = 0.75Ω, V_{OUT} = 13V, N_P = 68, N_S =12, N_A = 17, T_A = 25°C, unless otherwise specified,12V0.4A application)

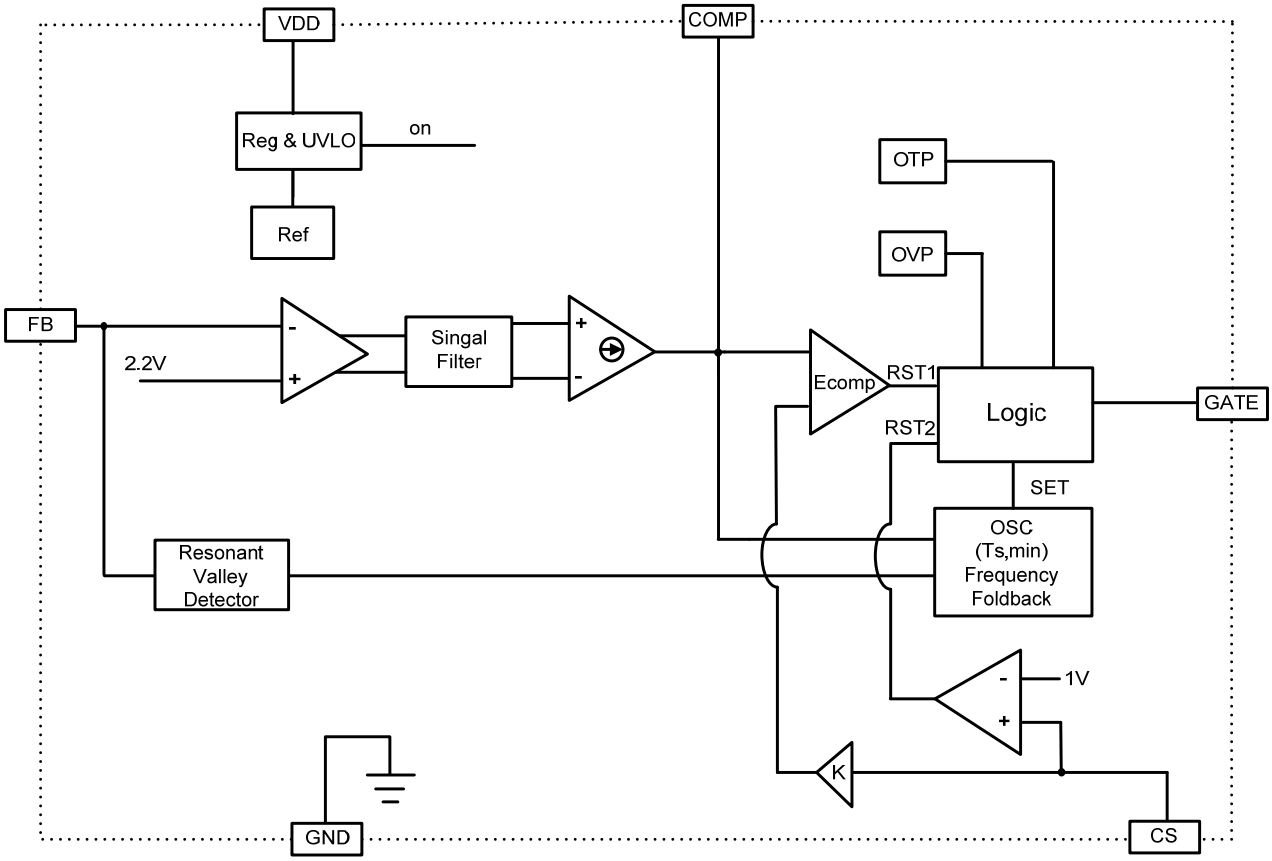
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVE						
Gate Rise Time	T_{RISE}	VDD = 10V, CL = 1nF		150	250	ns
Gate Falling Time	T_{FALL}	VDD = 10V, CL = 1nF		90		ns
Gate Low Level ON-Resistance	R_{ONLO}	I_{SINK} = 30mA		10		Ω
Gate High Level ON-Resistance	R_{ONHI}	I_{SOURCE} = 30mA		31		Ω
Gate Leakage Current		GATE = 18V, before VDD turn-on			1	μA
COMPENSATION						
Inside Compensate Resistor	R_{COMP}	ACT412		0		kΩ
Output Sink Current	I_{COMP_SINK}	V_{FB} = 3V, V_{COMP} = 2V	15	40		μA
Output Source Current	I_{COMP_SOURCE}	V_{FB} = 1.5V, V_{COMP} = 2V	15	40		μA
Transconductance of Error Amplifier	Gm			71		μA/V
Maximum Output Voltage	$V_{COMPMAX}$	V_{FB} = 1.5V		3.5		V
Minimum Output Voltage	$V_{COMPMIN}$	V_{FB} = 3V		0.4		V
CS to COMP Gain				2		V/V
Pre-Amp Gain				1		V/V
COMP Leakage Current		COMP = 2.5V			1	μA
OSCILLATOR						
Maximum Switching	f_{MAX}		108	120	132	kHz
Maximum Duty Cycle	D_{MAX}		65	75		%
Minimum Switching Frequency	f_{MIN}			1164		Hz

ELECTRICAL CHARACTERISTICS CONT'D

(V_{DD} = 18V, L_M = 0.5mH, R_{CS} = 0.75Ω, V_{OUT} = 13V, N_P = 68, N_S =12, N_A = 17, T_A = 25°C, unless otherwise specified,12V0.4A application)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Protection						
CS Short Waiting Time			2	2.25	3	μs
CS Short Detection Threshold				0.1	0.15	V
CS Open Threshold Voltage				1.75		V
Abnormal OCP Blanking Time				190		ns
Inductance Short CS Threshold Voltage				1.75		V
Thermal Shutdown Temperature				135		˚C
Thermal Hysteresis				20		˚C
Vo Short Detection Threshold	V_{FBUVLO}			0.28		V
Line UVLO	I_{FBUVLO}			0.2		mA
Line UVLO Hysteresis				20		μA
Line OVP	I_{FBOVP}			2.4		mA
VFB Over Voltage Protection				3		V
Valley Detection						
Valley Detection Time Window		V_{COMP} = 0.45V		3.3		μs

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ACT412 is a high performance peak current mode low-voltage PWM controller IC. The controller includes the most advance features that are required in the adaptor applications up to 36 Watt. Unique fast startup, frequency fold back, QR switching technique, accurate OLP, low standby mode operation, external compensation adjustment, short winding protection, OCP, OTP, OVP and UVLO are included in the controller.

Startup

Startup current of ACT412 is designed to be very low so that VDD could be charged to V_{DDON} threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, two 1MΩ, 1/8 W startup resistors could be used together with a VDD capacitor(4.7uF) to provide a fast startup and yet low power dissipation design solution.
During startup period, the IC begins to operate with minimum Ippk to minimize the switching stresses for the main switch, output diode and transformers. And then, the IC operates at maximum power output to achieve fast rise time. After this, V_{OUT} reaches about 90% V_{OUT}, the IC operates with a 'soft-landing' mode (decrease Ippk) to avoid output overshoot.

Constant Voltage (CV) Mode Operation

In constant voltage operation, the ACT412 senses the output voltage at FB pin through a resistor divider network R5 and R6 in Figure 2. The signal at FB pin is pre-amplified against the internal reference voltage, and the secondary side output voltage is extracted based on Active-Semi's proprietary filter architecture.

This error signal is then amplified by the internal error amplifier. When the secondary output voltage is above regulation, the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = 2.20V \times (1 + \frac{R_{FB1}}{R_{FB2}}) \times \frac{N_S}{N_A} - V_D \qquad (1)$$

where R_{FB1} (R5) and R_{FB2} (R6) are top and bottom feedback resistor, N_S and N_A are numbers of transformer secondary and auxiliary turns, and V_D is the rectifier diode forward drop voltage at approximately 0.1A bias.

Constant Power (CP) Mode Operation

When the secondary output current reaches a level set by the internal current limiting circuit, the ACT412 enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. An internal current shaping circuitry adjusts the switching frequency and current limit threshold slowly based on the flyback voltage so that the transferred power is fixed to the output voltage, resulting in a constant power at secondary side output power profile. Through correctly setting K1, K2, the energy transferred to the output during each switching cycle is ½(LP × ILIM^2) , where LP is the transformer primary inductance, ILIM is the primary peak current, Formula can be present as below:

$$P_{OUTCP} = \frac{1}{2} \times L_p \times (K_1 V_{CS\_TH})^2 \times \eta \times K_2 f_{SW} \qquad (2)$$

where f_{SW} is the switching frequency. The constant power operation typically extends down to 20% of nominal output voltage regulation.

Standby (No Load) Mode

In no load standby mode, the ACT412 oscillator frequency is further reduced to a minimum frequency while the current pulse is reduced to a minimum level to minimize standby power. The actual minimum switching frequency is programmable with an output preload resistor.

Loop Compensation

The ACT412 allows external loop compensation by connecting a capacitor to extend its applications, especially with different V_{OUT} in a wide output power range.

Primary Inductance Compensation

The ACT412 integrates a built-in primary inductance compensation circuit to maintain constant OLP despite variations in transformer manufacturing. The compensated ranges is +/-7%.

Primary Inductor Current Limit Compensation

The ACT412 integrates a primary inductor peak

FUNCTIONAL DESCRIPTION CONT'D

current limit compensation circuit to achieve constant power over wide line and wide load range.

Frequency Fold-back

When the load drops to 75% of full load level, ACT412 starts to decrease the switching frequency, which is proportional to the load current ,to improve the efficiency of the converter as show in Functional Block Diagram.

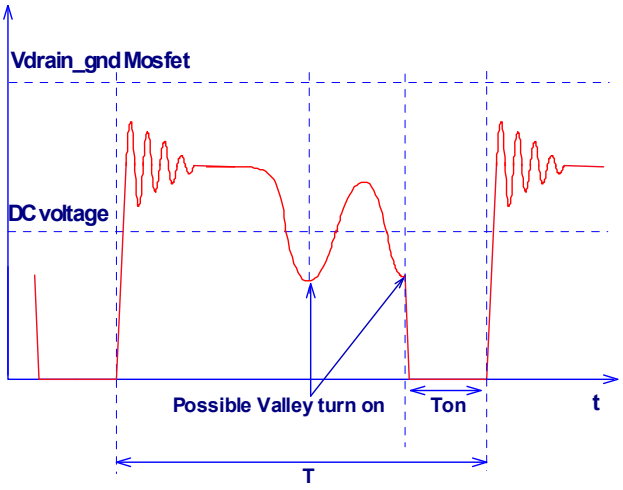
This enables the application to meet all latest green energy standards. The actual minimum switching frequency is programmable with a small dummy load (while still meeting standby power).

Valley Switching

ACT412 employed valley switching from medium load to heavy load to reduce switching loss and EMI. After the switch is turned off, the ringing voltage from the auxiliary winding is applied to the VFB pin through feedback network R5, R6. Internally, the VFB pin is connected to an zero-crossing detector to generate the switch turn on signal when the conditions are met. In light load, the frequency fold back scheme starts to take control to determine the switch turn on signal, so thus the switching frequency.

Figure 1:

Valley Switching at heavy load



Protection Features

The ACT412 provides full protection functions. The following table summarizes all protection functions.

Auto-Restart Operation

ACT412 will enter auto-restart mode when a fault is identified. There is a startup phase in the auto-restart mode. After this startup phase the conditions are checked whether the failure is still present. Normal operation proceeds once the failure mode is removed. Otherwise, new startup phase will be initiated again.

PROTECTION FUNCTIONS	FAILURE CONDITION	PROTECTION MODE
V_{DD} Over Voltage	V_{DD} > 20.5V (4 duty cycle)	Auto Restart
VFB Over Voltage	V_{FB} > 3V (4 duty cycle)	Auto Restart
Over Temperature	T > 135°C	Auto Restart
Short Winding/ Short Diode	V_{CS} > 1.75V	Auto Restart
Over Load	IPK = I_{LIMIT}	Auto Restart
Output Short Circuit	V_{FB} < 0.28V	Auto Restart
Open Loop	No switching for 4 cycle	Auto Restart
V_{CC} Under Voltage	V_{CC} < 6.8V	Auto Restart

To reduce the power loss during fault mode, the startup delay control is implemented. The startup delay time increases over lines.

Short Circuit Protection

When the secondary side output is short circuited, the ACT412 enters hiccup mode operation. This hiccup behavior continues until the short circuit is removed.

FB Over Voltage Protection

The ACT412 includes output over-voltage protection circuitry, which shuts down the IC when the output voltage is 40% above the normal regulation voltage 4 consecutive switching cycles. The ACT412 enters hiccup mode when an output over voltage fault is detected.

VDD Over Voltage Protection

ACT412 can monitor the converter output voltage. The voltage generated by the auxiliary winding tracks converter's output voltage through VDD, which is in proportion to the turn ratio (V_{OUT}+V_{DIODE}) xN_A/N_S. When the V_{OUT} is abnormally higher than design value for four consecutive cycles, IC will

TYPICAL APPLICATION CONT'D

enter the restart process. A counter is used to reduce sensitivity to noise and prevent the auto start unnecessary.

Open Loop Protection

ACT412 is able to protect itself from damage when the control loop is open. The typical open loop condition includes either VFB floating or RFB5 open.

Over Temperature Shutdown

The thermal shutdown circuitry detects the ACT412 die temperature. The threshold is set at typical 135˚C. When the die temperature rises above this threshold (135˚C) the ACT412 is disabled and remains disabled until the die temperature falls below 115˚C, at which point the ACT412 is re-enabled.

TYPICAL APPLICATION CONT'D

Design Example

The design example below gives the procedure for a DCM fly back converter using an ACT412. Refer to Application Circuit Figure 2, the design for an adapter application starts with the following specification:

Input Voltage Range	90VAC - 265VAC, 50/60Hz
Output Power, P_O	5W
Output Voltage, V_{OUTCV}	12V
Full Load Current, I_{OUTFL}	0.4A
CC Current, I_{OUTMAX}	1.8A
System Efficiency CV, η	0.75

The operation for the circuit shown in Figure 1 is as follows: the rectifier bridge D1-D4 and the capacitor C1/C2 convert the AC line voltage to DC. This voltage supplies the primary winding of the transformer T1 and the startup resistor R7/R8 to VDD pin of ACT412 and C4. The primary power current path is formed by the transformer's primary winding, the mosfet, and the current sense resistor R9. The resistors R3, R2, diode D5 and capacitor C3 create a snubber clamping network that protects Q1 from voltage spike from the transformer primary winding leakage inductance. The network consisting of capacitor C4, diode D6 and resistor R4 provides a VDD supply voltage for ACT412 from the auxiliary winding of the transformer. The resistor R4 is optional, which filters out spikes and noise to makes VDD more stable. C4 is the decoupling capacitor of the supply voltage and energy storage component for startup. During power startup, the current charges C4 through startup resistor R7/R8 from the rectified high voltage. The diode D8 and the capacitor C5/C6 rectify filter the output voltage. The resistor divider consists of R5 and R6 programs the output voltage.

Since a bridge rectifier and bulk input capacitors are used, the resulting minimum and maximum DC input voltages can be calculated:

$$V_{INDC\_MIN} = \sqrt{2V_{INAC\_MIN}^2 - \frac{2P_{OUT}\left(\frac{1}{2f_L} - t_C\right)}{\eta \times C_{IN}}}$$
$$= \sqrt{2 \times 85^2 - \frac{2 \times 5 \times \left(\frac{1}{2 \times 47} - 3.5ms\right)}{0.75 \times 2 \times 6.8\mu F}} \approx 90V \quad (3)$$

$$V_{IN(MAX)DC} = \sqrt{2} \times V_{IN(MAX)AC}$$
$$= \sqrt{2} \times (265\,V_{AC}) = 375\,V \quad (4)$$

Where η is the estimated circuit efficiency, f_L is the line frequency, t_C is the estimated rectifier conduction time, C_{IN} is empirically selected to be 2x6.8μF electrolytic capacitors.

The full load system duty cycle is set to be 40% at low line voltage 85VAC and the circuit efficiency is estimated to be 75%. Then the average input current at full load is:

$$I_{IN\_FL} = \frac{P_{OUT\_FL}}{V_{INDC\_MIN} \times \eta}$$
$$= \frac{5}{90 \times 0.75} \approx 75\ mA \quad (5)$$

The input primary peak current at full load:

$$I_{ppk\_FL} = \frac{2 \times L_{IN\_FL}}{D_{FL}} = \frac{2 \times 75}{0.4} = 375\ mA \quad (6)$$

The primary inductance of the transformer:

$$L_p = \frac{V_{INDC\_MIN} D_{FL}}{I_{ppk\_FL} \times f_s}$$
$$= \frac{90 \times 0.4}{375\ mA \times 130\ k} \approx 0.74\ mH \quad (7)$$

The primary turns on time at full load:

$$T_{ON\_FL} = L_p \frac{I_{ppk\_FL}}{V_{INDC\_MIN}}$$
$$= \frac{0.74\,mH \times 375\,mA}{90} = 3.08\,\mu s \quad (8)$$

The ringing periods from primary inductance with mosfet Drain-Source capacitor:

$$T_{RINGING\_MAX} = 2\pi\sqrt{L_{p\_MAX} C_{DS\_MAX}}$$
$$= 2 \times 3.14 \times \sqrt{0.73mH \times (1+7\%) \times 100PF} = 1.76\,\mu s \quad (9)$$

Design only an half ringing cycle at maximum load in minimum low line, so secondly reset time:

$$T_{RST} = T_{SW} - T_{ON\_FL} - 0.5T_{RINGING\_MAX}$$
$$= 1/130kHz - 3.08\,\mu s - 0.5 \times 1.76\,\mu s = 3.73\,\mu s \quad (10)$$

Base on conservation of energy and transformer transform identity, the primary to secondary turns ratio N_P/N_S:

$$\frac{N_P}{N_S} = \frac{T_{ON}}{T_{RST}} \times \frac{V_{IN\_MIN}}{V_{OUT} + V_D}$$
$$= \frac{3.08}{3.73} \times \frac{90}{13 + 0.45} = 5.53 \quad (11)$$

The auxiliary to secondary turns ratio N_A/N_S:

$$\frac{N_A}{N_S} = \frac{V_{DD} + V_D'}{V_{OUT} + V_D} = \frac{18 + 0.45}{13 + 0.45} = 1.37 \quad (12)$$

TYPICAL APPLICATION CONT'D

An EE16 core is selected for the transformer. From the manufacture's catalogue recommendation, the core with an effective area A_E is 19.2mm^2 .The turn of the primary winding is:

$$N_P \geq \frac{I_{lim} \times L_{p\_max}}{A_E \times B_{max}} = \frac{0.75 \times 0.00073}{19.2 \times 3000 \times 10^{-10}} = 95T \quad (13)$$

$$I_{lim} = 2 \times I_{p\_FL} = 2 \times 375\,mA \approx 750\,mA \quad (14)$$

The turns of secondary and auxiliary winding can be derived accordingly:

$$N_s = N_p / \frac{N_p}{N_S} = 95 / 5.53 \approx 17\,T$$
$$N_A = \frac{N_A}{N_S} \times N_s = 1.4 \times 17 \approx 24\,T \quad (15)$$

Determining the value of the current sense resistor (R9) uses the peak current in the design. Since the ACT412 internal current limit is set to 1V, the design of the current sense resistor is given by:

$$R_{CS} = \frac{V_{CS}}{I_{lim}} = \frac{1}{0.75} \approx 1.3.\Omega \quad (16)$$

The voltage feedback resistors are selected according to frequency at full load. The design frequency at full load is given by:

$$f_s = \frac{N_p}{N_s} \times \frac{R_{fb1} \times R_{fb2}}{R_{fb1} + R_{fb2}} \times \frac{V_O + V_D}{L_p \times \frac{V_{cs}}{R_{cs}} \times K_{f\_sw}} \quad (17)$$

The design Vo is given by:

$$V_o = (1 + \frac{R_{fb1}}{R_{fb2}}) \times \frac{N_s}{N_a} \times V_{FB} - V_D \quad (18)$$

Where k is IC constant and K=0.0000065, then we can get the value:

$$R_{fb1} = 45.3K, R_{fb2} = 6.9K \quad (19)$$

When selecting the output capacitor, a low ESR electrolytic capacitor is recommended to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C_{OUT} = \frac{I_{OUT}}{f_{sw} \times V_{RIPPLE}} = \frac{1.8}{110k \times 50mV} = 327\mu F \quad (20)$$

Two 330µF electrolytic capacitors are used to keep the ripple small.

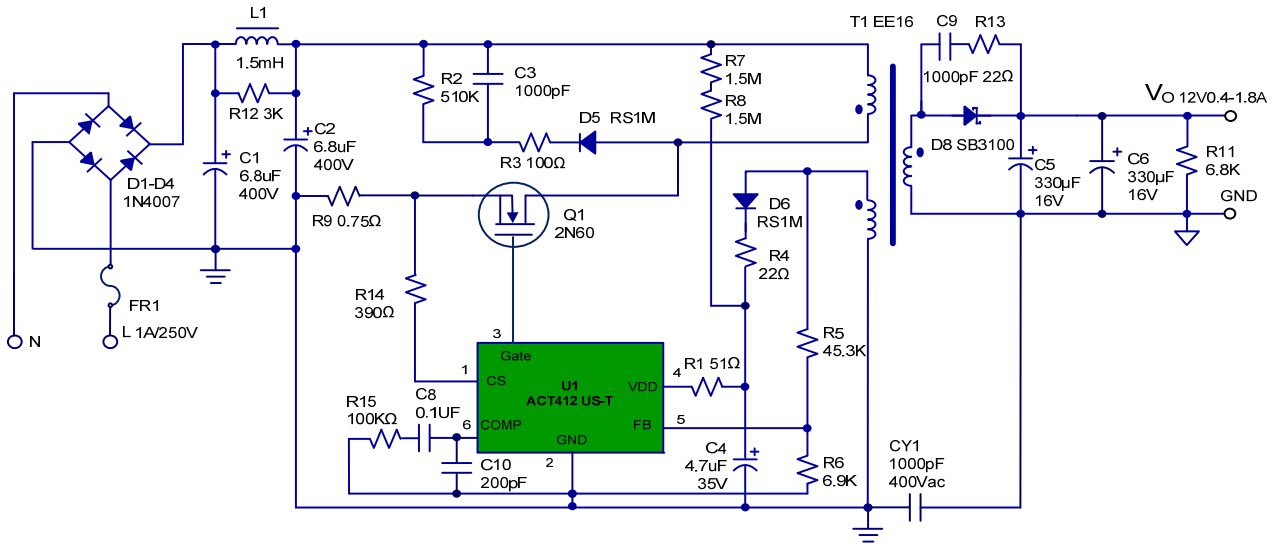
In fact, consider of transformer production, we scale down the turn ratio and inductance.

$$N_p = 68T, N_s = 12T, N_A = 17T, L_p = 0.5mH \quad (21)$$

PCB Layout Guideline

Good PCB layout is critical to have optimal performance. Decoupling capacitor (C4) and feedback resistor (R5/R6) should be placed close to VDD and FB pin respectively. There are two main power path loops. One is formed by C1/C2, primary winding, Mosfet transistor and current sense resistor (R9). The other is secondary winding, rectifier D8 and output capacitors (C5/C6). Keep these loop areas as small as possible. Connecting high current ground returns, the input capacitor ground lead, and the ACT412 GND pin to a single point (star ground configuration).

Figure 2:
ACT412, Universal VAC Input, 12V/400mA Output Charger



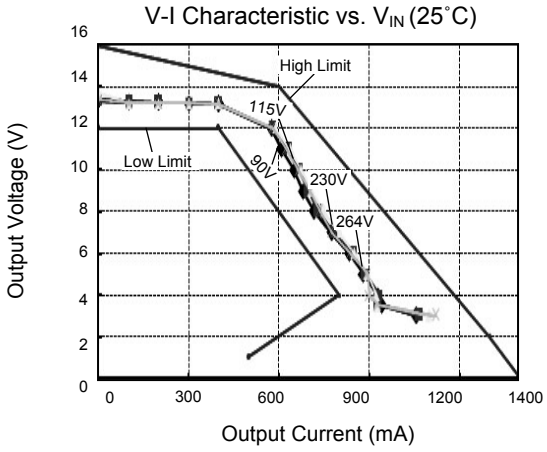


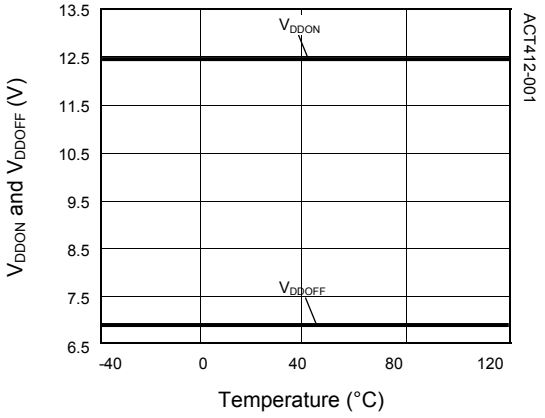
Table 2:

ACT412 Bill of Materials

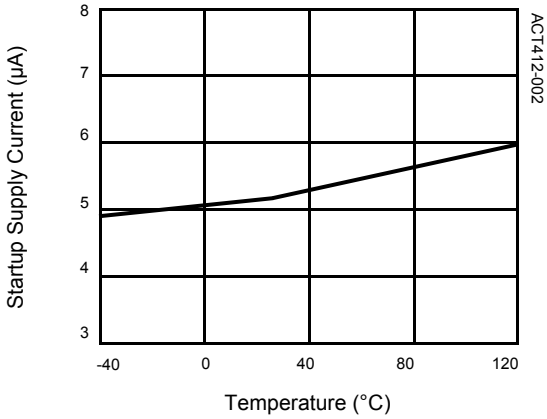
ITEM	REFERENCE	DESCRIPTION	QTY	MANUFACTURER
1	U1	IC, ACT412,SOT23-6	1	Active-Semi.
2	C1,C2	Capacitor, Electrolytic, 6.8μF/400V, 10x12mm	2	KSC
3	C3	Capacitor, Ceramic, 1000pF/500V, 0805,SMD	1	POE
4	C4	Capacitor, Electrolytic,4.7μF/35V,5x11mm	1	KSC
5	C5,C6	Capacitor, Electrolytic, 330μF/16V, 8x11.5mm	2	KSC
6	C8	Capacitor, Ceramic, 0.1μF/25V, 0805,SMD	1	POE
7	C9	Capacitor, Ceramic, 1000pF/100V, 0805,SMD	1	POE
8	C10	Capacitor, Ceramic, 200pF/50V, 0805,SMD	1	POE
9	CY1	Safety Y1,Capacitor,1000pF/400V,Dip	1	UXT
10	D1-D4	Diode,Rectifier,1000V/1A,1N4007, DO-41	4	Good-Ark
11	D5	Fast Recovery Rectifier, RS1M,1000V/1.0A, RMA	1	PANJIT
12	D6	Fast Recovery Rectifier,RS1D,200V/1.0A,SMA	1	PANJIT
13	D7	NC		
14	D8	Diode, schottky, 100V/3A, SB3100, DO-47	1	Good-Ark
15	L1	Axial Inductor, 1.5mH, 5*7,Dip	1	SoKa
16	L2	Axial Inductor, 0.55*5T, 5*7,Dip	1	SoKa
17	Q1	Mosfet Transistor, 4N60,TO-220	1	Infineon
18	PCB1	PCB, L*W*T=52.2x30x1.6mm,Cem-1,Rev:A	1	Jintong
19	FR1	Fuse,1A/250V	1	TY-OHM
20	R1	Chip Resistor, 51Ω, 0805, 5%	1	TY-OHM
21	R2	Chip Resistor, 510KΩ, 1206, 5%	1	TY-OHM
22	R3	Chip Resistor, 100Ω, 0805, 5%	1	TY-OHM
23	R4,R13	Chip Resistor, 22Ω, 0805, 5%	2	TY-OHM
24	R5	Chip Resistor, 45.3KΩ, 0805,1%	1	TY-OHM
25	R6	Chip Resistor, 6.9KΩ, 0805, 1%	1	TY-OHM
26	R7,R8	Chip Resistor, 1.5MΩ, 0805 , 5%	2	TY-OHM
27	R9	Chip Resistor, 0.75Ω, 1206,1%	1	TY-OHM
28	R11	Chip Resistor, 6.8KΩ, 0805, 5%	1	TY-OHM
29	R12	Chip Resistor, 3KΩ, 0805 , 5%	1	TY-OHM
30	R14	Chip Resistor, 390Ω, 0805 , 5%	1	TY-OHM
31	R15	Chip Resistor, 100KΩ, 0805 , 5%	1	TY-OHM
32	T1	Transformer, Lp=0.5mH, EE16	1	

TYPICAL PERFORMANCE CHARACTERISTICS

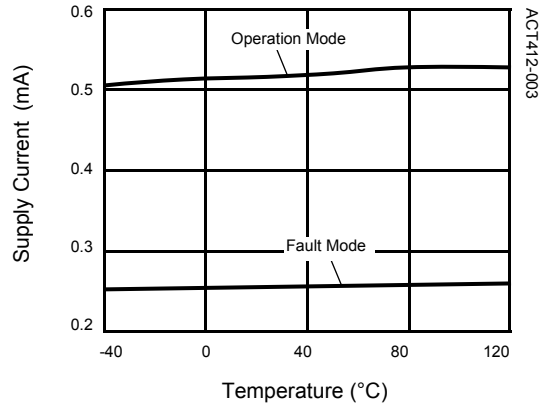
VDD ON/OFF Voltage vs. Temperature



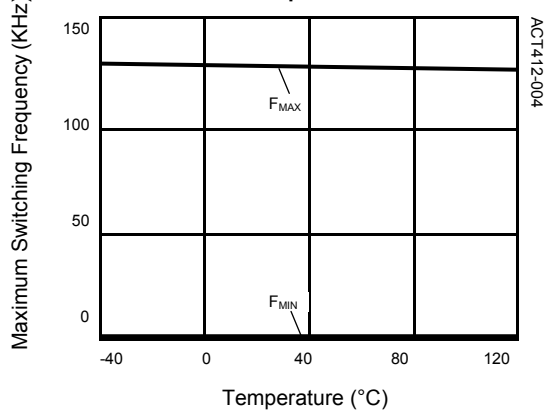
Startup Supply Current vs. Temperature



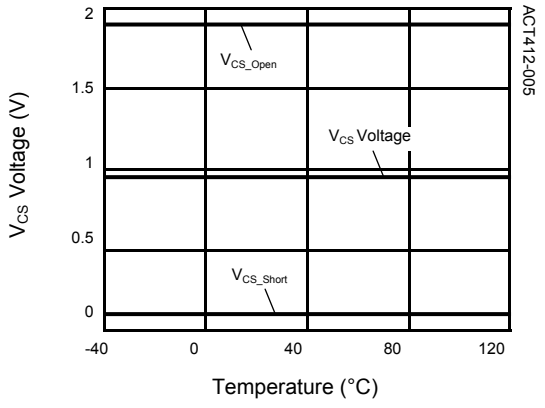
Supply Current at Operation/Fault Mode vs. Temperature



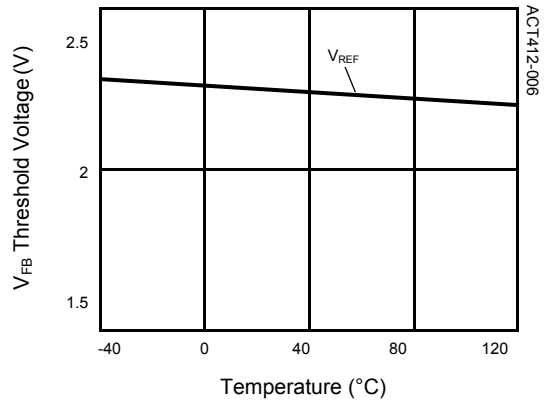
Maximum/Minimum Switching Frequency vs. Temperature



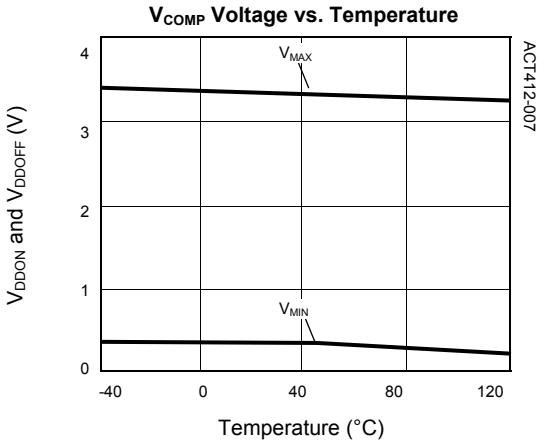
V_{CS} Voltage vs. Temperature



V_{FB} Threshold Voltage vs. Temperature

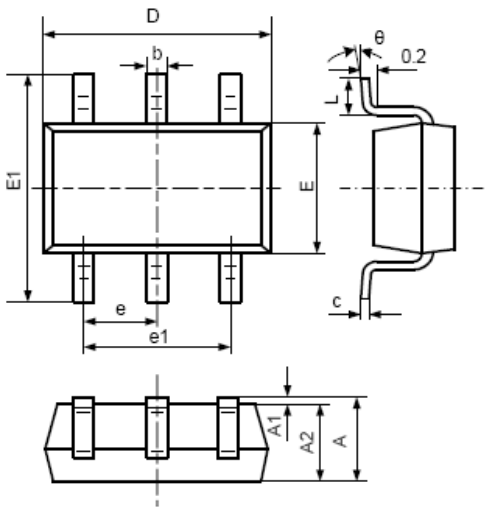


TYPICAL PERFORMANCE CHARACTERISTICS



PACKAGE OUTLINE

SOT23-6 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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