AN5693K

Luminance, chroma and sync. signals processing IC (with built-in I²C-bus interface) for PAL/NTSC color-TV

■ Overview

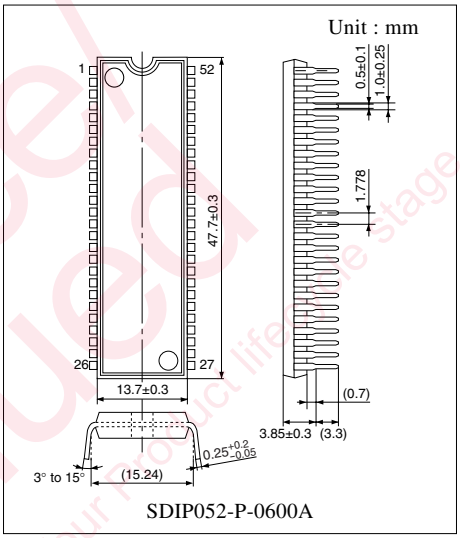
The AN5693K is an IC that processes PAL-and NTSC-compatible video,chroma,RGB and sync. signals.

■ Features

- Built-in I²C-bus control interface.
- SECAM-compatible together with the AN5637 SECAM signal processing IC.

■ Applications

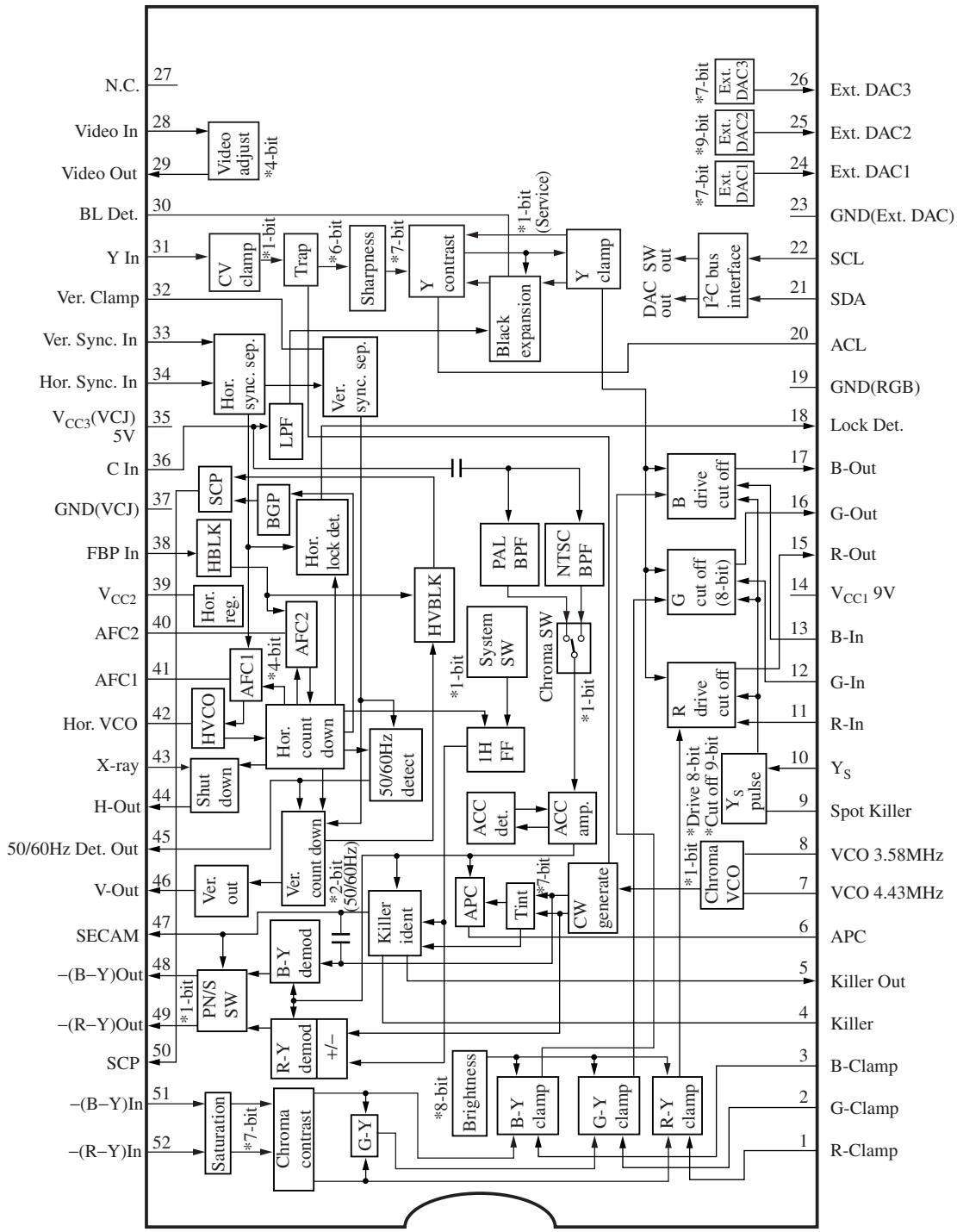
- TV (Multi-system compatible)



SDIP052-P-0600A

Note) The package of this product will be changed to lead-free type (SDIP052-P-0600F). See the new package dimensions section later of this datasheet.

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	(R−Y)Clamp	27	N.C.
2	(G−Y)Clamp	28	Video Level Adjust Input
3	(B−Y)Clamp	29	Video Level Adjust Output
4	Killer Filter	30	Black Level Det/Blank Off SW
5	Killer Output	31	Y Input
6	Chroma APC Filter	32	Ver. Sync. Clamp
7	Chroma VCO 4.43 MHz	33	Ver. Sync. Input
8	Chroma VCO 3.58 MHz	34	Hor. Sync. Input
9	Spot Killer	35	V_{CC3}(Chroma/Jungle/DAC)
10	Y_S Input(Fast Blanking)	36	Chroma Input/Black Exp. Start
11	External R Input	37	GND(Video/Chroma/Jungle)
12	External G Input	38	FBP Input
13	External B Input	39	V_{CC2}(Hor. Stability Supply)
14	V_{CC1}	40	Hor. AFC 2 Filter
15	R Output	41	Hor. AFC 1 Filter
16	G Output	42	Hor. VCO(32 f_H)
17	B Output	43	X-Ray Protection Input
18	Hor. Lock Detect	44	Hor.Pulse Output
19	GND(RGB/I^2C/DAC)	45	Ver. 50/60 Hz Detect Output
20	ACL	46	Ver. Pulse Output
21	SDA	47	SECAM Interface/CW Output
22	SCL	48	−(B−Y)Output
23	GND(EXT DAC)	49	−(R−Y)Output
24	External DAC 1 DC	50	Sandcastle Pulse Output
25	External DAC 2 DC	51	−(B−Y)Input
26	External DAC 3 DC	52	−(R−Y)Input

■ Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
Power supply voltage	V_{CC}	V_{CC1}(14)	10.5	V
		V_{CC3}(35)	6.0	
Power supply current	I_{CC}	I_{14}	77	mA
		I_{35}	119	
		I_{39}	27	
Power dissipation *2	P_D	1 372		mW
Operating ambient temperature *1	T_{opr}	−20 to +70		°C
Storage temperature *1	T_{stg}	−55 to +150		°C

Note) *1: Except for the operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.
*2: The power dissipation shown is the value for T_a = 70°C. (Refer to "Technical Information")

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Operating supply voltage range	V_{CC1}	8.1 to 9.9	V
	V_{CC3}	4.5 to 5.5	
Operating supply pin voltage	V_5	0 to 6	V
	V_9	0 to V_{14}	
	V_{10}	0 to 6	
	V_{11}	0 to 6	
	V_{12}	0 to 6	
	V_{13}	0 to 6	
	V_{21}	0 to 6	
	V_{22}	0 to 6	
	V_{24}	0 to V_{14}	
	V_{25}	0 to V_{14}	
	V_{36}	0 to V_{14}	
	V_{38}	0 to V_{47}	
	V_{43}	0 to 2	
	V_{45}	0 to 6	
	V_{47}	0 to V_{14}	

Note) Do not apply external currents or voltage to any pins not specifically mentioned.
For ciicuit currents, '+' denotes current flowing into the IC, and '−' denotes current flowing out of the IC.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Operating supply circuit current	I_{39}	10 to 25	mA
	I_{15}	− 6.0 to + 0.6	
	I_{16}	− 6.0 to + 0.6	
	I_{17}	− 6.0 to + 0.6	
	I_{28}	− 0.3 to + 0.1	
	I_{29}	− 2.4 to + 0.8	
	I_{33}	− 0.8 to + 0.1	
	I_{34}	− 0.8 to + 0.1	
	I_{44}	− 6.4 to + 0.1	
	I_{46}	− 0.8 to + 0.1	
	I_{47}	− 0.3 to + 0.1	

Note) Do not apply external currents or voltage to any pins not specifically mentioned.
For ciicuit currents, '+' denotes current flowing into the IC, and '−' denotes current flowing out of the IC.

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply DAC data is standard.						
Supply current 1	I_{14}	Current when V_{14} = 9 V	38	48	58	mA
Supply current 2	I_{35}	Current when V_{35} = 5 V	48	60	72	mA
Steady state supply voltage	V_{39}	When pin 39 current I = 15 mA, pin 39 voltage	5.8	6.5	7.2	V
Steady state supply Current	I_{39}	Current when V_{39} = 5 V	2	5	7	mA
Steady state supply input resistance	R_{39}	DC measurement input resistance when I_{39} = 10 mA to 25 mA	1	5	10	Ω
Interface						
Video adjust gain	V_{PO}	DC measurement $20 \log \frac{\text{output (0A = F8)}}{\text{output (0A = 08)}}$	5	6	7	dB
Video adjust output resistance	R_{O29}	DC measurement	70	120	170	Ω
External DAC 1 DC voltage (max.)	$V_{EXT1max}$	Pin 24 DC voltage when DAC 0C = 00 DC measurement	3.10	3.40	3.70	V
External DAC 1 DC voltage (min.)	$V_{EXT1min}$	Pin 24 DC voltage when DAC 0C = 7F DC measurement	2.10	2.40	2.70	V
External DAC 2 DC voltage (max.)	$V_{EXT2max}$	Pin 25 DC voltage DAC 0B = 00, 04D7 = 0 DC measurement	7.8	8.1	8.7	V
External DAC 2 DC voltage (min.)	$V_{EXT2min}$	Pin 25 DC voltage DAC 0B = FF, 04D7 = 1 DC measurement	0.1	0.8	1.0	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interface (continued)						
External DAC 3 DC voltage (max.)	$V_{EXT3max}$	Pin 26 DC voltage when DAC 0D = 7F DC measurement	5.50	6.00	6.50	V
External DAC 3 DC voltage (min.)	$V_{EXT3min}$	Pin 26 DC voltage when DAC 0D = 00 DC measurement	0.90	1.00	1.15	V
External DAC 1 maximum output current	$I_{EXT1max}$	Pin 24 DC current when DAC 0C = 7F DC measurement	200	—	—	µA
External DAC 3 maximum output current	$I_{EXT3max}$	Pin 26 DC current when DAC 0D = 7F DC measurement	1.0	—	—	mA
Video signal processing	Input: 0.6 V_{PP} (V_{WB} = 0.42 V_{0P} stair-step) at G-out					
Video output (typ.)	V_{YO}	DAC 03 = 40(typ.),(Contrast)	1.65	2.10	2.55	V_{PP}
Video output (max.)	V_{YOmax}	DAC 03 = 7F(max.),(Contrast)	3.60	4.50	5.35	V_{PP}
Video output (min.)	V_{YOmin}	DAC 03 = 00(min.),(Contrast)	0.07	0.25	0.50	V_{PP}
Contrast variable range	$Y_{Cmax/min}$	DAC 03 = 7F,DAC 03 = 00	20	25	33	dB
Video frequency characteristics	f_{YC}	f = 0.2 MHz as reference to −3 dB. DAC 0E D1 = 1,DAC 04 = 00(Sharp)	5.5	6.8	—	MHz
Sharpness variable range	$Y_{Smax/min}$	f = 3.8 MHz,DAC 0E D1 = 1 Sharp : (04 3F)/(04 00)	9	13	17	dB
Pedestal level (typ.)	V_{PED}	DAC 02 = 80(typ.),(Brightness)	1.9	2.5	3.1	V
Pedestal variable range	ΔV_{PED}	Difference between DAC 02 = 00 & FF (Brightness)	2.0	2.6	3.2	V
Brightness control sensitivity	ΔV_{BRT}	Average variable range of DAC 02 = 60 & A0	8	11	14	mV/step
Video input clamp voltage	V_{YCLP}	Pin 31 clamp voltage	3.2	3.7	4.2	V
ACL sensitivity	ACL	When V_{20} = 3.0 V−3.5 V 2 times of Y-out increase	2.1	2.7	3.2	V/V
Blanking off threshold voltage	V_{BOFF}	Reduse pin 30 voltage; the voltage when blanking is off	0.3	0.5	0.9	V
Blanking level	V_{YBL}	Blanking pulse DC voltage.	0.5	1.0	1.5	V
DC transmission quantity	T_{DC}	APL : 10% to 90%,TDC $TDC \frac{(\Delta AC - \Delta DC)\ 100\%}{\Delta AC}$	9	100	110	%
Video input clamp current	I_{YCLP}	DC measurement IC : internal sink current	8	13	18	µA
ACL start point	V_{ACL}	ACL pin 20 voltage reduces from 5 V until output is lesser by 10%	3.4	3.7	4.0	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing	All tests on: Burst 300 mV_{PP} (PAL), typ.: B-out					
Color difference output (typ.)	V_{COtyp}	Input: Color bar DAC 00 = 40(typ.), DAC 03 = 40(typ.)	2.6	3.3	4.0	V_{PP}
Color difference output (max.)	V_{COmax}	Input: Color bar DAC 00 = 7F, DAC 03 = 40	2.3	3.0	—	V_{OP}
Color difference output (min.)	V_{COmin}	Input: Color bar DAC 00 = 00, DAC 03 =40	0	—	100	mV_{PP}
Chroma contrast variable range	$C_{Cmax/min}$	DAC 00 = 40,DAC 03 = 7F,DAC 03 = 00	20	25	33	dB
ACC.characteristics 1	ACC1	Input: Rainbow Burst increase from 300 mV_{PP} → 600 mV_{PP}	0.9	1.0	1.2	Times
ACC.characteristics 2	ACC2	Input: Rainbow Burst decrease from 300 mV_{PP} → 60 mV_{PP}	0.7	1.0	1.1	Times
NTSC tint centre	$\Delta\theta_C$	Difference between DAC 01 = 40 & when tint is centre	−13	0	13	Step
NTSC tint adjustable range 1	$\Delta\theta_1$	Input: Rainbow, DAC 01 = 7F(Tint)	30	50	65	Deg
NTSC tint adjustable range 2	$\Delta\theta_2$	Input: Rainbow, DAC 01 = 00(Tint)	−65	−50	−30	Deg
Demodulation output ratio (R) PAL,NTSC	R/B	Input: Rainbow Ratio of R-out/B-out	0.71	0.83	0.95	Times
Demodulation output ratio (G) PAL,NTSC	G/B	Input: Rainbow Ratio of G-out/B-out	0.31	0.37	0.43	Times
Color difference output angle (R) PAL,NTSC	∠R	Input: Rainbow	78	90	102	Deg
Color difference output angle (G) PAL,NTSC	∠G	Input: Rainbow	224	236	248	Deg
Color killer tolerance (PAL)	V_{KILLP}	Input: Color bar, 0 dB = 300 mV_{PP} Attenuate input level	−57	−44	−34	dB
Color killer tolerance (NTSC)	V_{KILLN}	Input: Color bar, 0 dB = 300 mV_{PP} Attenuate input level	−57	−44	−34	dB
APC pull-in range (H) PAL,NTSC	f_{CPH}	Input: Color bar High side pull-in range	450	900	—	Hz
APC pull-in range (L) PAL,NTSC	f_{CPL}	Input: Color bar Low side pull-in range	—	−900	− 450	Hz
Color killer detector output voltage (Color)	V_{KC}	Voltage at pin 5 when chroma signal is inputed	4.5	5.0	—	V
Color killer detector output voltage (B/W)	V_{KBW}	Voltage at pin 5 when no chroma signal is inputed	0	0.1	0.5	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing (continued)		All tests on: Burst 300 mV_{PP} (PAL), typ.: B-out				
Demodulation output−(B−Y) PAL,NTSC	V_{DB}	Input: Color bar (NTSC: Adjust to tint centre)Measure pin 48	555	695	835	mV_{PP}
Demodulation output−(R−Y) PAL,NTSC	V_{DR}	Input: Color bar (NTSC: Adjust to tint centre)Measure pin 49	430	540	650	mV_{PP}
Demodulation output angle ∠B PAL,NTSC	$\angle R_{DB}$	Input: Rainbow Phase difference of B−Y axis	−5	0	5	Deg
Demodulation output angle ∠R PAL,NTSC	$\angle R_{DR}$	Input: Rainbow Phase difference of B−Y and R−Y axis	85	90	95	Deg
CW output level(4.43 MHz)	V_{CWP}	AC component at pin 47 when VCO is at 4.43 MHz	250	300	350	mV_{PP}
CW output level(3.58 MHz)	V_{CWN}	AC component at pin 47 when VCO is at 3.58 MHz	—	0	50	mV_{PP}
SECAM output CW period	T_{CW}	Period of CW is outputed when in SECAM	1.31	1.41	1.51	ms
SECAM detector current	I_{SECAM}	Minimum current from pin 47 when SECAM is detected	50	100	150	µs
PAL/NTSC output DC voltage	V_{47PN}	PAL/NTSC output DC voltage at pin 47	0.80	1.30	1.65	V
SECAM output DC voltage	V_{47S}	SECAM output DC voltage at pin 47	4.1	4.6	5.1	V
Demodulation output impedance (PAL/NTSC) −(R−Y), −(B−Y)	$R_{O48,49PN}$	Pin impadance of pin 48, pin 49 in PAL/ NTSC mode	390	480	570	Ω
Demodulation output impedance (SECAM) −(R−Y), −(B−Y)	$R_{O48,49S}$	Pin impadance of pin 48, pin 49 in SECAM mode	100	—	—	kΩ
RGB processing		DAC data standard				
Pedestal difference voltage	ΔV_{IPL}	R,G,B out pedestal difference voltage	0	—	0.3	V
Brightness voltage tracking	ΔV_{BL}	DAC 02 = 40 to C0 (Brightness). Ratio of variable level	0.9	1.0	1.1	Times
Video voltage gain ratio	ΔG_{YC}	R,B out output ratio with G-out	0.8	1.0	1.2	Times
Video voltage gain tracking	ΔT_{CONT}	DAC 03 = 20 to 60 ratio (contrast) of gain	0.9	1.0	1.1	$\frac{\text{Times}}{\text{Times}}$
Driver control characteristics	G_{DV}	R,B out AC adj. amount Driver DAC 08 = 00 to FF Driver DAC 09 = 00 to FF	5.3	6.3	7.3	dB
Cut-off control characteristics	V_{CUTOFF}	R,G,B output DC cut off DAC range from min.to max.	1.9	2.4	2.9	V
Y_S threshold voltage	V_{YS}	Smallest level when Y_S is on	0.7	1.0	1.3	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RGB processing (continued) DAC data standard						
External RGB DC Voltage	V_{EPL}	Y_S is on	1.7	2.3	2.9	V
External RGB pedestal difference voltage(R/B)(G/B)	ΔV_{EPL}	Y_S is on	0	—	250	mV
Internal/External pedestal difference voltage	$\Delta V_{PL/IE}$	Internal–External	50	200	400	mV
External RGB output Voltage	V_{ERGB}	Input 3 V_{PP}, DAC 03 = 7F(Contrast)	4.3	5.4	6.5	V_{PP}
External RGB output difference voltage	ΔV_{ERGB}	Input 3 V_{PP}, DAC 03 = 7F(Contrast)	− 0.6	0	+ 0.6	V
External RGB contrast control characteristics	$E_{Cmax/min}$	DAC 03 = 7F, DAC 03 = 00	10	13	16	dB
External RGB frequency characteristics	f_{RGBC}	Input 0.2 V_{PP}, DC = 1 V	8	12	—	MHz
Synchronizing signal processing						
Horizontal output free run frequency	f_{HO}	No input signal The frequency at pin 44	15.33	15.63	15.93	kHz
Horizontal output pulse duty	τ_{HO}	Horizontal output pulse's high level's duty	31	37	43	%
Horizontal output pull-in range	f_{HP}	Horizontal sync. sep. freq. pull-in approaching 15.625 kHz	± 500	± 650	—	Hz
Vertical free run frequency (PAL)	f_{VO-P}	Forced 50 Hz mode, DAC 0E-D2 = 1 D3 = 0, No sync.signal input	48	50	52	Hz
Vertical free run frequency (NTSC)	f_{VO-N}	Forced 60 Hz mode, DAC 0E-D2 = 1 D3 = 1, No sync.signal input	58	60	62	Hz
Vertical output pulse width NTSC,PAL	τ_{VO}	Hor. & Ver.sync. condition,the pulse width at pin 46	9	10	11	1/fH
Vertical pull-in range (PAL)	f_{VPP}	f_H = 15.625 kHz, Forced 50 Hz mode	46	—	54	Hz
Vertical pull-in range (NTSC)	f_{VPN}	f_H = 15.75 kHz, Forced 60 Hz mode	56	—	64	Hz
Horizontal output voltage (H)	V_{44H}	Horizontal output pulse's high level's DC voltage	3.2	3.5	3.8	V
Horizontal output voltage (L)	V_{44L}	Horizontal output pulse's low level's DC voltage	0	—	0.3	V
Vertical output voltage (H)	V_{46H}	Vertical output pulse's high level's DC voltage	3.9	4.2	4.5	V
Vertical output voltage (L)	V_{46L}	Vertical output pulse's low level's DC voltage	0	—	0.3	V
Screen centre variable range	ΔT_{HC}	Variable amount of phase between H_{SYNC} & H_{OUT} DAC 0A = 80 to 8F	2.6	3.2	4.4	µs

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Synchronizing signal processing (continued)						
Shut down operating	V_{43L}	Pin 43 minimum voltage when H-out does not appear	0.60	0.68	0.76	V
Vertical frequency detection operation (50 Hz)	f_{50}	Vertical input freq.when the DC level at pin 45 = "L"(< 0.5 V)	47	—	55	Hz
Vertical frequency detection operation (60 Hz)	f_{60}	Vertical input freq. when the DC level at pin 45 = "H"(> 4.5 V)	57	—	63	Hz
Sync. separation input clamp voltage (Vertical)	V_{33}	V_{33} clamp voltage	1.0	1.3	1.6	V
Sync. separation input clamp voltage (Horizontal)	V_{34}	V_{34} clamp voltage	1.0	1.3	1.6	V
Horizontal output start voltage	V_{fHS}	Minimum V_{38} when horizontal output is above 1 V_{PP}, fo > 10 kHz	3.4	4.2	5.0	V
I²C interface						
Sinking current at ACK	I_{ACK}	When ACK, pin21 pin current with 2.2 kΩ pull-up to 5 V	1.8	2.5	5.0	mA
SCL,SDA signal input high level	V_{IHI}	—	3.1	—	5.0	V
SCL,SDA signal input low level	V_{ILO}	—	0	—	0.9	V
Input possible maximum frequency	f_{Imax}	—	100	—	—	Kbit/s

• Reference data for design

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video signal processing	Input: 0.6 V_{PP} (V_{WB} = 0.42 V_{0P} stair-step) at G-out					
Y signal delay time	t_{DL}	Measure output's delay time with input (PAL = 4.43 MHz)	620	690	760	ns
Black level correction 1	V_{BLC1}	All black input. Find the diff.of G-out when pin 30 is 9 V & open	−100	0	+100	mV
Black level correction 2	V_{BLC2}	All black input. Find the diff.of G-out when pin 30 is 3 V & 9 V	500	800	1100	mV
Black level correction 3	V_{BLC3}	Input: About 20 IRE the diff.of G-out when pin 30 is open & 9 V	100	300	500	mV
Contrast variation with sharpness	ΔV_{CS}	Y-out output level difference when sharpness = max. to min.	−300	0	+300	mV
Brightness variation with sharpness	ΔV_{BS}	Pedestal DC level difference when sharpness = max. to min.	−250	0	+250	mV

■ Electrical Characteristics at T_a = 25°C (continued)

• Reference data for design (continued)

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video signal processing (continued)		Input: 0.6 V_{PP} (V_{WB} = 0.42 V_{0P} stair-step) at G-out				
Y input dynamic range	V_{Imax}	Contrast DAC 03 = 40 Measure at video input Pin31	1.0	1.7	—	V_{PP}
Y S/N ratio	SN_Y	Contrast DAC 03 = 7 F	51	56	—	dB
Black level expansion start point	V_{BLS}	Start point when V_{36} = 4.5 V	37	42	47	IRE
Trap on/off gain difference	ΔG_{TRAP}	Trap on/off ratio	−1	0	+1	dB
Trap on/off delay time variation	Δt_{TRAP}	Trap on/off	480	530	580	ns
Trap frequency tolerance	Δf_{TRAP}	When chroma input is 4.43 MHz, trap centre frequency from 4.43 M	−70	0	+70	kHz
Trap attenuation 4.43 MHz	ATT_{TRAPP}	When chroma input is 4.43 MHz, 4.43 MHz component attenuation	26	30	—	dB
Trap attenuation 3.58 MHz	ATT_{TRAPN}	When chroma input is 3.58 MHz, 3.58 MHz component attenuation	26	30	—	dB
Trap automatic adjustment range	f_{TRAP}	VCO frequency of $\Delta f_{TRAP} \leq$ 70 kHz	3	—	5	MHz
Trap set frequency	f_{ST}	DAC 0 E–D6 = 1 Trap's frequency	4.7	5.5	6.3	MHz
Video signal output V_{CC} variation	$\Delta V_Y/V$	V_{CC1} = 9 V (± 10%)	0	100	200	mV/V
Video signal output temperature variation	$\Delta V_Y/T$	T_a = −20°C to +70°C	0	5	10	%
PAL/NTSC delay time difference	$\Delta t_{P/N}$	Trap on(NTSC-PAL)	−10	10	30	ns
Color signal processing		All tests on: Burst 300 mV_{PP}(PAL)standard is B-out				
Demodulation output residue carrier	V_{CAR1}	Pin 48, pin 49 output's 2nd harmonics	0	—	30	mV
Color difference output residue carrier	V_{CAR2}	Pin 15, pin 16, pin 17 output's 2nd harmonics	0	—	50	mV
VCO free run frequency (PAL)	f_{CP}	Compare with standard f = 4.433619 MHz	−300	0	+300	Hz
VCO free run frequency (NTSC)	f_{CN}	Compare with standard f = 3.579545 MHz	−300	0	+300	Hz
VCO V_{CC} variation	$\frac{\Delta f_C}{V_{CC}}$	V_{CC1} = 9 V (± 10%) V_{CC3} = 5 V (± 10%)	−300	0	+300	Hz
Phase hold characteristic (PAL)	$\Delta\theta_P$	Tint change when Δf_C = −300 Hz to +300 Hz	0	2	5	$\frac{deg}{100\ Hz}$

■ Electrical Characteristics at T_a = 25°C (continued)

• Reference data for design (continued)

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing (continued)		All tests on: Burst 300 mV_{PP}(PAL)standard is B-out				
Phase hold characteristic (NTSC)	$\Delta\theta_N$	Tint change when Δf_C = −300 Hz to +300 Hz	0	2	5	$\frac{deg}{100\ Hz}$
Color difference output PAL/NTSC ratio	$R_{P/N}$	R out PAL/R out NTSC	0.8	1.0	1.2	Times
Line crawling	ΔV_{PAL}	Pin49: −(R−Y)out every 1 H output difference in voltage	0	—	50	mV
Color difference output frequency characteristics	f_{CC}	Bandwidth when gain reduces by 3 dB	—	1.0	—	MHz
Chroma BPF characteristics (PAL)	BPF_P	f = 4.43 MHz −2.00 MHz output level difference	—	32	—	dB
Chroma BPF characteristics (NTSC)	BPF_N	f = 3.58 MHz to2.00 MHz output level difference	—	22	—	dB
Color difference output V_{CC} variation	$\Delta V_C/V$	V_{CC1} = 9 V (± 10%) V_{CC3} = 5 V (± 10%)	—	± 10	± 15	%
Color difference output Temperature variation	$\Delta V_C/T$	Temperature: −20°C to +70°C	—	± 10	± 15	%
Color variation to brightness variation	V_{BC}	When color: max.to min. the difference in pedestal DC	− 250	0	+ 250	mV
Color to brightness variation voltage	ΔV_{BC}	RGB output variation voltage difference	0	—	20	mV
RGB processing						
(C−Y)/Y ratio	$R_{C/Y}$	Input: Color bar. B-out, contrast: typ. Color: DAC 00 = 60	0.9	1.2	1.5	$\frac{V_{OP}}{V_{PP}}$
C−Y,Y delay difference	$\Delta t_{C/Y}$	Input: Color bar, B-out Green = magenta delay	−100	0	+100	ns
Y_S switching speed	f_{YS}	External input 3 V output level when at −3 dB frequency	7	11	—	MHz
Exeternal RGB input dynamic range	V_{DEXT}	DAC 03 = 7 F(Contrast : max.)	2.0	2.5	3.2	V_{OP}
Internal/External RGB crosstalk	CT_{RGB}	f = 1 MHz 1 V_{PP} The crosstalk level when Y_S = 5 V	—	−60	−50	dB
Spot killer operation	V_{SPK}	Voltage at pin 9 from V_9 = 9 V reduces until spot killer is on	7.4	7.8	8.2	V
Contrast variation to brightness variation	V_{BAC}	When contrast is max.to min., the diff. in pedestal DC	−250	0	+250	mV

■ Electrical Characteristics at T_a = 25°C (continued)

• Reference data for design (continued)

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RGB processing (continued)						
Contrast to brightness variation voltage	ΔV_{BAC}	RGB output variation voltage difference	0	—	20	mV
RGB output color/BW DC difference voltage	ΔV_{CBW}	Difference in pedestal voltage between burst on/off	− 60	0	+ 60	mV
Pedestal level V_{CC} variation	$\Delta V_{PL}/V$	Pedestal level change when V_{CC1} = 9 V (± 10%)	0	200	400	mV/V
Pedestal level temperature variation	$\Delta V_{PL}/T$	Pedestal level change when temperature is −20°C ~ +70°C	−2.6	−2.2	−1.8	mV/°C
Pedestal level 2	V_{PD2}	The pedestal level when G cutoff DAC 05 = 18	2.1	2.7	3.3	V
Synchoronizing signal processing						
Lock detector output voltage	V_{LD}	Pin18 DC voltage when horizonal AFC is locked	5.7	6.3	6.9	V
Lock detector charging current	I_{LD}	DC measurement	± 0.6	± 0.8	±1.1	mA
FBP input slice level (RGB)	V_{FBP}	Minimum voltage at which blacking of RGB outputs happens	0.40	0.75	1.10	V
FBP input slice level (AFC2)	V_{FBPH}	Minimum voltage at which AFC 2 operates	1.5	1.9	2.3	V
Horizontal AFC μ	μ_H	Calculate from AFC current DC measurement	30	37	44	μA/μs
Horizontal VCO-β curve	β_H	Slope of β curve near to f = 15.7 kHz	1.4	1.9	2.4	Hz/mV
Burst gate pulse position NTSC,PAL	P_{BGP}	When hor. AFC is on, hor. sync. rising edge to the BGP rising edge	0.2	0.4	0.6	μs
Burst gate pulse width (PAL)	W_{BGPP}	When hor. AFC is on, BGP's pulse width	3.4	4.0	4.6	μs
Burst gate pulse width (NTSC)	W_{BGPN}	When hor. AFC is on, BGP's pulse width	2.5	3.0	3.5	μs
Burst gate pulse output voltage	V_{BGP}	Pin50 DC voltage during BGP period	4.5	4.7	4.9	V
Horizontal blanking pulse output voltage	V_{HBLK}	Pin50 DC voltage during H-blanking period	2.1	2.4	2.7	V
Vertical blanking pulse output voltage	V_{VBLK}	Pin50 DC voltage during V-blanking period	2.1	2.4	2.7	V
Vertical blanking pulse width (PAL)	W_{VP}	Pulse width when f_H = 15.625 kHz	1.31	1.41	1.51	ms
Vertical blanking pulse width (NTSC)	W_{VN}	Pulse width when f_H = 15.73 kHz	1.01	1.11	1.21	ms
FBP allowable range	T_{FBP}	delay from hor. output rising edge to FBP centre	12	—	19	μs

■ Electrical Characteristics at T_a = 25°C (continued)

• Reference data for design (continued)

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C interface						
Bus free before start	t_{BUF}	—	4.0	—	—	µs
Start condition set-up time	$t_{SU,STA}$	—	4.0	—	—	µs
Start condition hold time	$t_{HD,STA}$	—	4.0	—	—	µs
"L" period SCL, SDA	t_{LOW}	—	4.0	—	—	µs
"H" period SCL	t_{HIGH}	—	4.0	—	—	µs
Rise time SCL,SDA	t_r	—	—	—	1.0	µs
Fall time SCL,SDA	t_f	—	—	—	0.35	µs
Data set-up time (Write)	$t_{SU,DAT}$	—	0.25	—	—	µs
Data hold time (Write)	$t_{HD,DAT}$	—	0	—	—	µs
Acknowledge set-up time	$t_{SU,ACK}$	—	—	—	3.5	µs
Acknowledge hold time	$t_{HD,ACK}$	—	0	—	—	µs
Stop condition set-up time	$t_{SU,STO}$	—	4.0	—	—	µs
DAC						
4,6,7-bit DAC DNLE	$L_{4,6,7}$	1 LSB = {Data(max.)–Data(00)}/15(4-bit), 63(6-bit), 127(7-bit)	0.1	1.0	1.9	$\frac{LSB}{Step}$
8-bit DAC DNLE	L_8	1 LSB = {Data(FF)–Data(00)}/255(8-bit)	0.1	1.0	1.9	$\frac{LSB}{Step}$
Cut off DAC overlap	ΔStep	The overlap between the two 8-bit sections of R,B cutoff & AFT	27	32	37	Step

■ Electrical Characteristics at T_a = 25 °C (continued)

• Description of test circuits and test methods

1.Input signal

(1) Video : 10 stairs waveform 0.6 V_{PP}(V_{BW} = 0.42 V_{OP})

(2) Chroma : Color bar signal : Burst level 300 mV_{PP}

Rainbow signal : Burst level 300 mV_{PP}

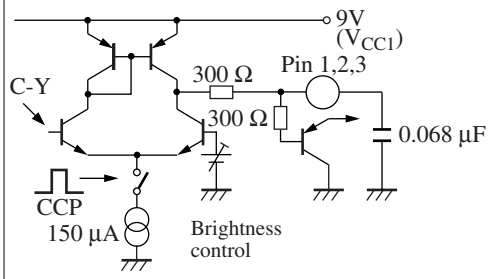
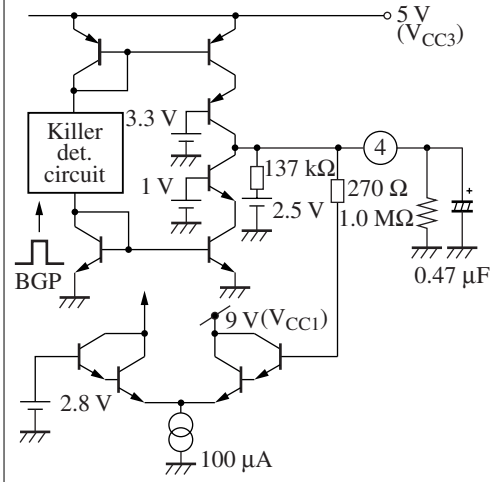
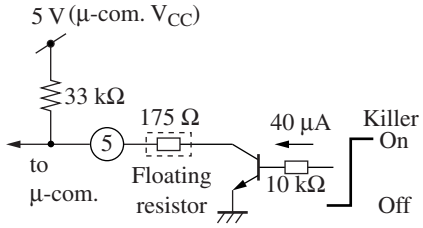
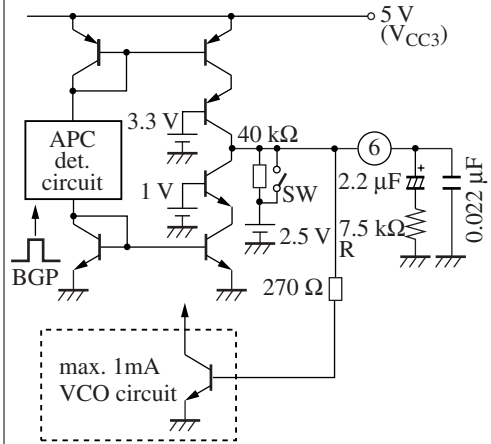
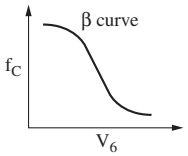
(3) Synchronous : Horizontal, vertical synchronous signal input are 1.5 V_{PP} to 2.5 V_{PP}

2.I^2C bus condition : (PAL)

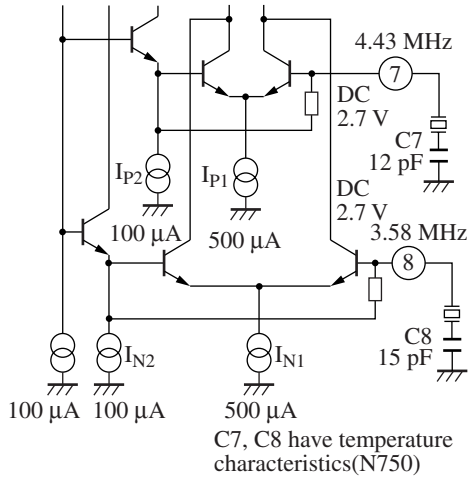
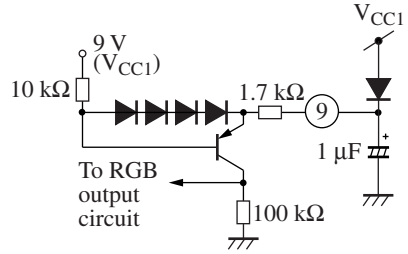
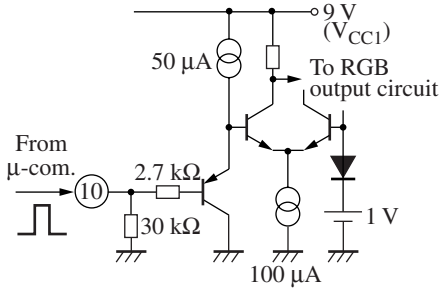
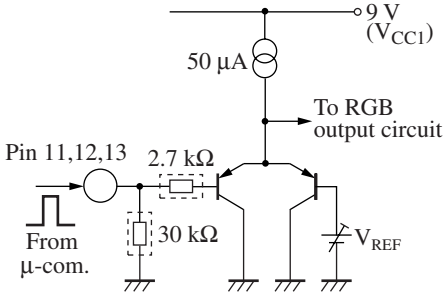
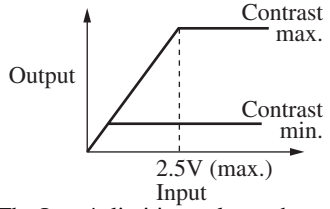
Sub address	Data(H)
00	40
01	40
02	80
03	40
04	80
05	00
06	00
07	00
08	80
09	80
0A	88
0B	01
0C	40
0D	40
0E	01

Control	Data(H)
Color	00 = 40
Tint	01 = 40
Brightness	02 = 80
Contrast	03 = 40
Sharpness	04 = 00
Cutoff R,B	05, 07 = 00
Cutoff G	06 = 00
Driver R,B	08, 09 = 80
Video output	0A(upper byte) = 8*
Hor.centre	0A(lower byte) = *8
External DAC 2	0B = 01 (04–D7=1)
External DAC 1	0C = 40
External DAC 3	0D = 40

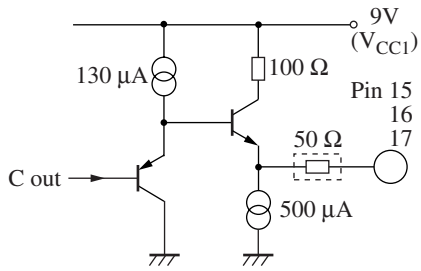
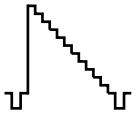
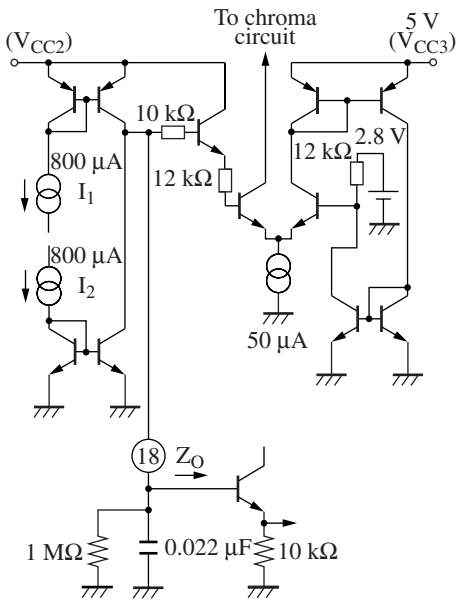
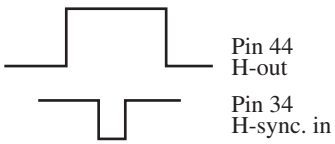
■ Pin Equivalent Circuit

Pin No.	Equivalent circuit	Function	Status
1 2 3		Pin1 : Color Difference Clamp Pin(R−Y) Pin2 : Color Difference Clamp Pin(G−Y) Pin3 : Color Difference Clamp Pin(B−Y) • Input from Pin51, 52, the color difference signals are clamped according to brightness control voltage • The clamp pulse uses internal clamp pulse	DC about 7 V
4		Killer Filter Pin : • Killer detection circuit's filter pin (operate during BGP period) • Below 2.8 V, killer is on(no color output)	DC about 3.3 V
5		Killer Output Pin : • Killer detection circuits output pin • Pin5 pull-up resistor, 33 kΩ, is connected to MICOM's V_{CC}.	DC Killer on 0.2 V Killer off 5 V
6		APC Filter Pin : • APC detector circuit's filter pin (operate during BGP period) • As external resistor, R, becomes larger, detection sensitivity becomes larger (pull in becomes easier. Interference by noise becomes easier)  • During SECAM mode, the 40 kΩ is shorted to stop APC circuit's operation	DC about 2.5 V

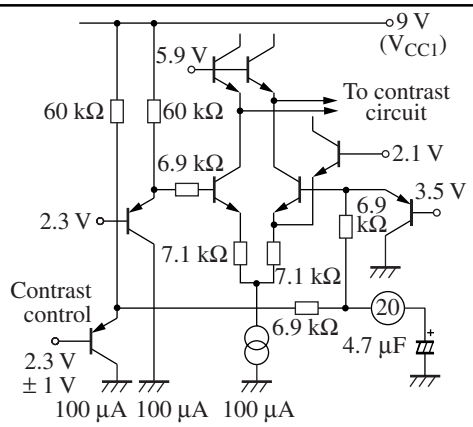
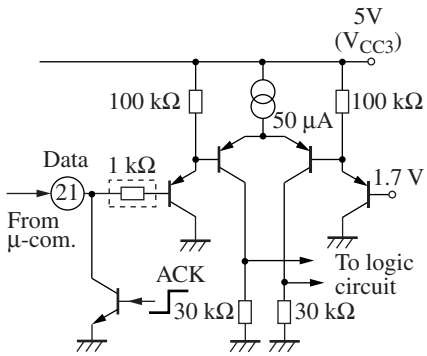
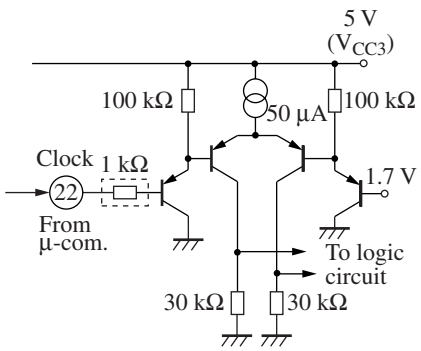
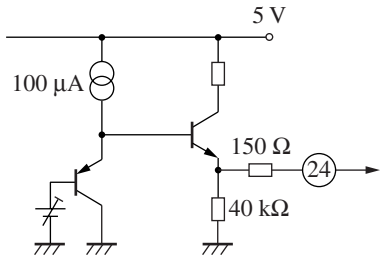
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
7 8		Pin7 : Chroma Oscillator Pin(4.43 MHz) Pin8 : Chroma Osicillator Pin(3.58 MHz) • At chroma oscillator pin, either 4.43 MHz or 3.58 MHz oscillation takes place • Oscillation frequency switching is done by I²C bus, 0E-D0 bit • When 0E-D0 =1, IP1, IP2 is on. 3.58 MHz is oscillating • The PCB layout pattern between the pin and the resonator must be as short as possible	AC $f = f_C$ about 0.3 V_{PP}
9		Spot Killer Pin : • When the set is power off, it is used for discharging the electric charge from CRT quicky • When V_{CC1} reduces, RGB output pin's DC voltage rise	DC about 9 V
10		Y_S Input Pin : • The fast blanking pulse input pin is for the OSD • Above 1 V_{OP} is on	AC (Pulse) 
11 12 13		Pin11 : External R Input Pin Pin12 : External G Input Pin Pin13 : External B Input Pin • The external input pins are for the OSD • The output level changes linearly with the input level  • The Input's limiting voltage changes according to the contrast control level	AC (Pulse) 

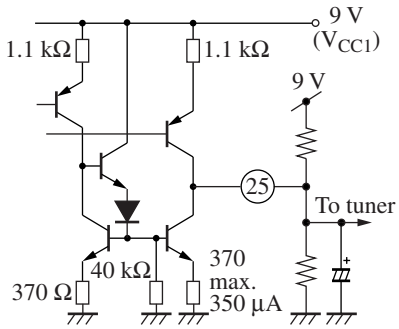
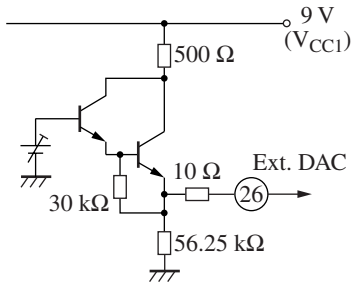
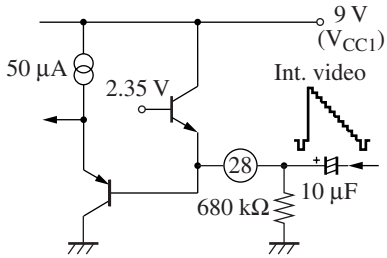
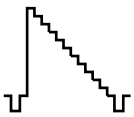
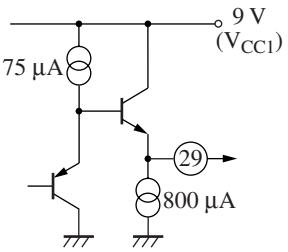
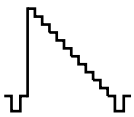
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
14	—	V_{CC1} (typ. 9 V) : • IF circuit • Video circuit • RGB circuit	DC 9V
15 16 17		Pin15 : R out Pin Pin16 : G out Pin Pin17 : B out Pin • BLK level about 0.9 V • Black(pedestal)level about 2.2 V • If Pin30(Black level detection output pin)is 0 V, blanking is removed.	AC 
18		Horizontal Synchronous Detection Output Pin : • The phase between horizontal synchronous signal and horizontal output pulse is detected • When synchronising comes off, Pin18 voltage goes low • When not synchronising,color control is minimum,and chroma output disappears • In the case where Pin18 voltage is used by MICOM, impedance has to be taken care(Zo ≥ 1 MΩ is required)  • H sync. period, Pin44 level is "H" : I_1 on "L" : I_2 on	DC When synchronising about V_{CC2}-V_{SAT} When synchronising comes off about 0.3 V
19	—	GND : • RGB circuit • DAC I^2C circuit • IF circuit	—

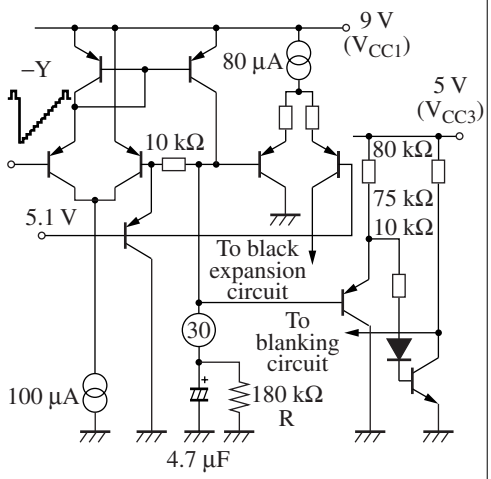
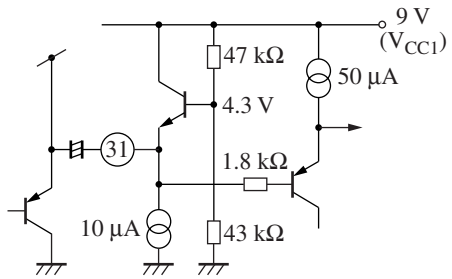
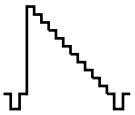
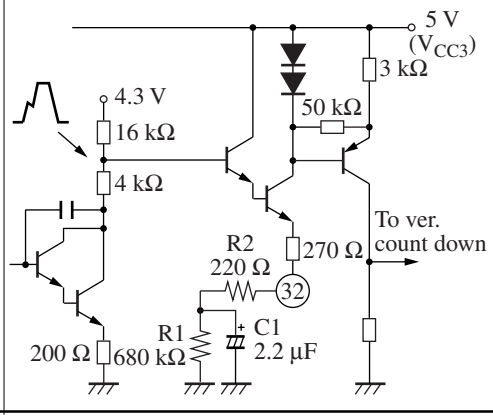
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
20		ACL Pin : • When Pin20 DC voltage is externally decreased, contrast is limited	DC about 3 V
21		I^2C BUS DATA Input Pin :	AC (Pulse)
22		I^2C BUS CLOCK Input Pin :	AC (Pulse)
23	—	GND : • External DAC circuit	—
24		External DAC 1 Pin : • External DAC 1 voltage is adjustable by using I^2C bus	DC

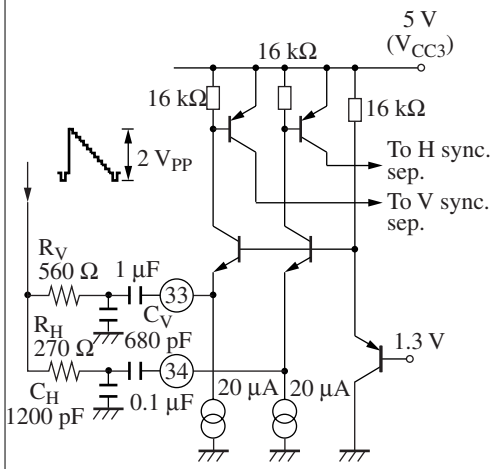
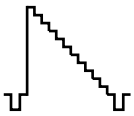
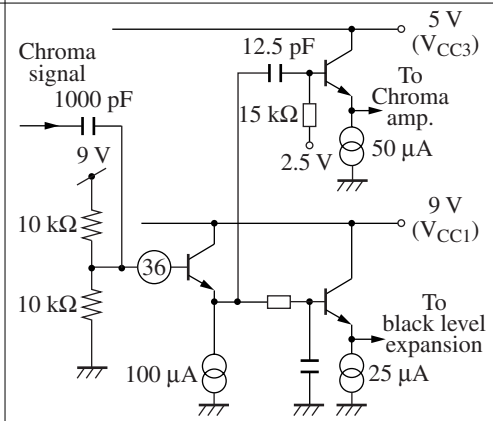
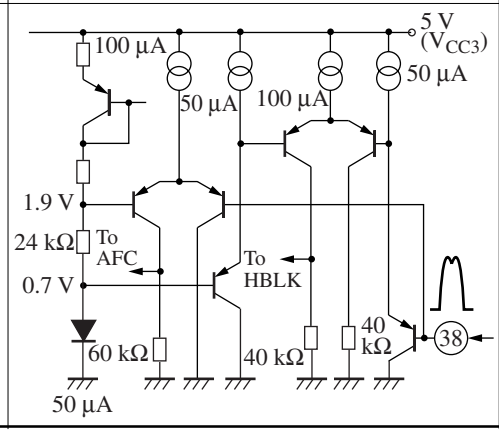
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
25		External DAC 2 Pin : • External DAC 2 voltage is adjustable by using I^2C bus through the change in DAC output current	DC
26		External DAC 3 Pin : • External DAC 3 voltage is adjustable by using I^2C bus	DC
27	—	N.C. Pin	—
28		Video Input Pin : • From VIF IC, the detected signal's (internal video signal)input pin • Input by DC cut • Standard input 1 V_{PP}(max.1.5 V_{PP})	AC 1 V_{PP} (composite)  DC level about 1.6 V
29		Video Output Pin : • Adjustable to 2 V_{PP} by I^2C bus (use 0A upper 4-bit)	AC 1.75 V_{PP} 

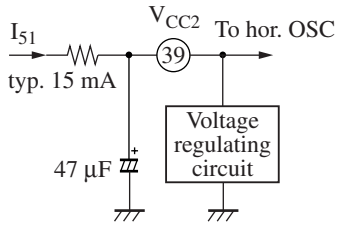
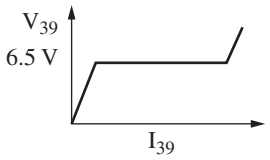
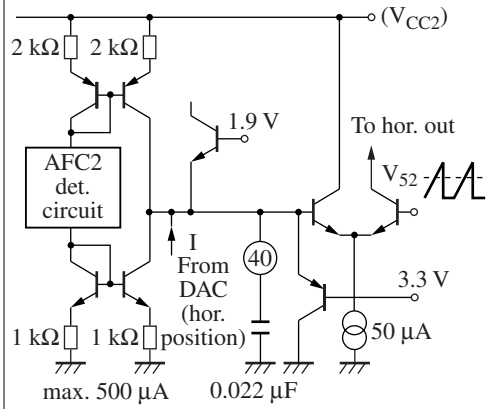
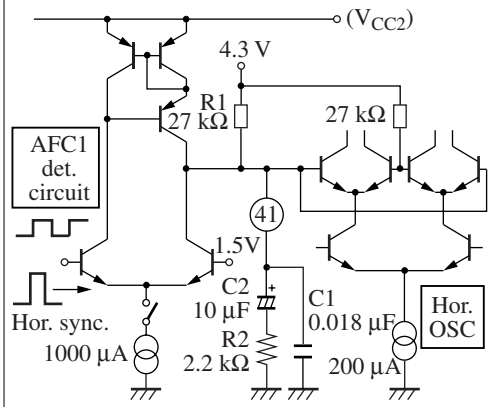
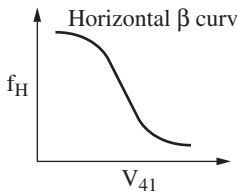
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
30		Black level detecion output pin blanking off switch pin : • For black expansion circuit's black level detection output filter pin • For removing the blanking period and holding the darkest Y level • By changing the external resistor, R, the black level expansion sensitivity can be changed. When R is bigger, area of response is smaller • To stop black expansion circuit, set Pin30 voltage to about V_{CC}(9 V) • If Pin30 voltage is GND, blanking is off.(Black expansion is also off)	DC abuot 5.1 V
31		Video Input Pin : • Video signal input pin (Composite video also allowable) • Standard input 0.6 V_{PP} • Sync. top is clamped to 3.5 V • Video signal is inputed to low impedance inputs	AC 0.6 V_{PP} 
32		Vertical Synchronous Signal Clamp Pin : • This is the peak clamp pin for vertical synchronous signal separation • The integration of the vertical synchronous signal is determined by the internal time constant, but the external time constant, R1, C1, is chosen according to the required trigger timing • Using R1 > 200 kΩ • R2 is the resistor which is used to control the emitter current	AC f = fV 

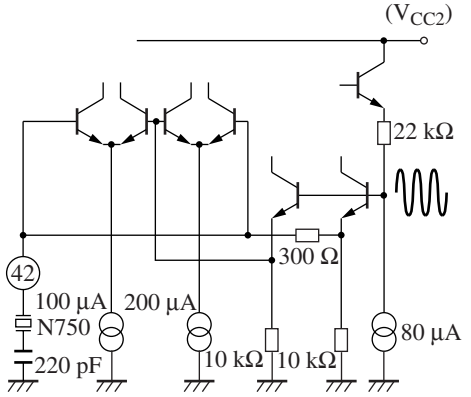
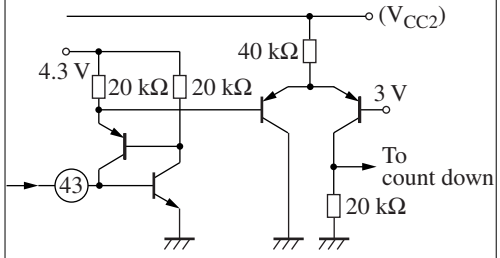
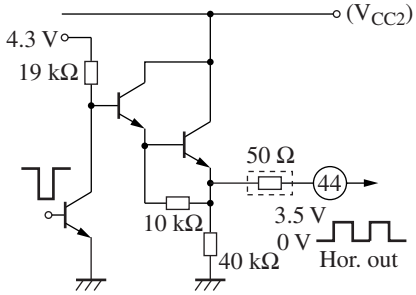
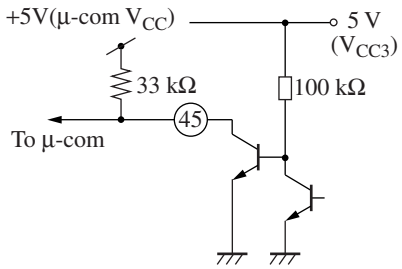
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
33 34		Pin33 : Vertical Sync. Separation Input Pin Pin34 : Horizontal Sync. Separation Input Pin • Pin33, 34 internal circuits are similar • Usually, vertical synchronous threshold is deeper than horizontal synchronous' threshold. Thus $R_V > R_H$ • R_H and C_H determine cutoff frequency at about 500 kHz • R → big, threshold becomes deeper (Sync. compression is weaker). R → small, threshold becomes shallower (fluctuation becomes weaker due to vertical sag) Sync. top is clamped at 1.3 V	AC 2 V_{PP} 
35	—	V_{CC3} (typ.5V) : • For chroma and jungle circuit	DC 5 V
36		Chroma Signal Input Pin Black Expansion Starting Point Adjustment Pin : • Pin36 is chroma signal input pin and external DC voltage is applied to adjust the starting point of black expansion	AC + DC Burst typ. 300 mV_{PP} DC typ. 4.5 V
37	—	GND : • For video,chroma and jungle circuit	DC 0 V
38		FBP Input Pin : • The FBP input pin is for horizontal blanking and AFC circuit • Threshold level for HBLK : 0.7 V AFC : 1.9 V • External DC 1.3 V must be applied to become all blanking • Input voltage below 0 V is prohibited	AC FBP 

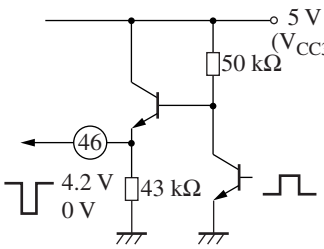
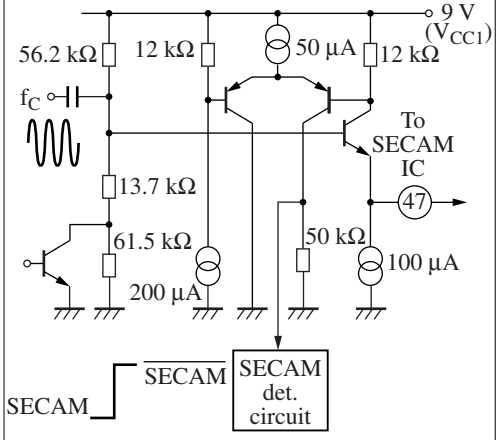
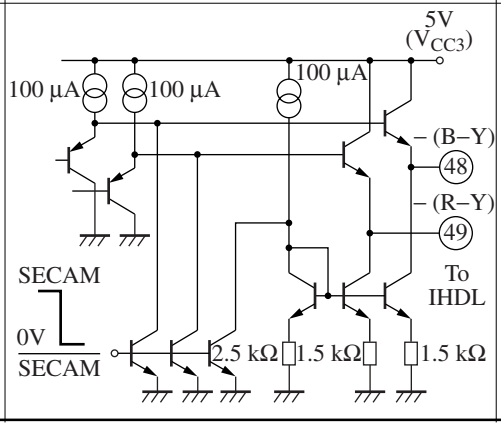
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
39		Horizontal Steady State Supply Pin : • Steady state supply is used by horizontal circuit startup. Internal voltage regulating circuit is present 	DC 6.5 V
40		Horizontal AFC 2 Filter Pin : • FBP and IC internal pulse phase difference is compared. At Pin40, a capacitor is connected for charging and discharging this current • The current from the picture centre position adjustment DAC establishes DC by chaging and discharging current • Time difference from Hout to FBP-in depends on V_{40} which changes the slice level of internal sawtooth waveform	DC 1.5 V to 3.5 V
41		Horizontal AFC 1 Filter Pin : • Horizontal synchrous signal and IC internal pulse phase difference is compared. At Pin41, a capacitor is connected for charging and discharging current • R1, R2, C1, C2, are lag-lead filter used by AFC 1 	DC typ. 4.3 V

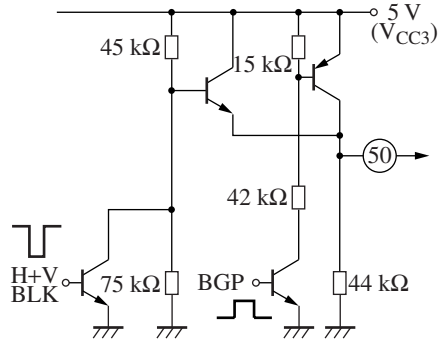
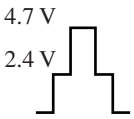
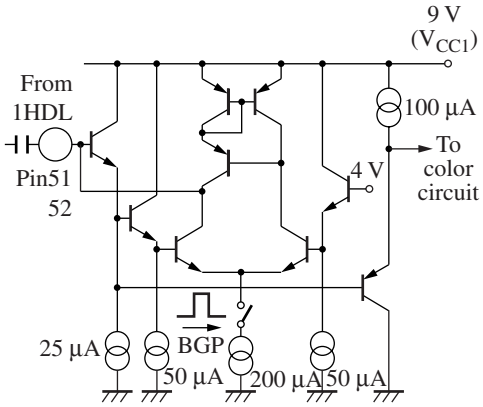
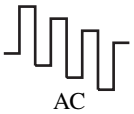
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
42		Horizontal Oscillator Pin : • Oscillates by 32 × f_H = 500 kHz ceramic resonator • Horizontal and vertical pulses are made by the IC internal count down circuit	AC f = 32 f_H (about 500 kHz)
43		Over Voltage Protection Input Pin : • Input pin is used by X-ray protector circuit for over voltage • By internal logic circuit, when H out pulse is low, shut down starts (Prevent damaging the horizontal drive transistor)	DC usually 0 V
44		Horizontal Pulse Output Pin : • Duty is about 37 %	AC (Pulse) 
45		Vertical Frequency Detection Output Pin : • The output of the result of the internal counter of the vertical synchronous signal period • f_V = 60 Hz : V45 is "H" = 50 Hz : V45 is "L"	DC 0 V or 5 V

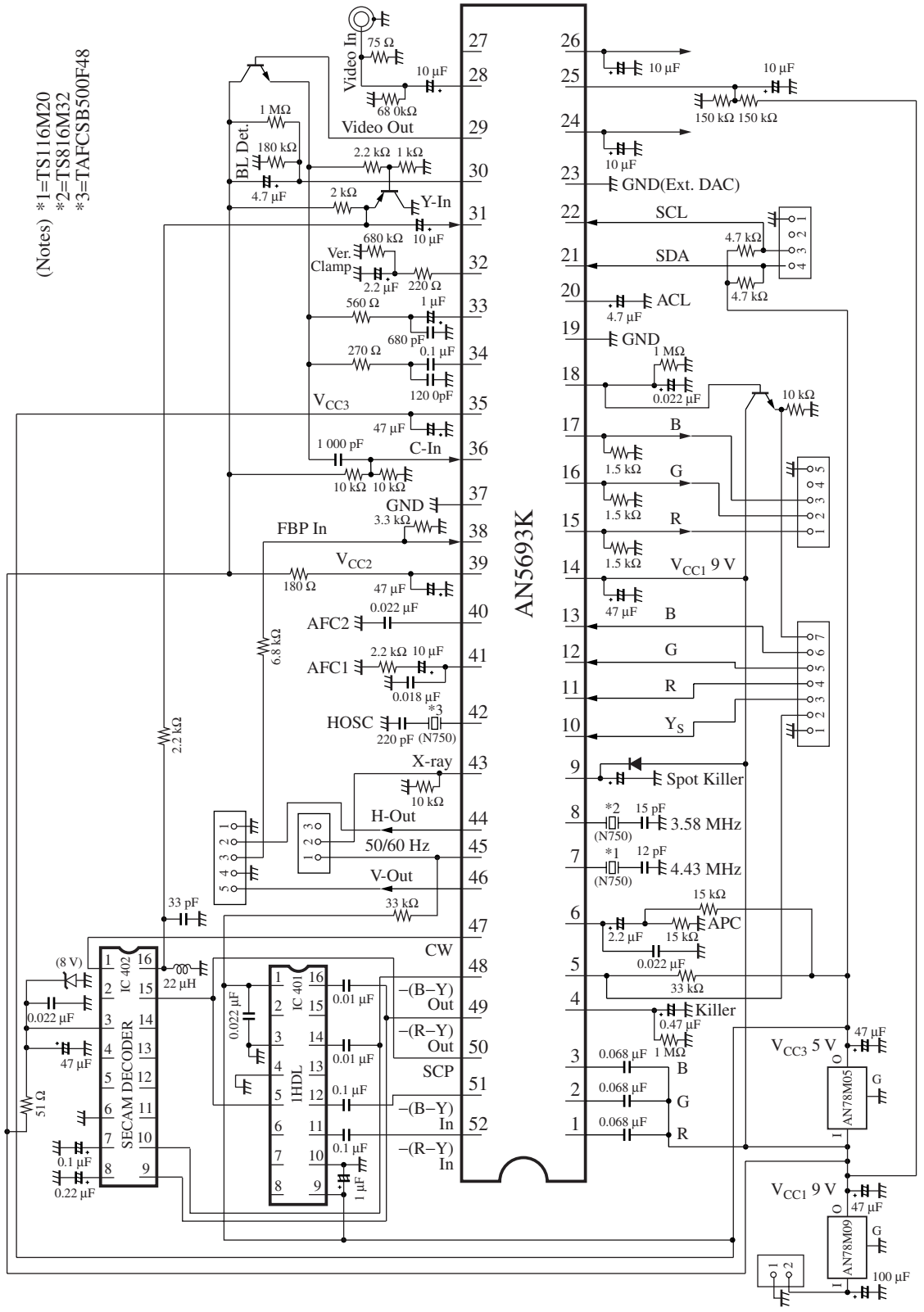
■ Pin Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Function	Status
46		Vertical Pulse Output Pin : • Nagative polarity pulse width is 10H	AC (Pulse) 
47		SECAM Interface Pin : • The input and output pin for the interfacing with the SECAM IC • When above 100 µA current is drawn from Pin47, system becomes SECAM mode • When in non-SECAM, DC 4.6 V + AC 300 mV_{PP} • When in non-SECAM, DC 1.3 V + AC 300 mV_{PP} : 4.43 MHz or 0 mV_{PP} : 3.58 MHz	AD + DC AC 300 mV_{PP} or 0 mV_{PP} DC 4.6 V or 1.3 V
48 49		Pin48 : –(B–Y)Output Pin Pin49 : –(R–Y)Output Pin • when in SECAM, output circuit is off and output impedance is high impedance • The outputs to 1 HDL	AC –(B–Y)  AC –(R–Y)  DC level about 2.5 V

■ Pin Equivalent Circuit (continued)

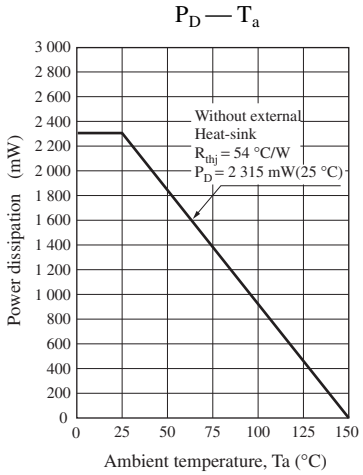
Pin No.	Equivalent circuit	Function	Status
50		Sandcastle Pulse Output Pin : • Sandcastle pulse is outputed to1 HDL and SECAM IC	AC (Pulse) 
51 52		Pin51 : –(B–Y)Input Pin Pin52 : –(R–Y)Input Pin • From 1 HDL, color difference signal outputs are inputed to these pins • These pins are clamped at 4.7 V pedestal level from the clamp circuit • The input levels at Pin51, 20 are about 2 times the output amplitude of Pin48, 49 respectively	AC –(B–Y)  AC –(R–Y)  DC level 4.7 V

■ Application Circuit Example



■ Technical Information

• Package Allowable Loss



• Outline of major blocks

• Video

(1) Y delay line built-in : total delay time is approximately 690 ns.

(2) Sharpness control is by using delay line aperture control. (contour emphasis type)
Together with black level extention circuit, high quality picture is achieved.

(3) Chroma trap is built-in : Trap frequency is synchronised with the chroma VCO frequency at 4.43 MHz/3.58 MHz automatically. By I^2C bus, the trap can be forced to by-pass. In SECAM mode, about 4.43 MHz free run frequency is obtained. When in black & white(B/W)mode(killer"On"), the trap is automatically by-passed.

(4) Pedestal clamp filter is built-in.

(5) Service switch : (Y contrast min., Vertical output stop). Can be switched by I^2C bus.

(6) Chart showing the modes of the trap :

System(f_C)	Color or B/W	Trap Status
4.43 MHz(PAL)	Color	4.43 MHz
	B/W	4.43 MHz free-run
3.58 MHz(NTSC)	Color	3.58 MHz
	B/W	3.58 MHz free-run
SECAM	Color	4.43 MHz free-run
	B/W	4.43 MHz free-run
Forced manual mode by I^2C bus	—	About 5.5 MHz
Forced through mode by I^2C bus	—	No trap point

• Chroma

(1) Using base-band 1H delay line(external 1HDL IC required), adjustment free is achieved.

(2) BPF(4.43 MHz/3.58 MHz), ACC filters are built-in, thus external components are reduced.

(3) By changing the following mode using the I^2C bus :

1. PAL/NTSC
2. 4.43 MHz/3.58 MHz
3. Forced PN/Forced SECAM

and together with the SECAM IC for automatic SECAM detection, multi-system application is possible.

■ Technical Information (continued)

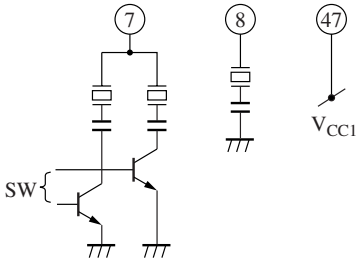
- Outline of major blocks (continued)
  - Chroma (continued)

(4) Killer output pin is available for system identification by MICOM.
(Killer"On" → 0 V : Either color signal is not properly detected due to wrong system settig, or the color signal field strength is too weak.
Killer"Off" → 5 V : Color signal is properly detected.)
When killer is on, according to the MICOM control sequence,the mode and VCO frequency will be switched by means of the I^2C bus.

(5) During SECAM, the color difference output pins are put into high impedance.

(6) AN5344(color-compensation IC)and other types of feature IC can be connected because color difference input pins are available.

(7) It is possible for South American set application.
(three-normal system : NTSC M,PAL M,PAL N).

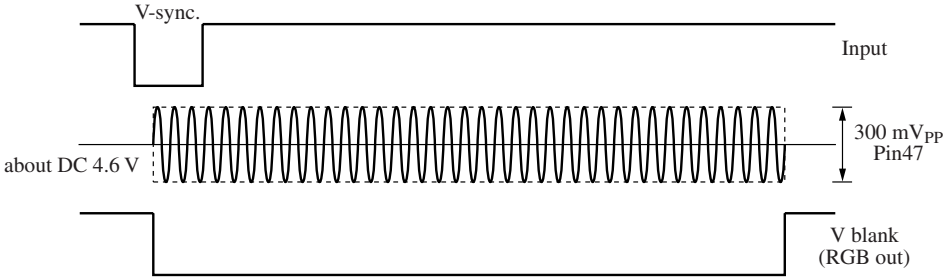


Note) For PAL M, crystal MEIDEN 3575 & C = 18 pF are used.
For PAL N, crystal MEIDEN 3012-M & C = 22 pF are used.
In order to extend downwards the β curve, a capacitor of 2 pF to 4 pF is added between Pin7 and GND.

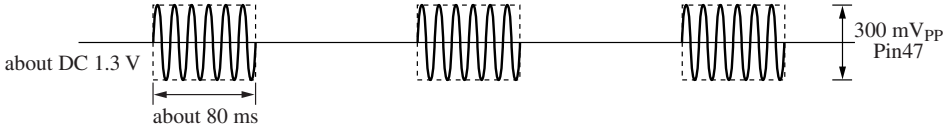
(8) PAL/NTSC, SECAM interface(Pin 47)

Input Signal	DC	f_C	AC Level
4.43 MHz	about 1.3 V	4.43 MHz	300 mV_{PP}
3.58 MHz	about 1.3 V	X	X
SECAM *1	about 4.6 V	4.43MHz	300 mV_{PP}
B/W *2	about 1.3 V	—	300 mV_{PP}

Note) *1 : 4.43 MHz AC component is output during vertical retrace period, is as shown below.



Note) *2 : Eventhough the MICOM switches the VCO between 4.43MHz and 3.58MHz, only the 4.43 MHz CW will be outputed at periodic intervals as shown below.



■ Technical Information (continued)

• Outline of major blocks (continued)

• RGB

(1) OSD is made up of 3 colors of RGB, by using simple analog input, of which input at 0 V is fixed at the pedestal level.(The input dynamic range is controllable by contrast)

(2) White balance(drive, cutoff)adjustment is implemented by I^2C bus.

(3) Spot killer is built-in : When power supply is off, R, G, B, output levels increase, the residue spot that is visible on the CRT is eliminated.

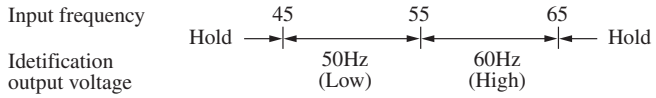
• Jungle

(1) 2-pin are used for synchronous inputs(Horizontal, Vertical)to improve the synchronisation characteristics of horizontal and vertical synchronisation.

(2) The horizontal circuit is based on countdown method using a 32 f_H ceramic oscillator.
AFC circuit is employing the doubler method.

(3) The vertical circuit is employing the trigger method's countdown circuit, thereby resulting in no adjustment and stable vertical synchronisation. The pulse output will not be interfered by interlace which is caused by pattern layout.

(4) Vertical frequency identification circuit is built-in : the output of 50/60 Hz identification is determined according to the vertical synchronous frequency.(60 Hz → "H")
Below 45 Hz and above 65 Hz, the previous state is hold. After 3 consecutive vertical period, if 60 or 50 Hz is identifield, the initial output will be changed.



(5) Horizontal lock detection circuit and X-ray protection circuit(Shut down method)are built-in.

(6) Picture centre position is adjustable by I^2C bus.(±1.6 µs)

(7) In the case of blue back in a weak field, the vertical trigger can be in off mode(I^2C bus).
Thus a stable picture is maintained.

• I^2C Bus

(1) There are 15 built-in DAC controls and 13 built-in switches to reduce adjustment for set maker.

(2) Auto-increment function present :

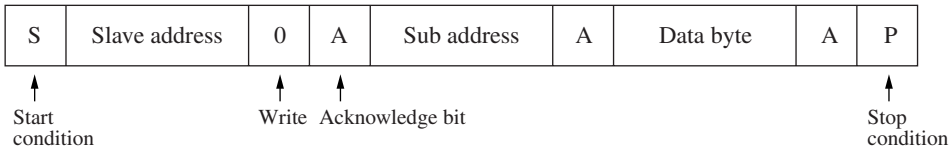
• Sub address 0*: Auto-increment mode
(When the data is sent in consecutive order, the sub-address will be changed in consecutive order, as data is inputed)

• Sub address 8*: Data refresh mode
(When the data is sent consecutively, it is sent to the same sub-address)

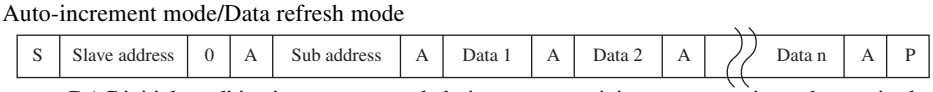
(3) I^2C Bus Protocol

• Slave address : 10001010(8AH)

• Format(Usual)



• Auto-increment mode/Data refresh mode



(4) Because DAC initial condition is not guaranteed, during power on, it is necessary to input the required standard data.

■ Technical Information (continued)

- Outline of major blocks (continued)
  - I^2C Bus Addressing

Sub Address	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00 (40H)	P/N (0→P)	←			Color			→
01 (40H)	PN/S (0→PN)	←			Tint			→
02 (80H)	←				Brightness			→
03 (40H)	SSW (0→Off)	←			Contrast			→
04 (A0H)	Ext. DAC2 (1→typ.)		←		Sharpness			→
05 (80H)	←				Cutoff R			→
06 (40H)	←				Cutoff G			→
07 (80H)	←				Cutoff B			→
08 (80H)	←				Drive R			→
09 (80H)	←				Drive B			→
0A (88H)	←		Video adjust	→	←		H center	→
0B (01H)	←				External DAC2			→
0C (40H)	SECAM Enable (0 → enable)	←			External DAC1			→
0D (40H)		←			External DAC3			→
0E (01H)	Ver. trig stop (0 → normal)	Auto trap (0 → auto)	Cut off B (0 → typ.)	Cut off R (0 → typ.)	Ver. OSC (0 → 50)	Ver. Auto trap (0 → auto)	Chroma trap (0 → normal)	Chroma VCO (1 → 4.43)

Note) Items in the brackets are initial conditions.

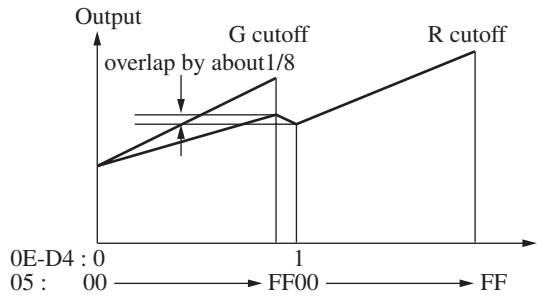
■ Technical Information (continued)

• Outline of major blocks (continued)

• I^2C Bus Control Contents

1. For the Control information, for all sub-address, when data goes up, output increases.
   (Example : Contrast 00 → contrast min., 7F → contrast max., Brightness 00 → pedestal low, FF → pedestal high)
2. Other control supplementary
   (1) 00 : Color
   When Color data is 00, chroma output is completely cutoff so that color is off.
   (2) 01 : Tint
   When tint data is 00, the skin color approaches red.When tint data is 7F, the skin color approaches green.
   (3) 05, 06, 07(8-bit)and 0ED4, 0ED5(1-bit) : cutoff R, G, B
   The cutoff controllable range has increased resolution with 1 extra bit and is segmented into 2 sub-section, each section is variable by 8-bit DAC.
   (Cutoff G is 1 section of 8-bit DAC, that has the same variable range as R, B)

   Example : Case of R cutoff



   (4) 08, 09 : Drive R, B
   8-bit DAC 1 section(no switching of sub-section).
   (5) 0A : Video Adjust
   Data 0*→ composite video min. F*→ composite video max. This control is used to adjust the composite video level.
   (6) 0A : Horizontal Centre
   Data *0→ picture moves left. *F→ picture moves right.
   (7) 0B : External DAC2 and 04 D7
   External DAC2 has 8-bits DAC of 2 sections adjustment.
   Data 01 → DC voltage shifts down.
   Data FF → DC voltage shifts up.
   (8) 0C : External DAC1
   Data 00 → DC voltage shifts down.
   Data 7F → DC voltage shifts up.
   (9) 0D : External DAC3
   Data 00 → DC voltage shifts down.
   Data 7F → DC voltage shifts up.

■ Technical Information (continued)

• Outline of major blocks (continued)

• Switch Operation

Data Bit	SW Contents	Detail Contents
00-D7	PAL/NTSC mode switch (0 → PAL) (1 → NTSC)	• Choroma signal delay line correction(PAL : short) • BGP width change(PAL : wide) • CW switch to killer(PAL : 90/270 deg) • Tint operation change(PAL : Tint off) • Ident operation change(PAL : Operating)
01-D7	PAL, NTSC/SECAM mode switch (0 → normal detection mode) (1 → forced SECAM mode)	• Demodulator Output mode switch In forced SECAM, color difference pin(48, 49) become high impedence.
03-D7	SSW(Service switch) (0 → normal) (1 → Service mode)	• When in Service mode(1 H line white balance adjust) Vertical output pulse stop(DC about 4.3 V) Y output off, Chroma output present
04-D6	Not used	
04-D7	External DAC2 (0 → no offset) (1 → offset)	• For External DAC2 2 section adjustment
0C-D7	SECAM enable switch (0 → normal) (1 → forced disable SECAM)	• SECAM error detection prevention switch 1 → non-SECAM,SECAM detection input condition (Pin47)will not be received
0D-D7	Not used	
0E-D0	Chroma VCO switch (0 → 3.58 MHz) (1 → 4.43 MHz)	• Chroma oscillator circuit switch (video circuit trap frequency also switch)
0E-D1	Chroma trap switch (0 → Trap present) (1 → Through)	• Video circuit's chroma trap switch (Y signal phase shift when through)
0E-D2	Vertical auto switch (0 → Auto switch) (1 → Manual switch)	• Vertical frequency detection circuit switch Auto switch : Auto detection mode by internal counter Manual switch : Depending on 0E-D3 data to force into 50 or 60 Hz mode.
0E-D3	Vertical oscillator switch (0 → 50 Hz) (1 → 60 Hz)	• Vertical frequency switch Only effective if 0E-D2 data is 1
0E-D4	Cutoff R (0 → no offset) (1 → offset)	• Used to switch the cutoff R between 2 section
0E-D5	Cutoff B (0 → no offset) (1 → offset)	• Used to switch the cutoff B between 2 section

■ Technical Information (continued)

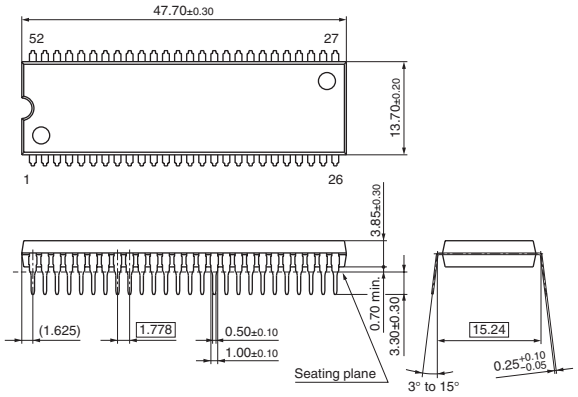
• Outline of major blocks (continued)

• Switch Operation (continued)

Data Bit	SW Contents	Detail Contents
0E-D6	Trap auto switch (0 → Auto switch) (1 → frequency fixed)	• Auto switch : Moves with chroma oscillating frequency. Frequency fixed : fixed at about 5.7 MHz
0E-D7	Vertical trigger stop switch (0 → normal) (1 → trigger off)	• Switch for prevention of vertical trigger input 1 → trigger input off. In blue back etc., vertical dancing due to any noise is prevented.

■ New Package Dimensions (Unit: mm)

• SDIP052-P-0600F (Lead-free package)



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