

**3A DDR TERMINATION REGULATOR****AP2302****General Description**

The AP2302 linear regulator is designed to meet the JEDEC specification SSTL-2 and SSTL-18 for termination of DDR-SDRAM. The regulator can sink or source up to 3A current continuously, offers enough current for most DDR applications. Output voltage is designed to track the reference voltage within a 2% (DDR I) and 3% (DDR II) tolerance for load regulation while preventing shooting through on the output stage. On-chip thermal limiting provides protection against a combination of high current and ambient temperature which would create an excessive junction temperature.

The AP2302, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs.

The AP2302 is available in SOIC-8, TO-252-5L and TO-263-5L packages.

**Features**

- Support Both DDR I ( $1.25V_{TT}$ ) and DDR II ( $0.9V_{TT}$ ) Requirements
- Source and Sink Current up to 3A
- High Accuracy Output Voltage at Full-load
- Adjustable  $V_{OUT}$  by External Resistors
- Shutdown for Standby or Suspend Mode Operation with High-impedance Output

**Applications**

- DDR-SDRAM Termination
- DDR-II Termination
- SSTL-2 Termination



Figure 1. Package Types of AP2302



**3A DDR TERMINATION REGULATOR**

**AP2302**

**Pin Configuration**

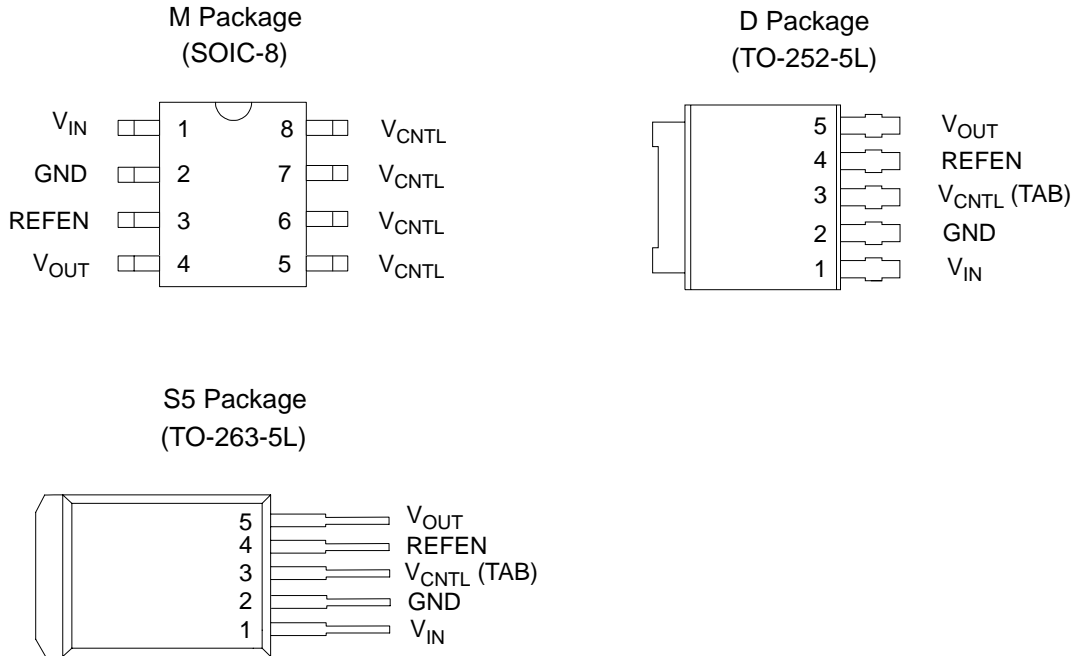


Figure 2. Pin Configuration of AP2302 (Top View)

**Pin Description**

Pin Number			Pin Name	Function
SOIC-8	TO-252-5L	TO-263-5L		
1	1	1	$V_{IN}$	Power Input
2	2	2	GND	Ground
3	4	4	REFEN	Reference Voltage Input and Chip Enable
4	5	5	$V_{OUT}$	Output Voltage
5, 6, 7, 8	3	3	$V_{CNTL}$	Supply Voltage for Internal Circuit (Internally Connected for SOIC-8), (TAB for TO-252-5L and TO-263-5L)



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**Functional Block Diagram**

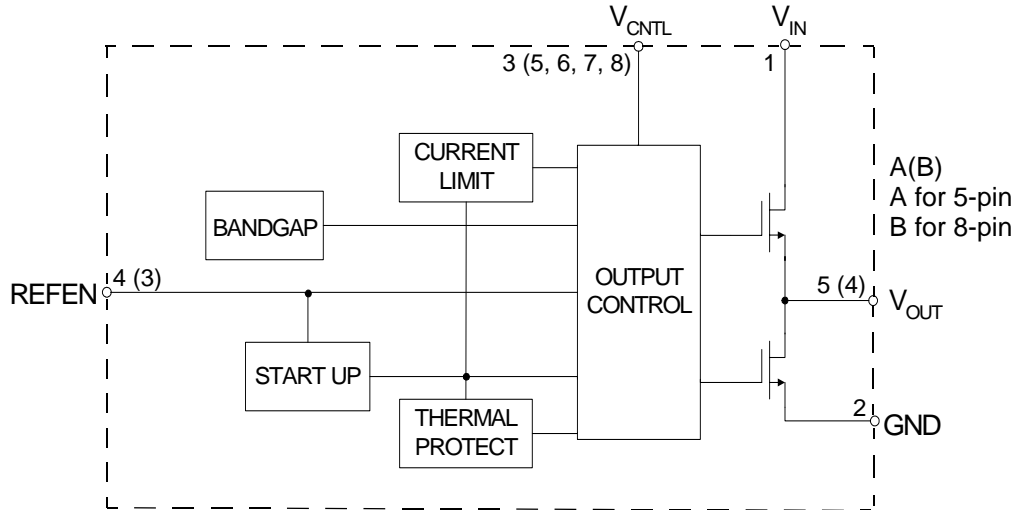
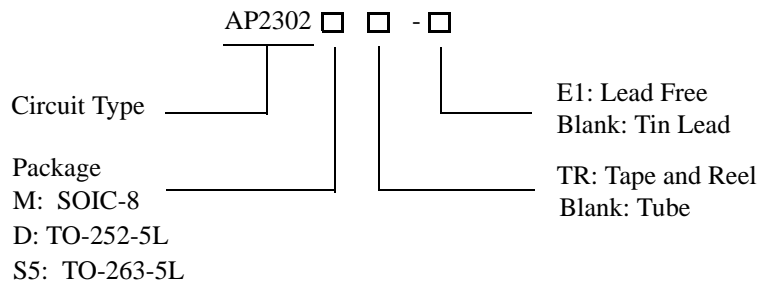


Figure 3. Functional Block Diagram of AP2302

**Ordering Information**



Package	Temperature Range	Part Number		Marking ID		Packing Type
		Tin Lead	Lead Free	Tin Lead	Lead Free	
SOIC-8	0 to 125°C	AP2302M	AP2302M-E1	2302M	2302M-E1	Tube
		AP2302MTR	AP2302MTR-E1	2302M	2302M-E1	Tape & Reel
TO-252-5L	0 to 125°C	AP2302D	AP2302D-E1	AP2302D	AP2302D-E1	Tube
		AP2302DTR	AP2302DTR-E1	AP2302D	AP2302D-E1	Tape & Reel
TO-263-5L	0 to 125°C	AP2302S5	AP2302S5-E1	AP2302S5	AP2302S5-E1	Tube
		AP2302S5TR	AP2302S5TR-E1	AP2302S5	AP2302S5-E1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "E1" suffix in the part number, are RoHS compliant.

**3A DDR TERMINATION REGULATOR****AP2302****Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Value		Unit
Supply Voltage for Internal Circuit	$V_{CNTL}$	7		V
Power Dissipation	$P_D$	Internally Limited		W
ESD (Human Body Model)	ESD	2		KV
Junction Temperature	$T_J$	150		°C
Storage Temperature Range	$T_{STG}$	-65 to 150		°C
Lead Temperature (Soldering, 10sec)	$T_{LEAD}$	260		°C
Package Thermal Resistance (Free Air)	$\theta_{JA}$	SOIC-8	160	°C/W
		TO-252-5L	130	
		TO-263-5L	90	

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for Internal Circuit	$V_{CNTL}$ (Note 2, 3)		3.3	6	V
Power Input	DDR I	1.6	2.5	$V_{CNTL}$	V
	DDR II		1.8		
Junction Temperature	$T_J$	0		125	°C

Note 2: Keep  $V_{CNTL} \geq V_{IN}$  in power on and power off sequences.

Note 3: For safe operation,  $V_{CNTL}$  MUST be tied to 3.3V rather than 5V.



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**Electrical Characteristics**

( $T_J=25^{\circ}\text{C}$ ,  $V_{IN}=2.5\text{V}$ ,  $V_{CNTL}=3.3\text{V}$ ,  $V_{REFEN}=1.25\text{V}$ ,  $C_{OUT}=10\mu\text{F}$  (Ceramic), unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Offset Voltage	$V_{OS}$	$I_L=0\text{A}$ (Note 4)	-20	0	20	mV
Load Regulation	DDR I	$I_L=0$ to 1.5A		0.8	2	%
		$I_L=0$ to -1.5A		0.8	2	
	DDR II	$I_L=0$ to 1.5A		1.2	3	
		$I_L=0$ to -1.5A		1.2	3	
Quiescent Current of $V_{CNTL}$	$I_Q$	No Load		3	5	mA
Leakage Current in Shutdown Mode	$I_{SHDN}$	$V_{REFEN}<0.2\text{V}$ , $R_L=180\Omega$		3	6	$\mu\text{A}$
<b>Protection</b>						
Current Limit	$I_{LIMIT}$		3			A
Thermal Shutdown Temperature	$T_{SHDN}$	$3.3\text{V}\leq V_{CNTL}\leq 5\text{V}$		150		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis				50		$^{\circ}\text{C}$
<b>Shutdown Function</b>						
Shutdown Threshold Trigger		Output=High	0.8			V
		Output=Low			0.2	

Note 4:  $V_{OS}$  is the voltage measurement defined as  $V_{OUT}$  subtracted from  $V_{REFEN}$ .



**3A DDR TERMINATION REGULATOR**

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**Typical Performance Characteristics**

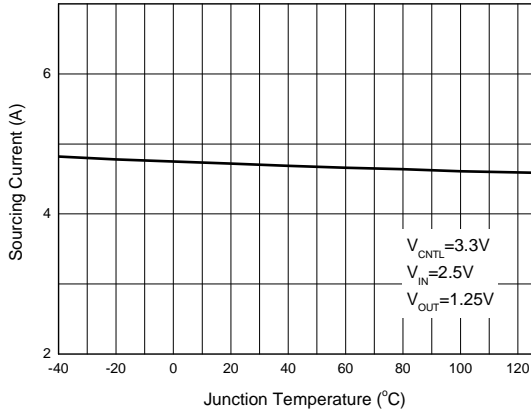


Figure 4. Sourcing Current vs. Junction Temperature

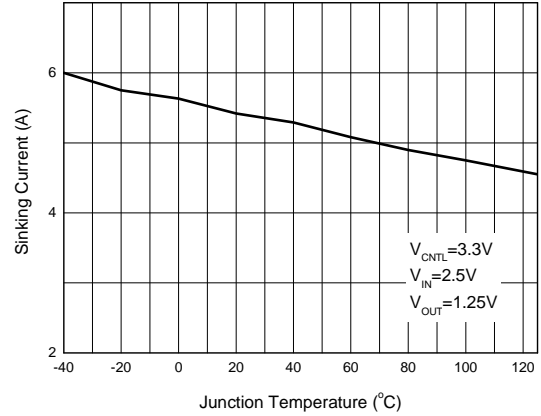


Figure 5. Sinking Current vs. Junction Temperature

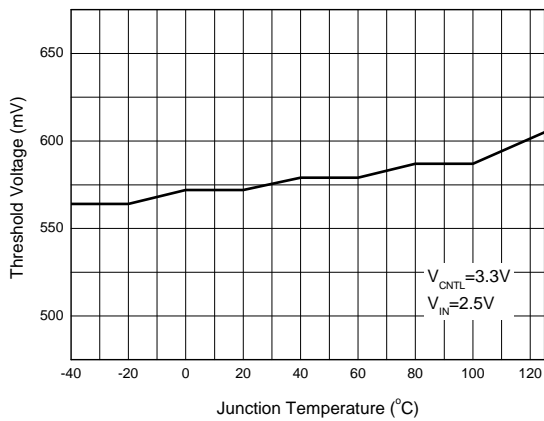


Figure 6. Threshold Voltage vs. Junction Temperature

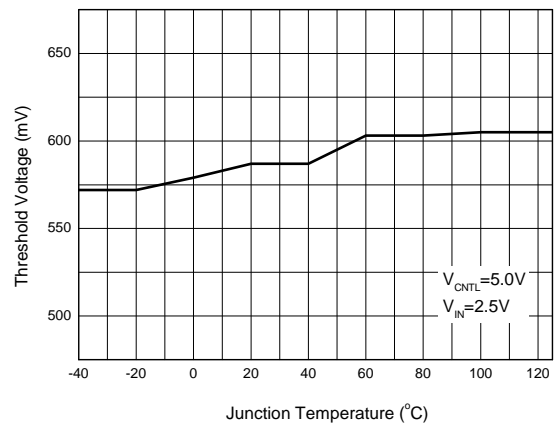


Figure 7. Threshold Voltage vs. Junction Temperature



**3A DDR TERMINATION REGULATOR**

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**Typical Performance Characteristics (Continued)**

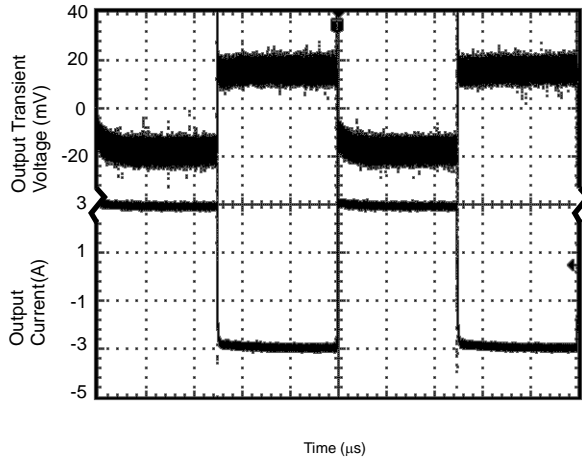


Figure 8. 0.9V<sub>TT</sub> at 3A Transient Response  
(Conditions: V<sub>IN</sub>=2.5V, V<sub>CNTL</sub>=3.3V, C<sub>OUT</sub>=10μF)

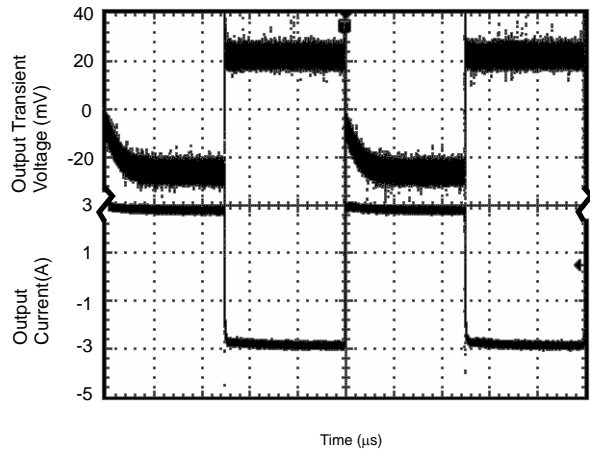


Figure 9. 1.25V<sub>TT</sub> at 3A Transient Response  
(Conditions: V<sub>IN</sub>=2.5V, V<sub>CNTL</sub>=3.3V, C<sub>OUT</sub>=10μF)

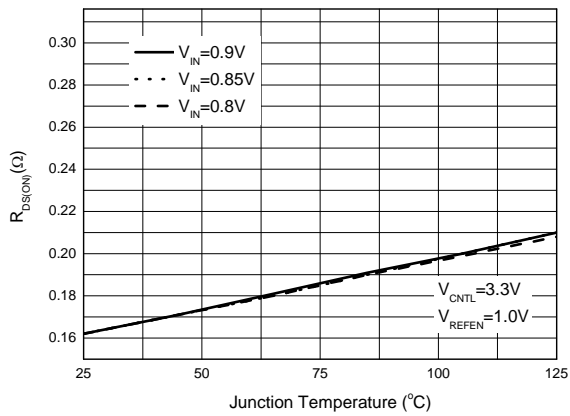


Figure 10. R<sub>DS(on)</sub> vs. Junction Temperature

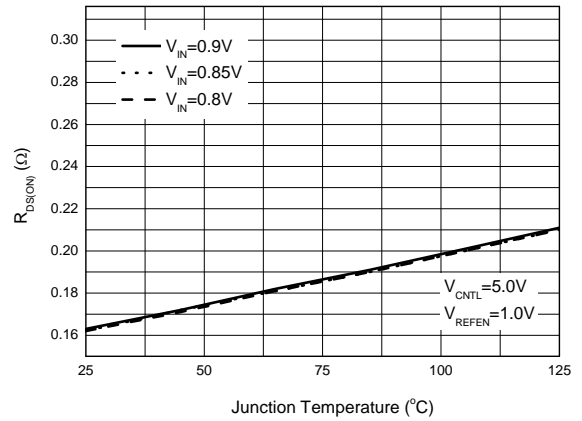


Figure 11. R<sub>DS(on)</sub> vs. Junction Temperature



**3A DDR TERMINATION REGULATOR**

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**Typical Performance Characteristics (Continued)**

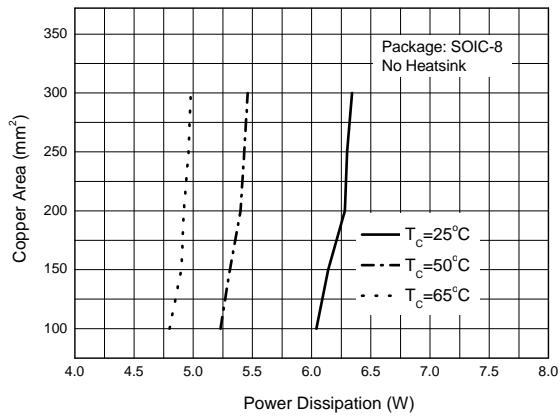


Figure 12. Copper Area vs. Power Dissipation

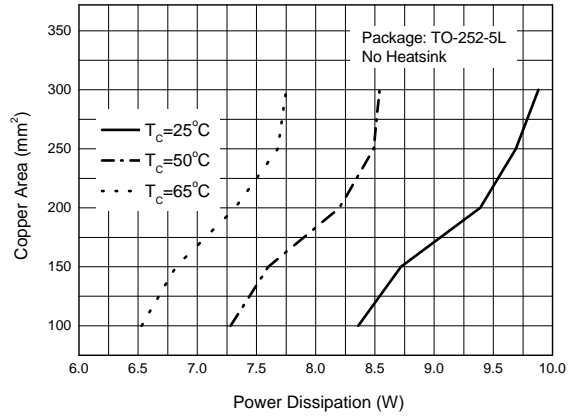


Figure 13. Copper Area vs. Power Dissipation

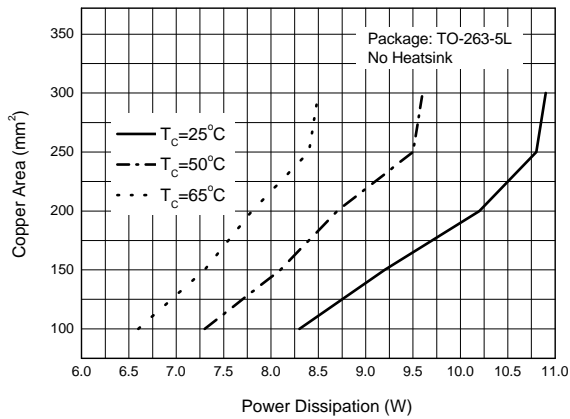


Figure 14. Copper Area vs. Power Dissipation





**3A DDR TERMINATION REGULATOR**

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**Typical Application**

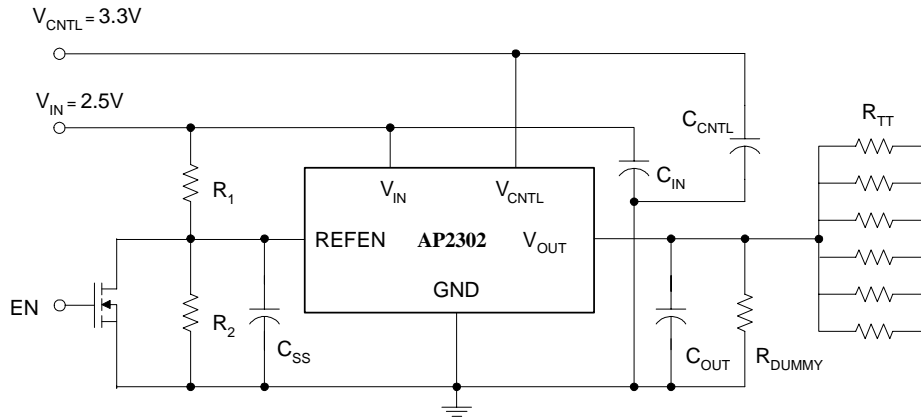


Figure 15. Typical Application of AP2302

$R_1=R_2=100K\Omega$ ,  $R_{TT}=50\Omega / 33\Omega / 25\Omega$

$R_{DUMMY}=1K\Omega$ , as for  $V_{OUT}$  discharge when  $V_{IN}$  is not present but  $V_{CNTRL}$  is present

$C_{SS}=1\mu F$ ,  $C_{IN}=470\mu F$ ,  $C_{CNTRL}=47\mu F$ ,  $C_{OUT}=470\mu F$



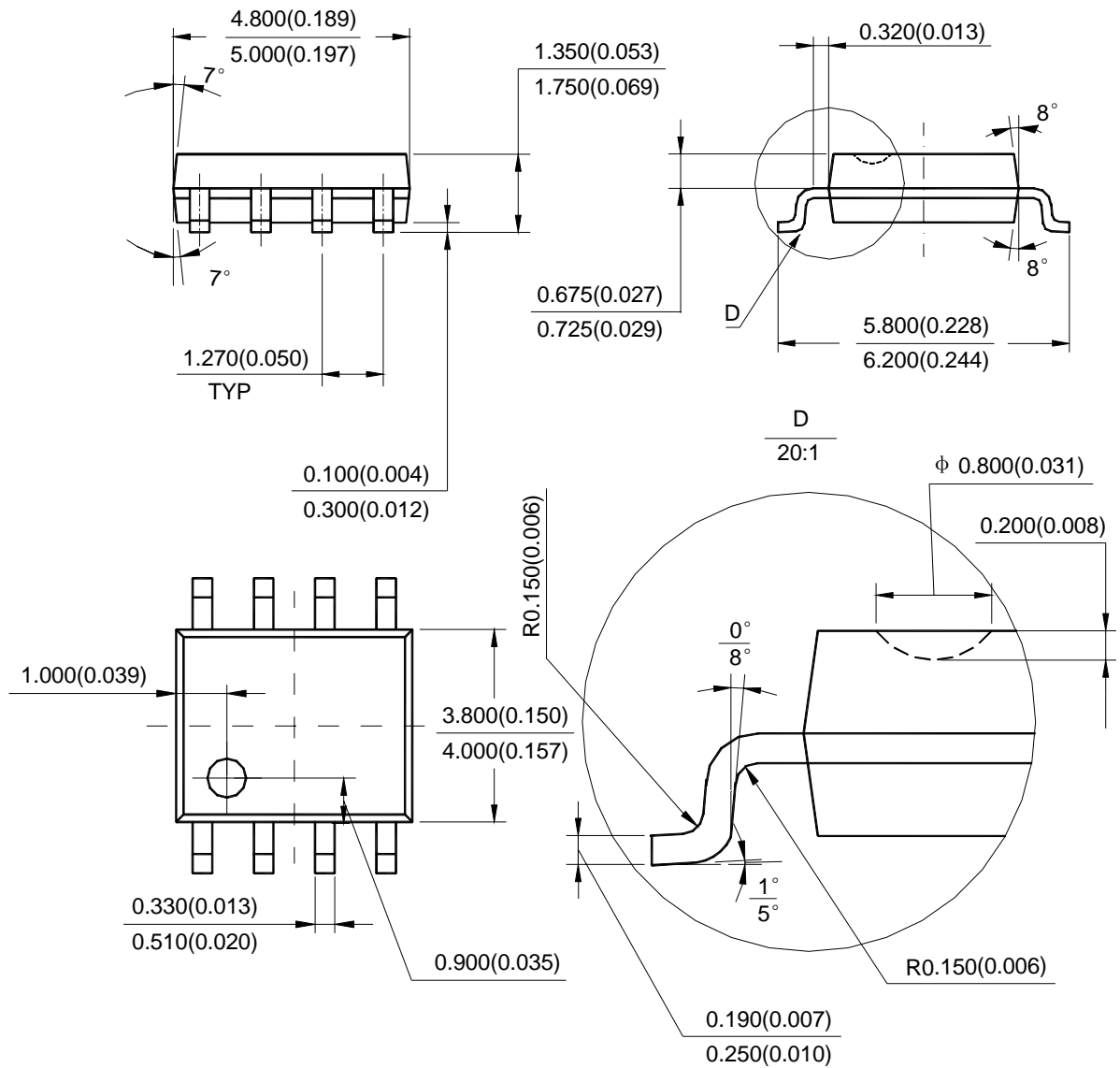
**3A DDR TERMINATION REGULATOR**

**AP2302**

**Mechanical Dimensions**

**SOIC-8**

**Unit: mm(inch)**





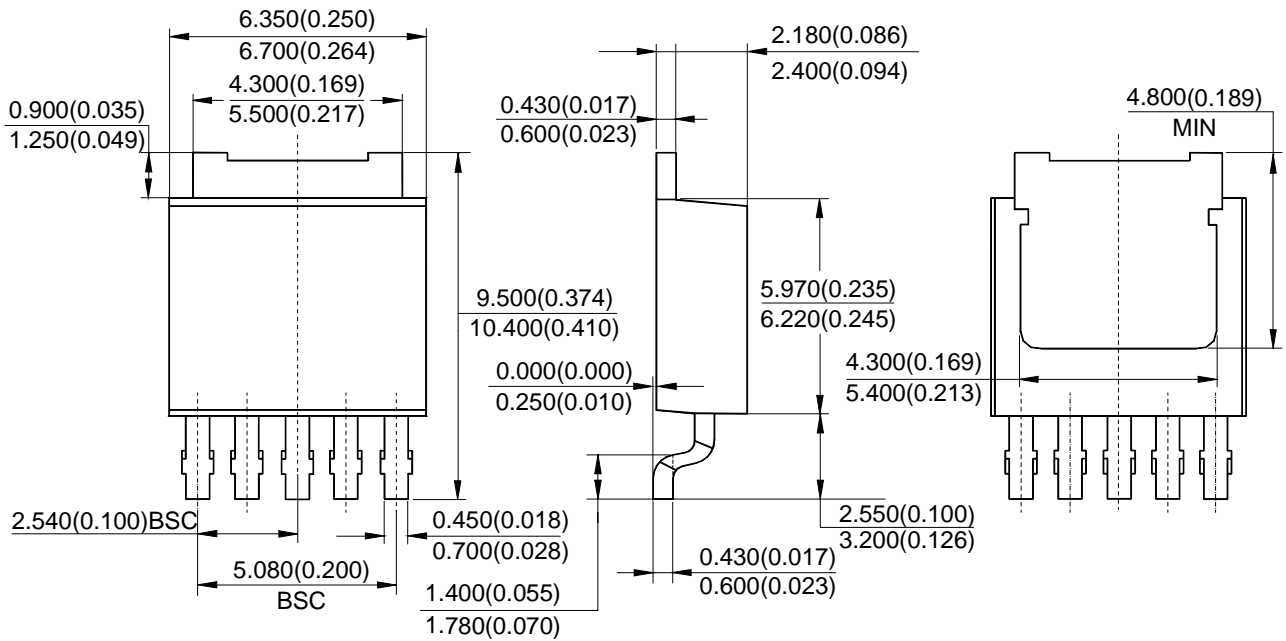
**3A DDR TERMINATION REGULATOR**

**AP2302**

**Mechanical Dimensions (Continued)**

**TO-252-5L**

**Unit: mm(inch)**





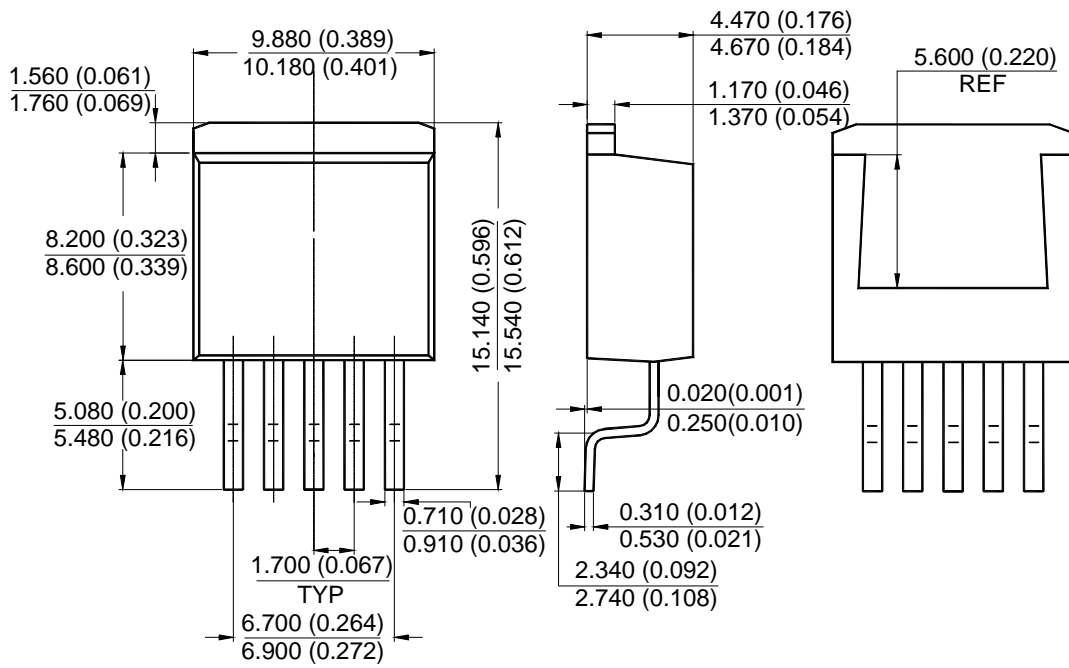
**3A DDR TERMINATION REGULATOR**

**AP2302**

**Mechanical Dimensions (Continued)**

**TO-263-5L**

**Unit: mm(inch)**





BCD Semiconductor Manufacturing Limited

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