**FLASH-ROM MODULE 2MByte (512K x32-Bit) –68-Pin JLCC**
**Part No. HMF51232J4V**

## GENERAL DESCRIPTION

The HMF51232J4V is a high-speed flash read only memory (FROM) module containing 524,288 words organized in a x32bit configuration. The module consists of four 512Kx 8 FROM mounted on a 68-pin, JLCC FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Four chip enable inputs, (/CE1, /CE2, /CE3, /CE4) are used to enable the module 's 4 bytes independently. Output enable (/OE) and write enable (/WE) can set the memory input and output.

When FROM module is disable condition, the module is becoming power standby mode, system designer can get low-power design.

All module components may be powered from a single +3.3V DC power supply and all inputs and outputs are LVTTL-compatible.

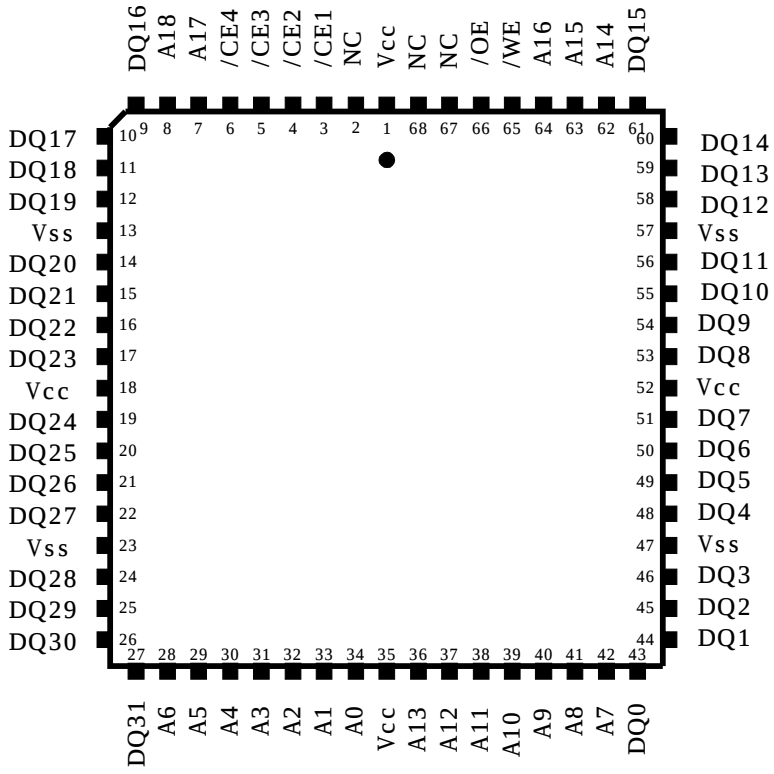
## FEATURES

- Access time : 55,70, 90 and 120ns
- High-density 2MByte design
- High-reliability, low-power design
- Single + 3V ± 0.3V power supply
- Easy memory expansion
- All inputs and outputs are TTL-compatible
- FR4-PCB design
- Low profile 68-pin JLCC
- Minimum 1,000,000 write/erase cycle
- Sector erases architecture
- Sector group protection
- Temporary sector group unprotection
- The used device is Am29LV040B

## OPTIONS MARKING

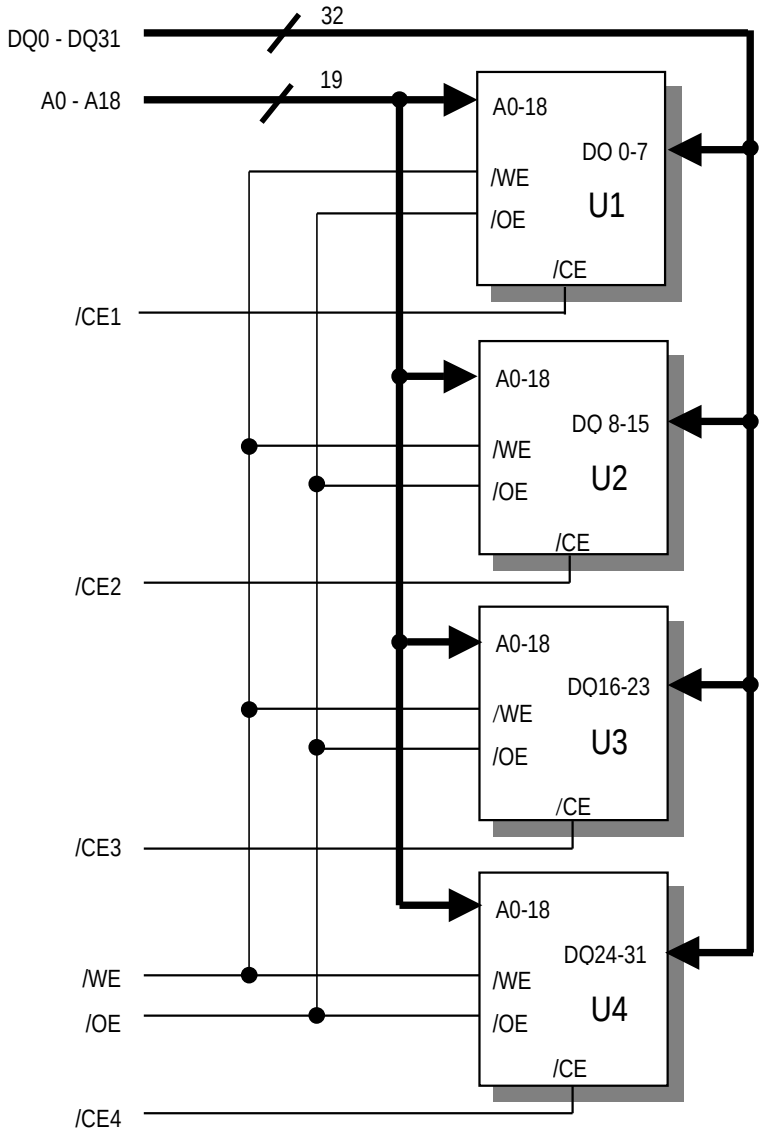
- Timing
  - 55ns access -55
  - 70ns access -70
  - 90ns access -90
  - 120ns access -120
- Packages
  - 68-pin JLCC J

## PIN ASSIGNMENT




**68-pin JLCC**
**TOP VIEW**

## FUNCTIONAL BLOCK DIAGRAM




## TRUTH TABLE

| MODE | /CE | /OE | /WE | DQ | ADDRESSES |
|---|---|---|---|---|---|
| READ | L | L | H | DOUT | AIN |
| WRITE | L | H | L | DIN | AIN |
| STANDBY | Vcc±0.3V | X | X | HIGH-Z | X |
| OUTPUT DISABLE | L | H | H | HIGH-Z | X |
| Reset | X | X | X | HIGH-Z | X |
| Sector Protect | L | H | L | DIN,DOUT | Sector Address, A6=L,A1=H,A0=L |

| | | | | | |
|---|---|---|---|---|---|
| Sector Unprotect | L | H | L | DIN,DOUT | Sector Address, A6=L,A1=H,A0=L |
| Temporary Sector Unprotect | X | X | X | DIN | AIN |

Note : X means don't care

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING |
|---|---|---|
| Voltage with respect to ground all other pins | $V_{IN,OUT}$ | -0.5V to Vcc +0.5V |
| Voltage with respect to ground Vcc | $V_{CC}$ | -0.5V to +4.0V |
| Storage Temperature | $T_{STG}$ | -65°C to +150°C |
| Operating Temperature | $T_A$ | -55°C to +125°C |

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP. | MAX |
|---|---|---|---|---|
| Vcc for regulated voltage range | $V_{CC}$ | 3.0V | | 3.6V |
| Vcc for full voltage range | Vcc | 2.7V | | 3.6V |
| Ground | $V_{SS}$ | 0 | 0 | 0 |

## DC AND OPERATING CHARACTERISTICS ($0^oC \leq T_A \leq 70\ ^oC$ ; Vcc = 5V ± 0.5V )

| PARAMETER | TEST CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Input Leakage Current | Vcc=Vcc max, $V_{IN}$= GND to Vcc | $I_{L1}$ | | ±1.0 | µA |
| Output Leakage Current | Vcc=Vcc max, $V_{out}$= GND to Vcc | $I_{L0}$ | | ±1.0 | µA |
| Output High Voltage | $I_{OH}$ = -2.0mA, Vcc = Vcc min | $V_{OH}$ | 0.85Vcc | | V |
| Output Low Voltage | $I_{OL}$ = 4.0mA, Vcc =Vcc min | $V_{OL}$ | | 0.45 | V |
| Vcc Active Current for Read(1) | /CE = $V_{IL}$, /OE=$V_{IH}$, f=5mHz | $I_{CC1}$ | | 12 | mA |
| Vcc Active Current for Program or Erase(2) | /CE = $V_{IL}$, /OE=$V_{IH}$ | $I_{CC2}$ | | 30 | mA |
| Vcc Standby Current | /CE=Vcc±0.3V | $I_{CC3}$ | | 5 | mA |
| Vcc Reset Current | | $I_{CC4}$ | | 5 | mA |
| Low Vcc Lock-Out Voltage | | $V_{LKO}$ | 2.3 | 2.5 | V |

**Notes:**

1. The Icc current listed is typically less than than 2mA/MHz, with /OE at $V_{IH}$. Typical Vcc is 3.0V
2. Icc active while embedded algorithm (program or erase) is in progress
3. Maximum Icc current specifications are tested with Vcc=Vcc max

## ERASE AND PROGRAMMING PERFORMANCE

| PARAMETER | LIMITS | | | UNIT | COMMENTS |
|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | | |
| Sector Erase Time | - | 1.7 | 15 | sec | Excludes 00H programming prior to erasure |
| Byte Programming Time | - | 9 | 300 | us | Excludes system-level overhead |
| Chip Programming Time | - | 4.5 | 13.5 | sec | Excludes system-level overhead |

## CAPACITANCE

| PARAMETER SYMBOL | PARAMETER DESCRIPTION | TEST SETUP | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 7.5 | 9 | pF |

**Notes** : Test conditions $T_A$ = 25°C, f=1.0 MHz.

## AC CHARACTERISTICS

### u Read Only Operations Characteristics

| PARAMETER SYMBOLS | | DESCRIPTION | TEST SETUP | | -55 | -90 | UNIT |
|---|---|---|---|---|---|---|---|
| JEDEC | STANDARD | | | | | | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | Min | 55 | 90 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | /CE = $V_{IL}$ /OE = $V_{IL}$ | Max | 55 | 90 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | /OE = $V_{IL}$ | Max | 55 | 90 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Chip Enable to Output Delay | | Max | 30 | 35 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High-Z | | Max | 25 | 30 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High-Z | | Max | 25 | 30 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First | | Min | 0 | 0 | ns |

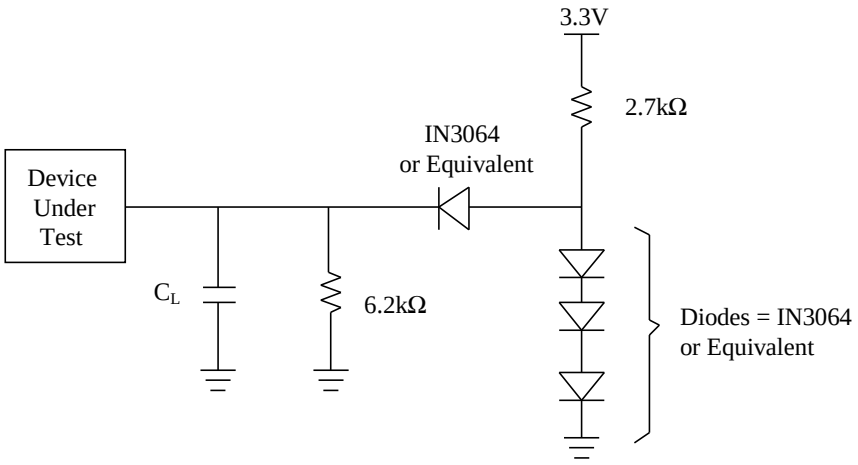
**Notes** : Test Conditions : Output Load : 1TTL gate and 100 pF

Input rise and fall times : 5 ns

Input pulse levels : 0V to 3.0V

Timing measurement reference level

Input : 1.5V / Output : 1.5V




Note : $C_L$ = 100pF including jig capacitance

## u Write/Erase/Program Operations

### Alternate /WE Controlled Writes

| PARAMETER SYMBOLS | | DESCRIPTION | | -55 | -90 | UNIT |
|---|---|---|---|---|---|---|
| JEDEC | STANDARD | | | | | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | Min | 55 | 90 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | Min | 0 | 0 | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | Min | 45 | 45 | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | Min | 35 | 45 | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | Min | 0 | 0 | ns |
| | $t_{OES}$ | Output Enable Setup Time | Min | 0 | 0 | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recover Time Before Write | Min | 0 | 0 | ns |
| $t_{ELWL}$ | $t_{CS}$ | /CE Setup Time | Min | 0 | 0 | ns |
| $t_{WHEH}$ | $t_{CH}$ | /CE Hold Time | Min | 0 | 0 | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | Min | 35 | 35 | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Pulse Width High | Min | 30 | 30 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Byte Programming Operation | Typ | 9 | 9 | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note1) | Typ | 0.7 | 0.7 | sec |
| | $t_{VCS}$ | Vcc Setup Time | Min | 50 | 50 | µs |

**Notes** :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

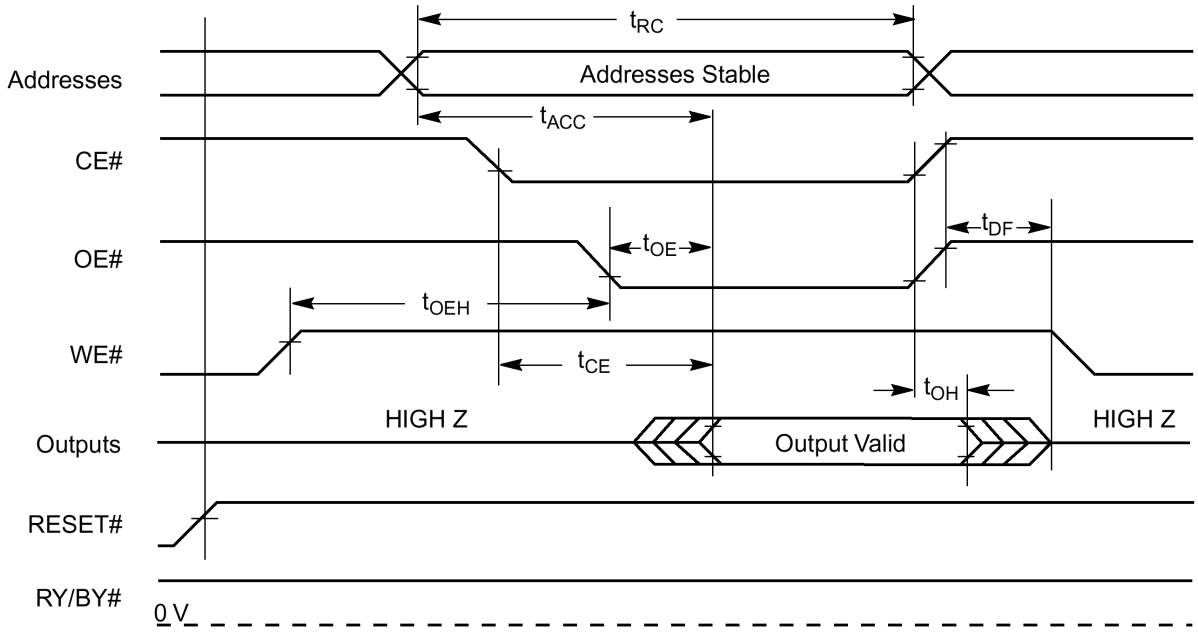
## u Write/Erase/Program Operations

### Alternate /CE Controlled Writes

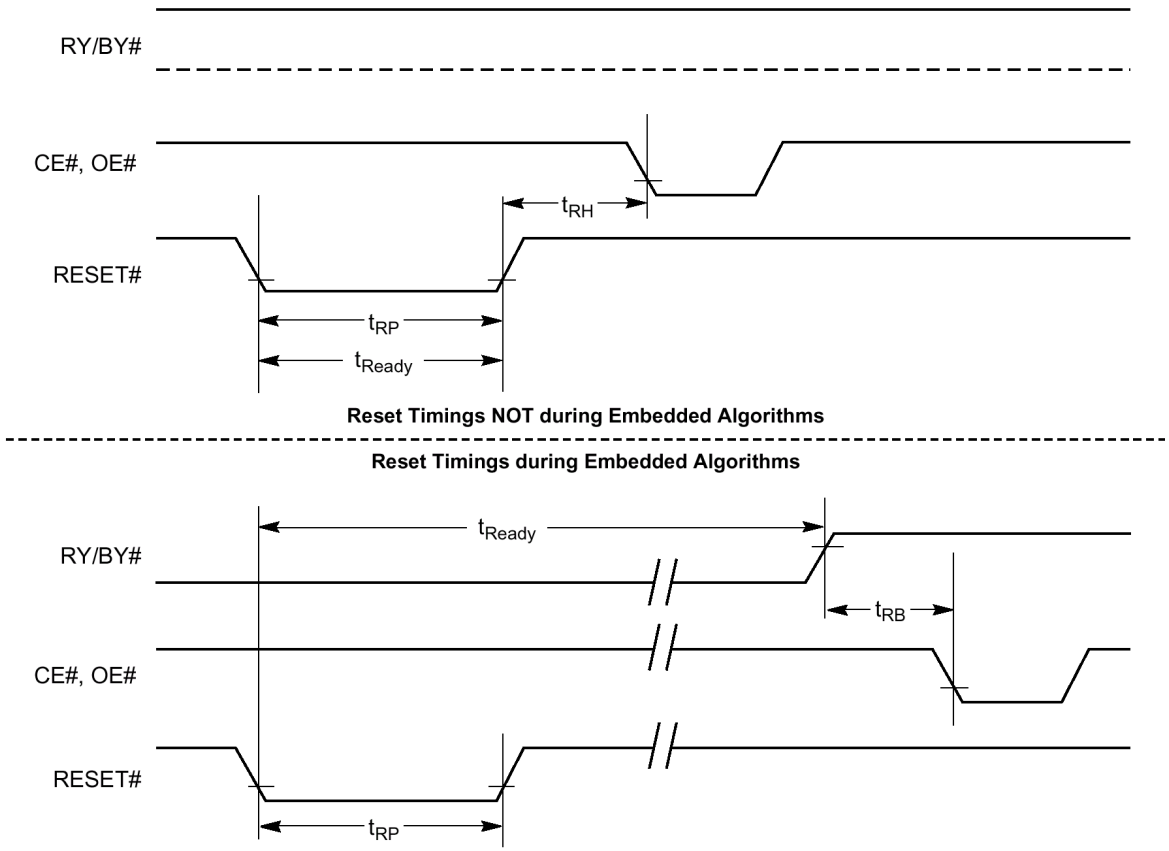
| PARAMETER SYMBOLS | | DESCRIPTION | | -55 | -90 | UNIT |
|---|---|---|---|---|---|---|
| JEDEC | STANDARD | | | | | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | Min | 55 | 90 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time | Min | 0 | 0 | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | Min | 45 | 45 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | Min | 35 | 45 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | Min | 0 | 0 | ns |
| | $t_{OES}$ | Output Enable Setup Time | Min | 0 | 0 | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recover Time Before Write | Min | 0 | 0 | ns |
| $t_{WLEL}$ | $t_{WS}$ | /WE Setup Time | Min | 0 | 0 | ns |
| $t_{EHWH}$ | $t_{WH}$ | /WE Hold Time | Min | 0 | 0 | ns |
| $t_{ELEH}$ | $t_{CP}$ | /CE Pulse Width | Min | 35 | 35 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | /CE Pulse Width High | Min | 30 | 30 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Byte Programming Operation | Typ | 9 | 9 | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note) | Typ | 0.7 | 0.7 | sec |

**Notes** : This does not include the preprogramming time.

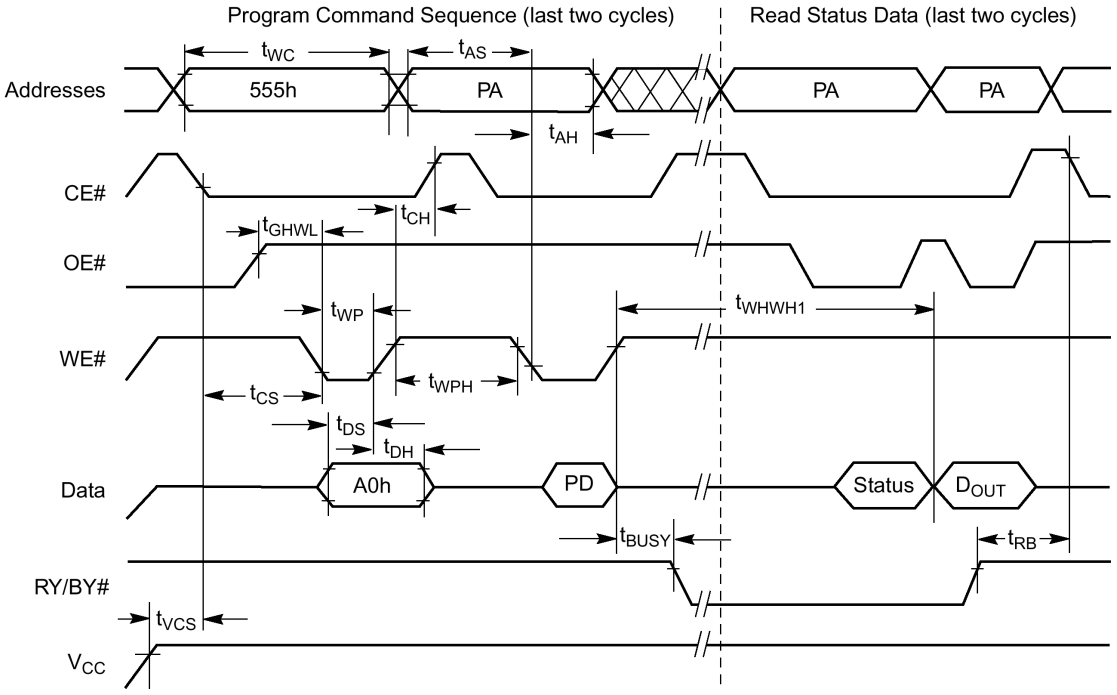
## u READ OPERATIONS TIMING



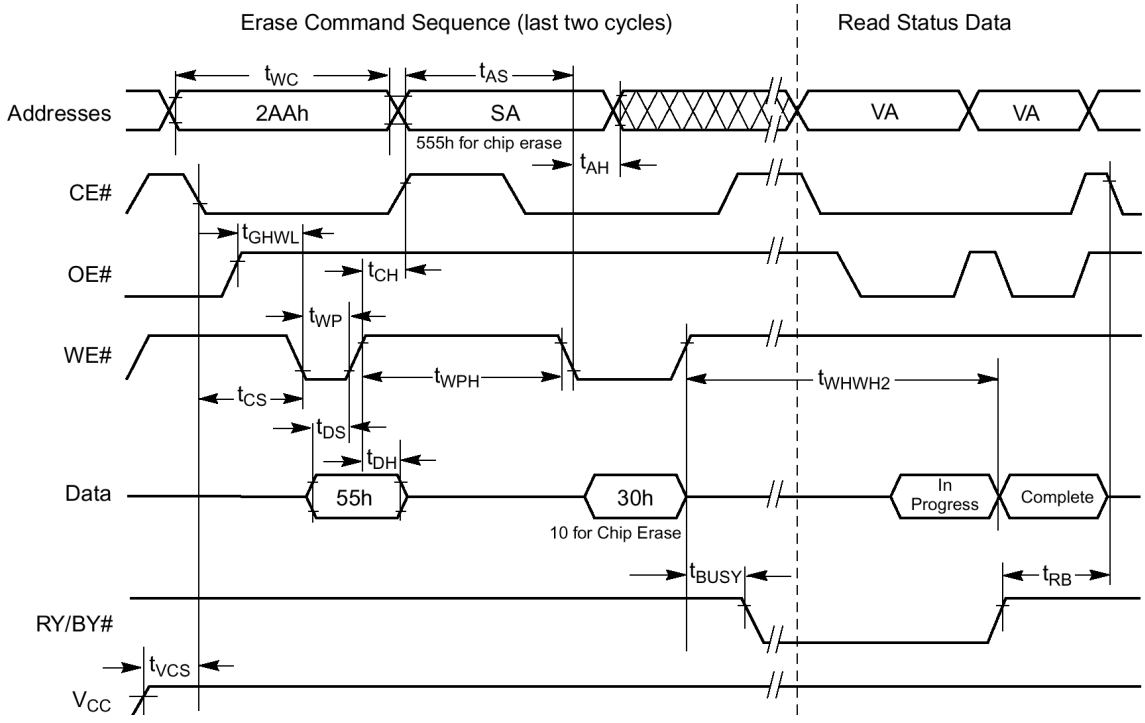

## u RESET TIMING



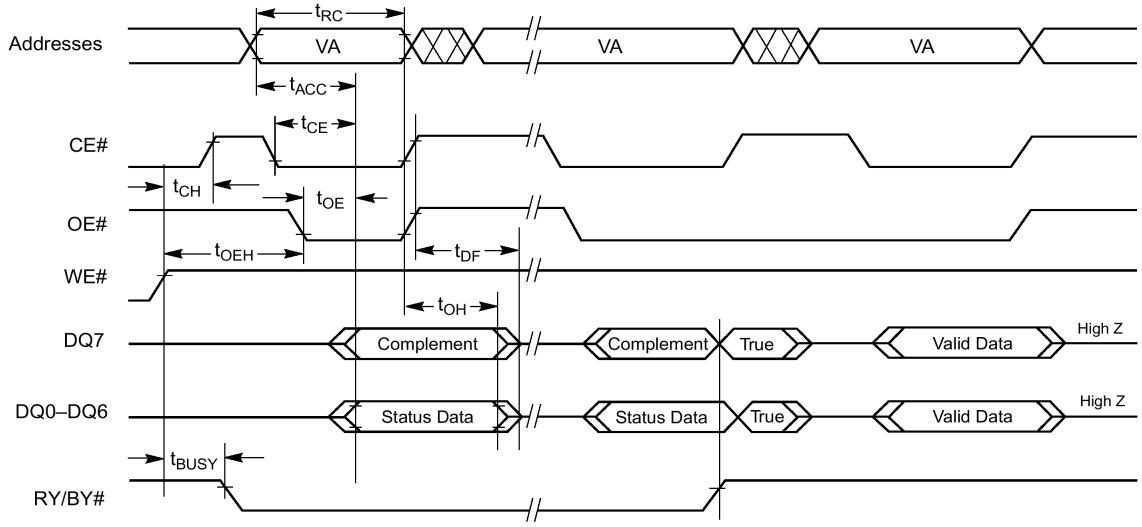
## u PROGRAM OPERATIONS TIMING



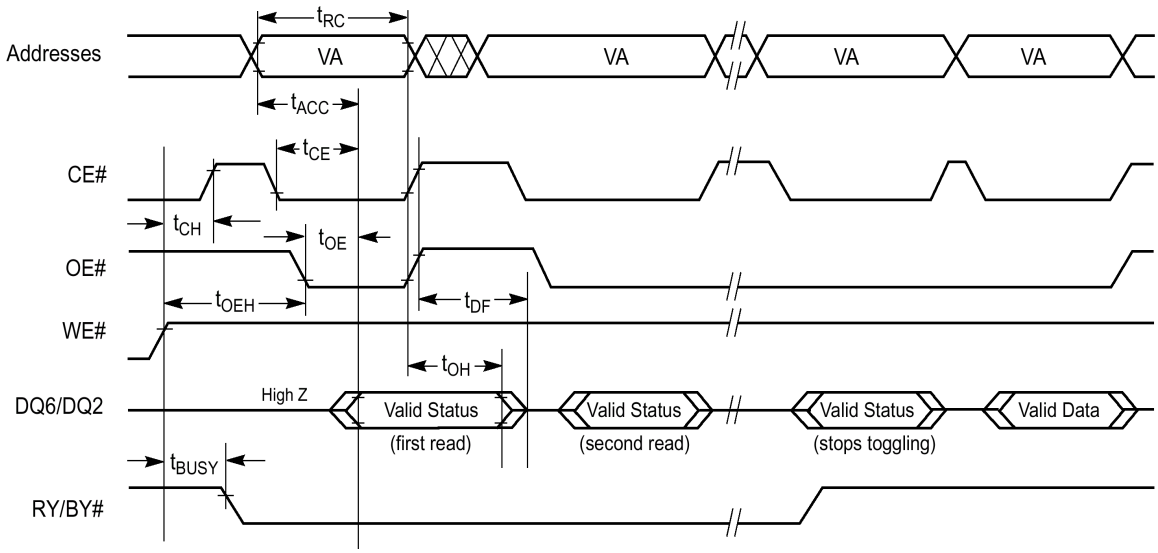

## u CHIP/SECTOR ERASE OPERATION TIMINGS



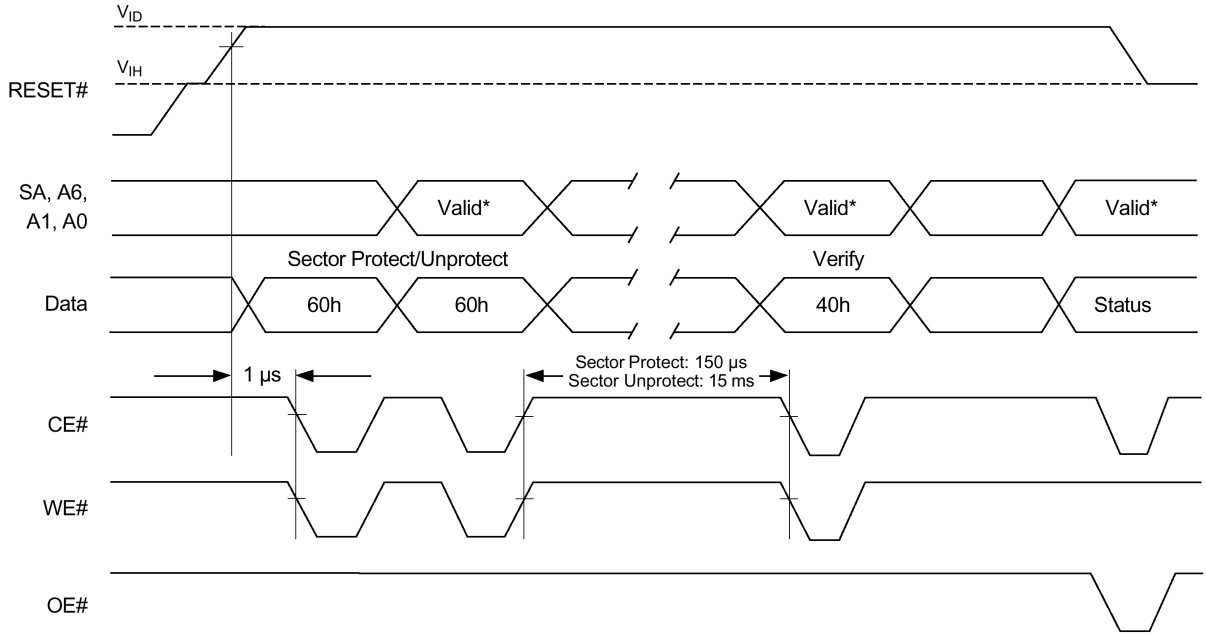
## u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



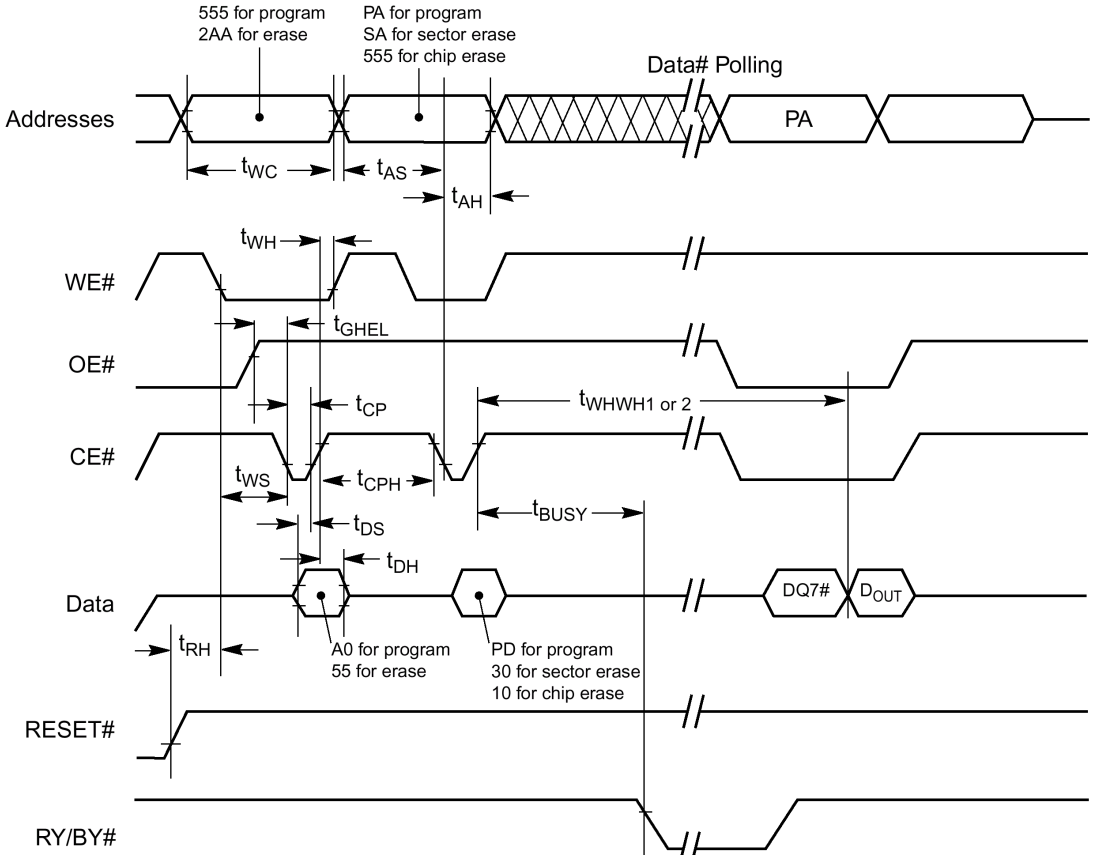

## u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



## u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

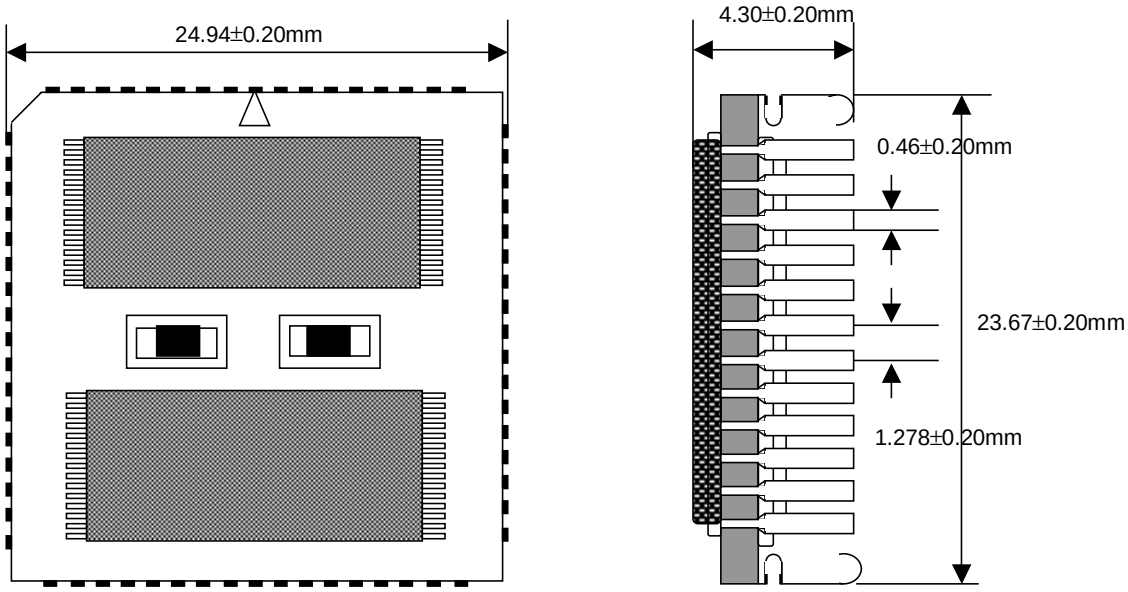



## u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



## PACKAGE DIMENSIONS

**68-Pin JLCC**




## ORDERING INFORMATION

| Part Number | Density | Org. | Package | Component Number | Vcc | SPEED |
|---|---|---|---|---|---|---|
| **HMF51232J4V-55** | 2MByte | 512k×32bit | 68Pin-JLCC | 4EA | 3.3V | 55ns |
| **HMF51232J4V-70** | 2MByte | 512k×32bit | 68 Pin-JLCC | 4EA | 3.3V | 70ns |
| **HMF51232J4V-90** | 2MByte | 512k×32bit | 68 Pin-JLCC | 4EA | 3.3V | 90ns |
| **HMF51232J4V-120** | 2MByte | 512k×32bit | 68 Pin-JLCC | 4EA | 3.3V | 120ns |