HMC940LC4B

13 Gbps, 1:4 FANOUT BUFFER w/ PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC940LC4B is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 13 Gbps
- Clock Buffering up to 13 GHz

Features

Inputs Terminated Internally in 50 Ohms

Differential Inputs are DC Coupled

Propagation Delay: 101 ps

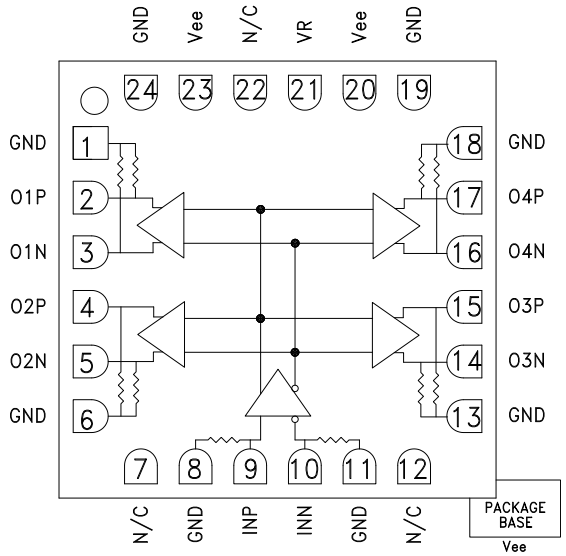
Fast Rise and Fall Times: 26 / 25 ps

Programmable Differential
Output Voltage Swing: 600 - 1400 mV

Power Dissipation: 440 mW

24 Lead Ceramic 4x4 mm SMT Package: 16 mm^2

Functional Diagram



General Description

The HMC940LC4B is a 1:4 Fanout Buffer designed to support data transmission rates up to 13 Gbps, and clock frequencies as high as 13 GHz. All differential inputs and outputs are DC coupled and terminated on chip with 50 Ohm resistors to ground. The outputs may be used in either single-ended or differential modes, and should be AC or DC coupled into 50 Ohm resistors connected to ground.

The HMC940LC4B also features an output level control pin, VR which allows for loss compensation or for signal level optimization. The HMC940LC4B operates from a single -3.3V DC supply and is available in a ceramic RoHS compliant 4x4 mm SMT package.

Electrical Specifications, T_A = +25 °C Vee = -3.3V, VR = 0V

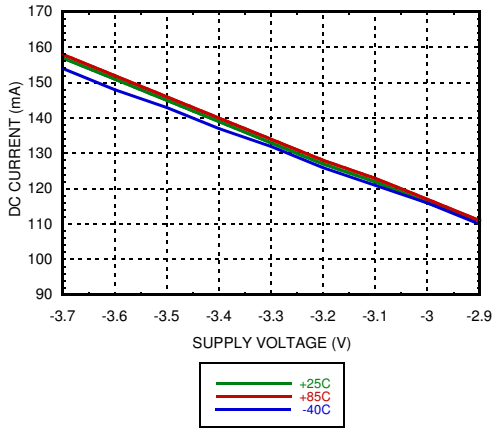
Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage (Vee)		-3.6	-3.3	-3.0	V
Power Supply Current			133		mA
Maximum Data Rate			13		Gbps
Maximum Clock Rate			13		GHz
Input High Voltage		-0.5		0.5	V
Input Low Voltage		-1.0		0.0	V
Input Return Loss	Frequency <15 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		585		mVp-p
	Differential, peak-to-peak		1170		mVp-p
Output High Voltage			-15		mV
Output Low Voltage			-600		mV
Output Rise / Fall Time	Single-Ended, 20% - 80%		26 / 25		ps

Electrical Specifications (continued)

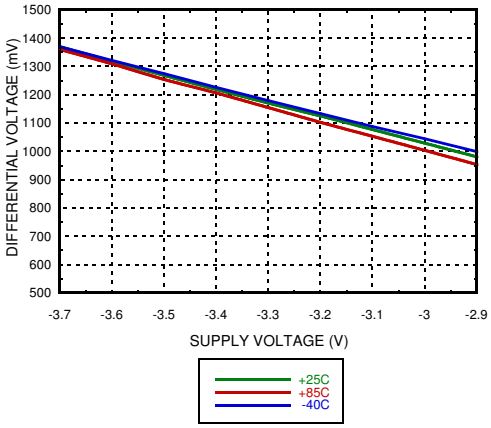
Parameter	Conditions	Min.	Typ.	Max	Units
Output Return Loss	Frequency <13 GHz		10		dB
Small Signal Gain			20		dB
Random Jitter J_R	rms			0.2	ps rms
Deterministic Jitter, J_D	δ - δ, 2^{15}-1 PRBS input [1]		4	6	ps
Propagation Delay, td			101		ps
D1 to D2 Data Skew, t_{SKEW}			±3		ps

[1] Deterministic jitter measured at 13 Gbps with a 300 mVp-p, 2^{15}-1 PRBS input sequence.

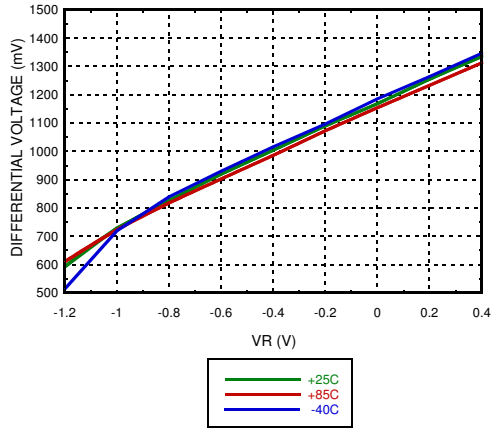
DC Current vs. Supply Voltage [1] [2]



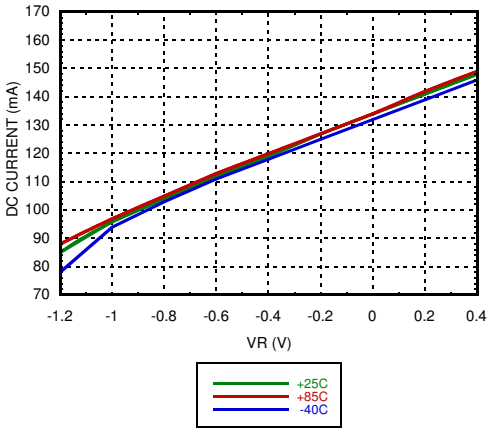
Output Differential vs. Supply Voltage [1] [2]



Output Differential vs. VR [2][3]



DC Current vs. VR [2][3]



[1] VR = 0.0V [2] Frequency = 13 GHz [3] Vee = -3.3V

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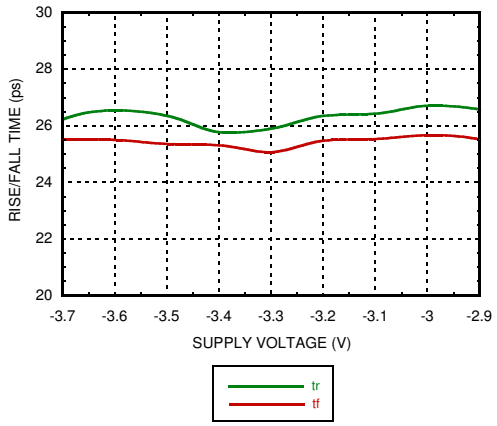
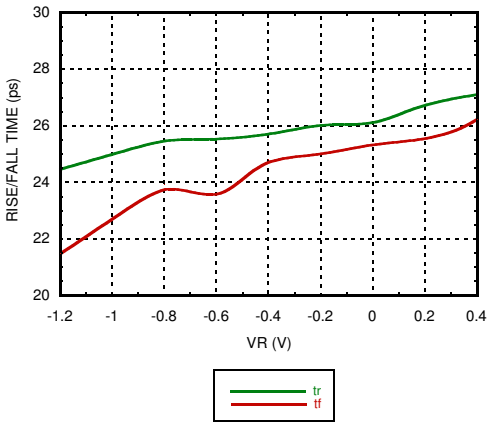
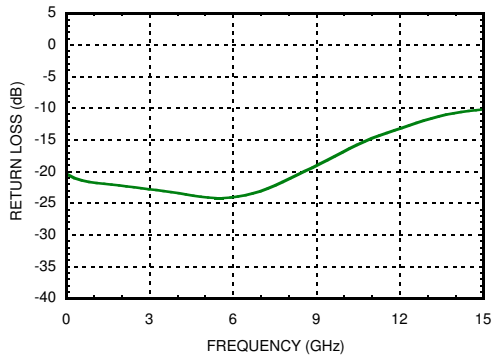
Rise / Fall Time vs. Supply Voltage [1][2]



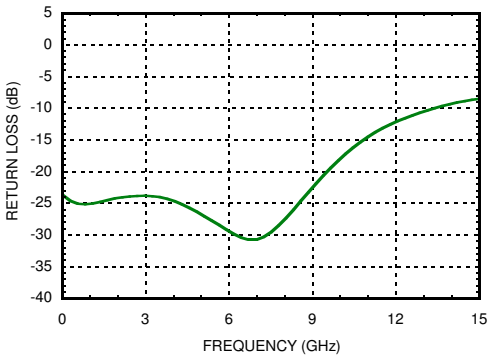
Rise / Fall Time vs. VR [2][5]



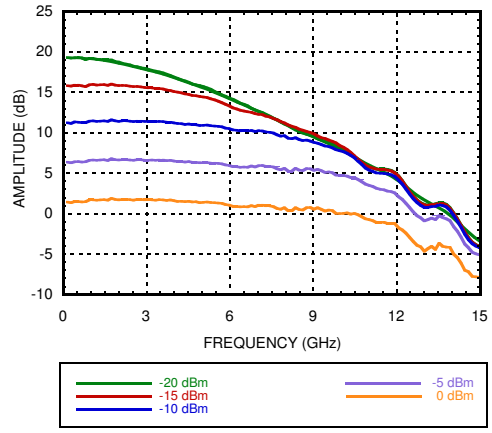
Input Return Loss vs. Frequency [1][3][5]



Output Return Loss vs. Frequency [1][3][5]



Amplitude vs. Input Power [1][4][5]

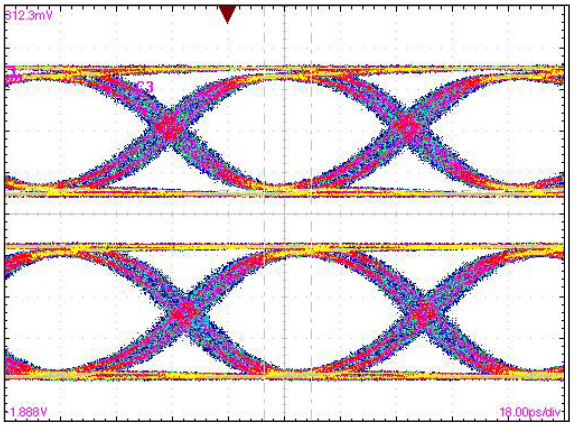


Truth Table

Input	Outputs
IN	Ox
L	L
H	H
Notes: IN = INP - INN Ox = OxP - OxN	H - Positive differential voltage L - Negative differential voltage

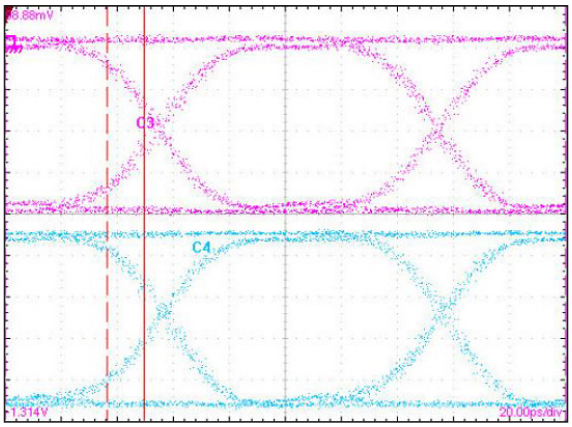
[1] VR = 0.0V [2] Frequency = 13 GHz [3] Device measured on evaluation board with gating after connector
[4] Device measured on evaluation board with port extensions [5] Vee = -3.3V

Eye Diagram



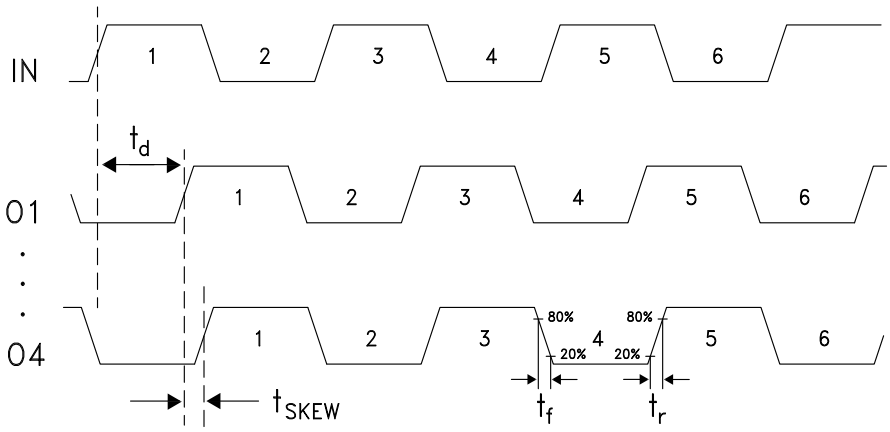
[1] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 13 Gbps PN code, Vin = 300 mVp-p differential.
Both output channels shown.

Eye Diagram



[2] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 10 Gbps PN code, Vin = 300 mVp-p differential.
Both output channels shown.

Timing Diagram



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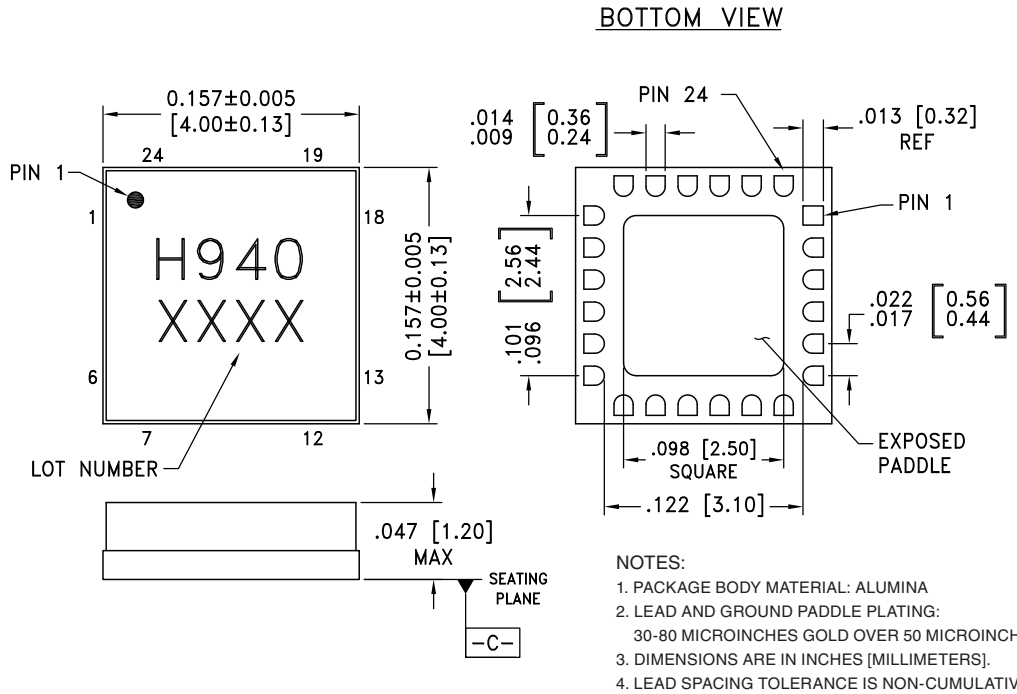
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +1 V
Junction Temperature	125 °C
Continuous Pdiss (T=85 °C) (derate 30 mW/°C above 85 °C	1.22 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worse case junction to package paddle	32.8 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



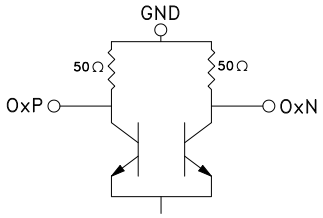
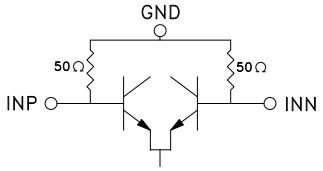
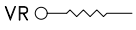
NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. EXPOSED PADDLE MUST BE SOLDERED TO VEE

Package Information

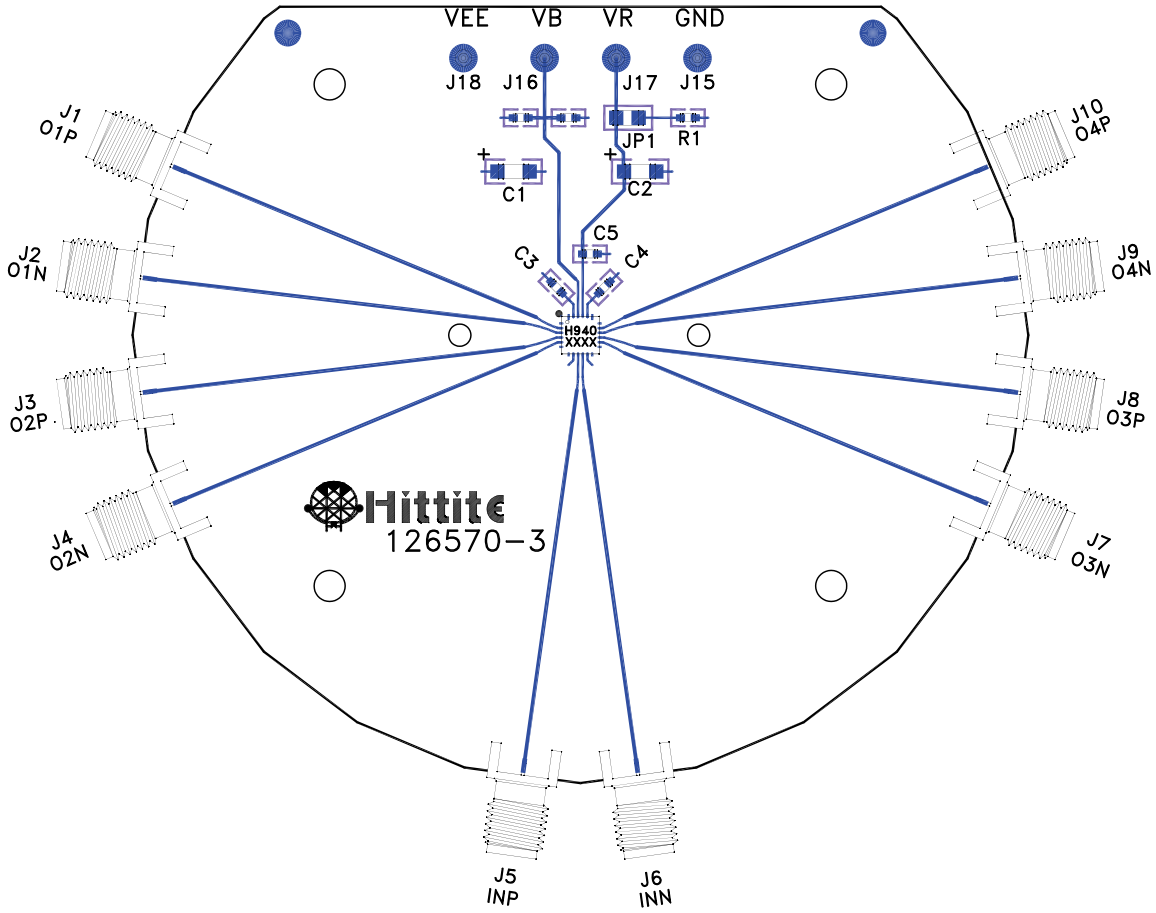
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC940LC4B	Alumina, White	Gold over Nickel	MSL3 [1]	H940 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 8, 11, 13, 18, 19, 24	GND	These pins must be connected to a high quality RF/DC ground.	
2, 3, 4, 5, 14, 15, 16, 17	O1P, O1N, O2P, O2N, O3N, O3P, O4N, O4P	Differential Outputs: Current Mode Logic (CML) referenced to positive supply.	
7, 12, 22	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
9, 10	INP, INN	Differential Inputs: Current Mode Logic (CML) referenced to positive supply	
20, 23 Package Base	Vee	These pins and the exposed paddle must be connected to the negative voltage supply.	
21	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per “Output Differential vs. VR” plot.	

Evaluation PCB



List of Materials for Evaluation PCB 126572 [1]

Item	Description
J1 - J10	PCB Mount SMA RF Connectors
J15 - J18	DC Pin
JP1	0.1" Header with Shorting Jumper
C1, C2	4.7 µF Capacitor, Tantalum
C3 - C5	100 pF, Capacitor, 0603 Pkg
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC940LC4B High Speed Logic, Fanout Buffer
PCB [2]	126570 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

Application Circuit