Ultrafast TTL Comparators

AD9696/AD9698

FEATURES
4.5 ns Propagation Delay
200 ps Maximum Propagation Delay Dispersion
Single +5 V or ±5 V Supply Operation
Complementary Matched TTL Outputs

APPLICATIONS
High Speed Line Receivers
Peak Detectors
Window Comparators
High Speed Triggers
Ultrafast Pulse Width Discriminators

GENERAL DESCRIPTION

The AD9696 and AD9698 are ultrafast TTL-compatible voltage comparators able to achieve propagation delays previously possible only in high performance ECL devices. The AD9696 is a single comparator providing 4.5 ns propagation delay, 200 ps maximum delay dispersion and 1.7 ns setup time. The AD9698 is a dual comparator with equally high performance; both devices are ideal for critical timing circuits in such applications as ATE, communications receivers and test instruments.

Both devices allow the use of either a single +5 V supply or ±5 V supplies. The choice of supplies determines the common mode input voltage range available: -2.2 V to +3.7 V for ±5 V operation, +1.4 V to +3.7 V for single +5 V supply operation.

The differential input stage features high precision, with offset voltages which are less than 2 mV and offset currents less than 1 µA. A latch enable input is provided to allow operation in either sample-and-hold or track-and-hold applications.

The AD9696 and AD9698 are both available as commercial temperature range devices operating from ambient temperatures of 0°C to +70°C, and as extended temperature range devices for ambient temperatures from -55°C to +125°C. Both versions are available qualified to MIL-STD-883 class B.

Package options for the AD9696 include a 10-pin TO-100 metal can, an 8-pin ceramic DIP, an 8-pin plastic DIP, and an 8-lead small outline plastic package. The AD9698 is available in a 16-pin ceramic DIP, a 16-lead ceramic gullwing, a 16-pin plastic DIP, and a 16-lead small outline plastic package. Military qualified versions of the AD9696 come in the TO-100 can and ceramic DIP; the dual AD9698 comes in ceramic DIP.

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ORDERING GUIDE

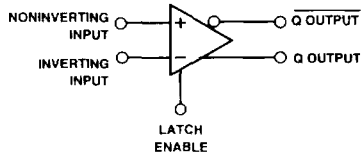
Model	Package	Temperature	Package Option[1]
AD9696KN	Plastic DIP	0°C to +70°C	N-8
AD9696KR	SOIC	0°C to +70°C	R-8
AD9696KQ	Cerdip	0°C to +70°C	Q-8
AD9696TQ/883B	Cerdip	-55°C to +125°C	Q-8
AD9696TZ/883B[2]	Gullwing	-55°C to +125°C	Z-8A
AD9698KN	Plastic DIP	0°C to +70°C	N-16
AD9698KR	SOIC	0°C to +70°C	R-16A
AD9698KQ	Cerdip	0°C to +70°C	Q-16
AD9698TQ/883B	Cerdip	-55°C to +125°C	Q-16
AD9698TZ/883B[3]	Gullwing	-55°C to +125°C	Z-16

NOTES
[1]N = Plastic DIP, Q = Cerdip, R = Small Outline (SOIC), Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]Refer to AD9696TZ/883B military data sheet.
[3]Refer to AD9698TZ/883B military data sheet.

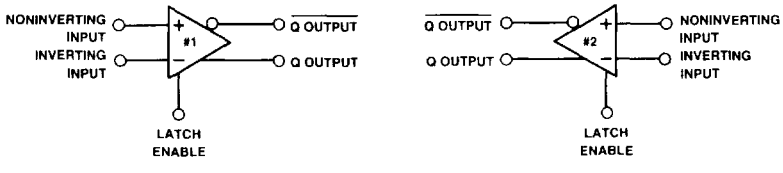
FUNCTIONAL BLOCK DIAGRAMS

AD9696/AD9698 Architecture

AD9696



AD9698



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AD9696/AD9698–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S/-V_S$) ..... +7 V/–7 V
Input Voltage Range ..... ±5 V
Differential Input Voltage ..... 5.4 V
Latch Enable Voltage ..... 0.5 V to $+V_S$
Output Current (Continuous) ..... 20 mA
Power Dissipation ..... 600 mW

Operating Temperature Range[2]
AD9696/AD9698KN/KQ/KR[3] ..... 0°C to +70°C
AD9696/AD9698TQ[3] ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature
KQ/TQ Suffixes ..... +175°C
KN/KR Suffixes ..... +150°C
Lead Soldering Temperature (10 sec) ..... +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = –5.2 V and +5.0 V; load as specified in Note 4, unless otherwise indicated)

Parameter	Temp	Test Level	0°C to +70°C AD9696/AD9698 KN/KQ/KR[3] Min	Typ	Max	–55°C to +125°C AD9696/AD9698 TQ[3] Min	Typ	Max	Units
INPUT CHARACTERISTICS									
Input Offset Voltage[5]	+25°C	I		1.0	2.0		1.0	2.0	mV
	Full	VI			3.0			3.0	mV
Input Offset Voltage Drift	Full	V		10			10		μV/°C
Input Bias Current	+25°C	I		16	55		16	55	μA
	Full	VI			110			110	μA
Input Offset Current	+25°C	I		0.4	1.0		0.4	1.0	μA
	Full	VI			1.3			1.3	μA
Input Capacitance	+25°C	V		3			3		pF
Input Voltage Range									
±5.0 V	Full	VI	2.2		+3.7	2.2		+3.7	V
±5.0 V	Full	VI	+1.4		+3.7	+1.4		+3.7	V
Common-Mode Rejection Ratio									
±5.0 V	Full	VI	80	85		80	85		dB
±5.0 V	Full	VI	57	63		57	63		dB
LATCH ENABLE INPUT									
Logic "1" Voltage Threshold	Full	VI	2.0			2.0			V
Logic "0" Voltage Threshold	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			10			10	μA
Logic "0" Current	Full	VI			1			1	μA
DIGITAL OUTPUTS									
Logic "1" Voltage (Source 4 mA)	Full	VI	2.7	3.5		2.7	3.5		V
Logic "0" Voltage (Sink 10 mA)	Full	VI		0.4	0.5		0.4	0.5	V
SWITCHING PERFORMANCE									
Propagation Delay (t_{PD})[9]									
Input to Output HIGH	Full	IV		4.5	7.0		4.5	7.0	ns
Input to Output LOW	Full	IV		4.5	7.0		4.5	7.0	ns
Latch Enable to Output HIGH	+25°C	IV		6.5	8.5		6.5	8.5	ns
Latch Enable to Output LOW	+25°C	IV		6.5	8.5		6.5	8.5	ns
Delta Delay Between Outputs	+25°C	IV		0.5	1.5		0.5	1.5	ns
Propagation Delay Dispersion									
20 mV to 100 mV Overdrive	+25°C	V		100			100		ps
100 mV to 1.0 V Overdrive	+25°C	IV		100	200		100	200	ps
Rise Time[11]	+25°C	V		1.85			1.85		ns
Fall Time[11]	+25°C	V		1.35			1.35		ns
Latch Enable									
Pulse Width [$t_{PW(H)}$]	+25°C	IV	3.5	2.5		3.5	2.5		ns
Setup Time (t_S)	+25°C	IV	3	1.7		3	1.7		ns
Hold Time (t_H)	+25°C	IV	3	1.9		3	1.9		ns

Specifications subject to change without notice.