PRELIMINARY

AMD

Am186™EM/EMLV and Am188™EM/EMLV

High Performance, 80C186-/80C188-Compatible and 80L186-/80L188-Compatible, 16-Bit Embedded Microcontrollers

DISTINCTIVE CHARACTERISTICS

- **E86™ family 80C186- and 80C188-compatible microcontrollers with enhanced bus interface**
  - — Lower system cost with higher performance
  - — 3.3-V ±.3-V operation (Am186EMLV and Am188EMLV microcontrollers)
- **High performance**
  - — 20-, 25-, 33-, and 40-MHz operating frequencies
  - — Supports zero-wait-state operation at 25 MHz with 110-ns static memory (Am186™EMLV and Am188™EMLV microcontrollers) and 40 MHz with 70-ns static memory (Am186™EM and Am188™EM microcontrollers)
  - — 1-Mbyte memory address space
  - — 64-Kbyte I/O space
- **New features provide faster access to memory and remove the requirement for a 2x clock input**
  - — Nonmultiplexed address bus
  - — Phase-locked loop (PLL) allows processor to operate at the clock input frequency
- **New integrated peripherals provide increased functionality while reducing system cost**
  - — Thirty-two programmable I/O (PIO) pins
  - — Asynchronous serial port allows full-duplex, 7-bit or 8-bit data transfers
  - — Synchronous serial interface allows half-duplex, bidirectional data transfer to and from ASICs
  - — Pseudo static RAM (PSRAM) controller includes auto refresh capability
  - — Reset configuration register
- **Familiar 80C186/80L186 peripherals**
  - — Two independent DMA channels
  - — Programmable interrupt controller with six external interrupts
  - — Three programmable 16-bit timers—timer 1 can be used as a watchdog interrupt timer
  - — Programmable memory and peripheral chip-select logic
  - — Programmable wait state generator
  - — Power-save clock divider
- **Software-compatible with the 80C186/80C188 and 80L186 /80L188 microcontrollers**
- **Widely available native development tools, applications, and system software**
- **Available in the following packages:**
  - — 100-pin, thin quad flat pack (TQFP)
  - — 100-pin, plastic quad flat pack (PQFP)

GENERAL DESCRIPTION

The Am186™EM/EMLV and Am188™EM/EMLV microcontrollers are the ideal upgrade for 80C186/188 and 80L186/188 microcontroller designs requiring 80C186/188 and 80L186/188 microcontroller compatibility, increased performance, serial communications, and a direct bus interface. The Am186EM/EMLV and Am188EM/EMLV microcontrollers increase the performance of existing 80C186/188 and 80L186/188 systems while decreasing their cost.

The Am186EM/EMLV and Am188EM/EMLV microcontrollers are part of the AMD E86 family of embedded microcontrollers and microprocessors based on the x86 architecture. The E86 family includes the 16- and 32-bit microcontrollers and microprocessors described on page 8

The Am186EM/EMLV and Am188EM/EMLV microcontrollers integrate the functions of the CPU, nonmultiplexed address bus, timers, chip selects, interrupt controller, DMA controller, PSRAM controller, asynchronous serial port, synchronous serial interface, and programmable I/O (PIO) pins on one chip. Compared to the 80C186/188 and 80L186/188 microcontrollers, the Am186EM/EMLV and Am188EM/EMLV microcontrollers enable designers to reduce the size, power consumption, and cost of embedded systems, while increasing functionality and performance.

The Am186EM/EMLV and Am188EM/EMLV microcontrollers have been designed to meet the most common requirements of embedded products developed for the office automation, mass storage, communications, and general embedded markets. Specific applications include disk drives, hand-held terminals and desktop terminals, fax machines, printers, photocopiers, feature phones, cellular phones, PBXs, multiplexers, modems, and industrial controls.

This document contains information on a product under development at Advanced Micro Devices. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

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$\overline{RD}$

Read Strobe (output, synchronous, three-state)

This pin indicates to the system that the microcontroller is performing a memory or I/O read cycle. $\overline{RD}$ is guaranteed not to be asserted before the address and data bus is floated during the address-to-data transition. $\overline{RD}$ floats during a bus hold condition.

$\overline{RES}$

Reset (input, asynchronous, level-sensitive)

This pin requires the microcontroller to perform a reset. When $\overline{RES}$ is asserted, the microcontroller immediately terminates its present activity, clears its internal logic, and CPU control is transferred to the reset address FFFF0h.

$\overline{RES}$ must be held Low for at least 1 ms.

$\overline{RES}$ can be asserted asynchronously to CLKOUTA because $\overline{RES}$ is synchronized internally. For proper initialization, V_{CC} must be within specifications, and CLKOUTA must be stable for more than four CLKOUTA periods during which $\overline{RES}$ is asserted.

The microcontroller begins fetching instructions approximately 6.5 CLKOUTA periods after $\overline{RES}$ is deasserted. This input is provided with a Schmitt trigger to facilitate power-on $\overline{RES}$ generation via an RC network.

$\overline{RFSH2}/\overline{ADEN}$ (Am188EM Microcontroller Only)

Refresh 2 (three-state, output, synchronous)
Address Enable (input, internal pullup)

$\overline{RFSH2}$—Asserted Low to signify a DRAM refresh bus cycle. The use of $\overline{RFSH2}/\overline{ADEN}$ to signal a refresh is not valid when PSRAM mode is selected. Instead, the $\overline{MCS3}/\overline{RFSH}$ signal is provided to the PSRAM.

$\overline{ADEN}$—If $\overline{RFSH2}/\overline{ADEN}$ is held High or left floating on power-on reset, the AD bus (AO15–AO8 and AD7–AD0) is enabled or disabled during the address portion of LCS and UCS bus cycles based on the DA bit in the LMCS and UMCS registers. If the DA bit is set, the memory address is accessed on the A19–A0 pins. This mode of operation reduces power consumption. For more information, see the “Bus Operation” section on page 37. There is a weak internal pullup resistor on $\overline{RFSH2}/\overline{ADEN}$ so no external pullup is required.

If $\overline{RFSH2}/\overline{ADEN}$ is held Low on power-on reset, the AD bus drives both addresses and data regardless of the DA bit setting. The pin is sampled one crystal clock cycle after the rising edge of $\overline{RES}$. $\overline{RFSH2}/\overline{ADEN}$ is three-stated during bus holds and ONCE mode.

RXD/PIO28

Receive Data (input, asynchronous)

This pin supplies asynchronous serial receive data from the system to the internal UART of the microcontroller.

$\overline{S2}$–$\overline{S0}$

Bus Cycle Status (output, three-state, synchronous)

These pins indicate to the system the type of bus cycle in progress. $\overline{S2}$ can be used as a logical memory or I/O indicator, and $\overline{S1}$ can be used as a data transmit or receive indicator. $\overline{S2}$–$\overline{S0}$ float during bus hold and hold acknowledge conditions. The $\overline{S2}$–$\overline{S0}$ pins are encoded as shown in Table 4.

Table 4. Bus Cycle Encoding

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	Read data from I/O
0	1	0	Write data to I/O
0	1	1	Halt
1	0	0	Instruction fetch
1	0	1	Read data from memory
1	1	0	Write data to memory
1	1	1	None (passive)

S6/$\overline{CLKDIV2}$/PIO29

Bus Cycle Status Bit 6 (output, synchronous)
Clock Divide by 2 (input, internal pullup)

S6—During the second and remaining periods of a cycle (t_2, t_3, and t_4), this pin is asserted High to indicate a DMA-initiated bus cycle. During a bus hold or reset condition, S6 floats.

$\overline{CLKDIV2}$—If S6/$\overline{CLKDIV2}$/PIO29 is held Low during power-on reset, the chip enters clock divided by 2 mode where the processor clock is derived by dividing the external clock input by 2. If this mode is selected, the PLL is disabled. The pin is sampled on the rising edge of $\overline{RES}$.

If S6 is to be used as PIO29 in input mode, the device driving PIO29 must not drive the pin Low during power-on reset. S6/$\overline{CLKDIV2}$/PIO29 defaults to a PIO input with pullup, so the pin does not need to be driven High externally.

SCLK/PIO20

Serial Clock (output, synchronous)

This pin supplies the synchronous serial interface (SSI) clock to a slave device, allowing transmit and receive operations to be synchronized between the microcontroller and the slave. SCLK is derived from the microcontroller internal clock and then divided by 2, 4, 8, or 16 depending on register settings.

An access to any of the SSR or SSD registers activates SCLK for eight SCLK cycles (see Figure 11 and Figure 12 on page 49). When SCLK is inactive, it is held High by the microcontroller.

SDATA/PIO21

Serial Data (input/output, synchronous)

This pin transmits synchronous serial interface (SSI) data to and from a slave device. When SDATA is inactive, a weak keeper holds the last value of SDATA on the pin.

SDEN1/PIO23, SDEN0/PIO22

Serial Data Enables (output, synchronous)

These pins enable data transfers on port 1 and port 0 of the synchronous serial interface (SSI). The microcontroller asserts either SDEN1 or SDEN0 at the beginning of a transfer and deasserts it after the transfer is complete. When SDEN1–SDEN0 are inactive, they are held Low by the microcontroller.

SRDY/PIO6

Synchronous Ready (input, synchronous, level-sensitive)

This pin indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active High input synchronized to CLKOUTA.

Using SRDY instead of ARDY allows a relaxed system timing because of the elimination of the one-half clock period required to internally synchronize ARDY. To always assert the ready condition to the microcontroller, tie SRDY High. If the system does not use SRDY, tie the pin Low to yield control to ARDY.

TMRIN0/PIO11

Timer Input 0 (input, synchronous, edge-sensitive)

This pin supplies a clock or control signal to the internal microcontroller timer 0. After internally synchronizing a Low-to-High transition on TMRIN0, the microcontroller increments the timer. TMRIN0 must be tied High if not being used.

TMRIN1/PIO0

Timer Input 1 (input, synchronous, edge-sensitive)

This pin supplies a clock or control signal to the internal microcontroller timer 1. After internally synchronizing a Low-to-High transition on TMRIN1, the microcontroller increments the timer. TMRIN1 must be tied High if not being used.

TMROUT0/PIO10

Timer Output 0 (output, synchronous)

This pin supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle. TMROUT0 is floated during a bus hold or reset.

TMROUT1/PIO1

Timer Output 1 (output, synchronous)

This pin supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle. TMROUT1 can also be programmed as a watchdog timer. TMROUT1 is floated during a bus hold or reset.

TXD/PIO27

Transmit Data (output, asynchronous)

This pin supplies asynchronous serial transmit data to the system from the internal UART of the microcontroller.

$\overline{\text{UCS}}$/$\overline{\text{ONCE}}$1

Upper Memory Chip Select (output, synchronous) ONCE Mode Request 1 (input, internal pullup)

$\overline{\text{UCS}}$—This pin indicates to the system that a memory access is in progress to the upper memory block. The base address and size of the upper memory block are programmable up to 512 Kbytes. $\overline{\text{UCS}}$ is held High during a bus hold condition.

After power-on reset, $\overline{\text{UCS}}$ is asserted because the processor begins executing at FFFF0h and the default configuration for the $\overline{\text{UCS}}$ chip select is 64 Kbytes from F0000h to FFFFFh.

$\overline{\text{ONCE}}$1—During reset, this pin and $\overline{\text{ONCE}}$0 indicate to the microcontroller the mode in which it should operate. $\overline{\text{ONCE}}$0 and $\overline{\text{ONCE}}$1 are sampled on the rising edge of $\overline{\text{RES}}$. If both pins are asserted Low, the microcontroller enters ONCE mode. Otherwise, it operates normally. In ONCE mode, all pins assume a high-impedance state and remain in that state until a subsequent reset occurs. To guarantee that the microcontroller does not inadvertently enter ONCE mode, $\overline{\text{ONCE}}$1 has a weak internal pullup resistor that is active only during a reset. This pin is not three-stated during a bus hold condition.

$\overline{UZI}$/PIO26

Upper Zero Indicate (output, synchronous)

$\overline{UZI}$—This pin lets the designer determine if an access to the interrupt vector table is in progress by ORing it with bits 15–10 of the address and data bus (AD15–AD10 on the 186 and AO15–AO10 on the 188). $\overline{UZI}$ is the logical OR of the inverted A19–A16 bits, and it asserts in the first period of a bus cycle and is held throughout the cycle.

This signal should be pulled High or allowed to float at reset. If this pin is Low at the negation of reset, the Am186EM and Am188EM microcontrollers will enter a reserved clock test mode.

V_{CC}

Power Supply (input)

These pins supply power (+5 V) to the microcontroller.

$\overline{WHB}$ (Am186EM Microcontroller Only)

Write High Byte (output, three-state, synchronous)

This pin and $\overline{WLB}$ indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 designs, this information is provided by $\overline{BHE}$, AD0, and $\overline{WR}$. However, by using $\overline{WHB}$ and $\overline{WLB}$, the standard system interface logic and external address latch that were required are eliminated.

$\overline{WHB}$ is asserted with AD15–AD8. $\overline{WHB}$ is the logical OR of $\overline{BHE}$ and $\overline{WR}$. This pin floats during reset.

$\overline{WLB}$ (Am186EM Microcontroller Only)
$\overline{WB}$ (Am188EM Microcontroller Only)

Write Low Byte (output, three-state, synchronous)
Write Byte (output, three-state, synchronous)

$\overline{WLB}$—This pin and $\overline{WHB}$ indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 designs, this information is provided by $\overline{BHE}$, AD0, and $\overline{WR}$. However, by using $\overline{WHB}$ and $\overline{WLB}$, the standard system interface logic and external address latch that were required are eliminated.

$\overline{WLB}$ is asserted with AD7–AD0. $\overline{WLB}$ is the logical OR of AD0 and $\overline{WR}$. This pin floats during reset.

$\overline{WB}$—On the Am188EM microcontroller, this pin indicates a write to the bus. $\overline{WB}$ uses the same early timing as the nonmultiplexed address bus. $\overline{WB}$ is associated with AD7–AD0. This pin floats during reset.

$\overline{WR}$

Write Strobe (output, synchronous)

This pin indicates to the system that the data on the bus is to be written to a memory or I/O device. $\overline{WR}$ floats during a bus hold or reset condition.

X1

Crystal Input (input)

This pin and the X2 pin provide connections for a fundamental mode or third-overtone parallel-resonant crystal used by the internal oscillator circuit. To provide the microcontroller with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.

X2

Crystal Output (output)

This pin and the X1 pin provide connections for a fundamental mode or third-overtone parallel-resonant crystal used by the internal oscillator circuit. To provide the microcontroller with an external clock source, leave the X2 pin unconnected and connect the source to the X1 pin.

FUNCTIONAL DESCRIPTION

AMD's Am186 and Am188 family of microcontrollers and microprocessors is based on the architecture of the original 8086 and 8088 microcontrollers and currently includes the 80C186, 80C188, 80L186, 80L188, Am186EM, Am188EM, Am186EMLV, Am188EMLV, Am186ES, Am188ES, Am186ESLV, Am188ESLV, Am186ER, and Am188ER microcontrollers.

All family members contain the same basic set of registers, instructions, and addressing modes and are compatible with the industry-standard 80C186/188 microcontrollers.

A full description of all the Am186EM and Am188EM microcontroller registers is included in the *Am186EM and Am188EM Microcontrollers User's Manual*, order# 19713. The instruction set for the Am186EM and Am188EM microcontrollers is documented in the *Am186 and Am188 Family Instruction Set Manual*, order# 21267.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address that consists of a 16-bit segment value and a 16-bit offset. The 16-bit segment values are contained in one of four internal segment registers (CS, DS, SS, or ES). The physical address is calculated by shifting the segment value left by 4 bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 3). This allows for a 1-Mbyte physical address size.

All instructions that address operands in memory must specify the segment value and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 5).

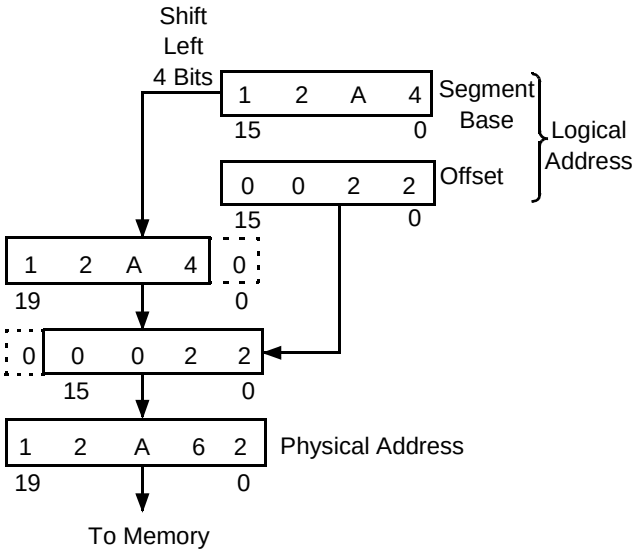


Figure 2. Two-Component Address

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions (IN, INS and OUT, OUTS) address the I/O space with either an 8-bit port address specified in the instruction, or a 16-bit port address in the DX register. Eight-bit port addresses are zero-extended so that A15–A8 are Low. I/O port addresses 00F8h through 00FFh are reserved. The Am186EM and Am188EM microcontrollers provide specific instructions for addressing I/O space.

Table 5. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instructions (including immediate data)
Local Data	Data (DS)	All data references
Stack	Stack (SS)	All stack pushes and pops; any memory references that use BP Register
External Data (Global)	Extra (ES)	All string instruction references that use the DI Register as an index

BUS OPERATION

The industry-standard 80C186 and 80C188 microcontrollers use a multiplexed address and data (AD) bus. The address is present on the AD bus only during the t_1 clock phase. The Am186EM and Am188EM microcontrollers continue to provide the multiplexed AD bus and, in addition, provide a nonmultiplexed address (A) bus. The A bus provides an address to the system for the complete bus cycle (t_1–t_4).

For systems where power consumption is a concern, it is possible to disable the address from being driven on the AD bus on the Am186EM microcontroller and on the AD and AO buses on the Am188EM microcontroller during the normal address portion of the bus cycle for accesses to UCS and/or LCS address spaces. In this mode, the affected bus is placed in a high impedance state during the address portion of the bus cycle. This feature is enabled through the DA bits in the UMCS and LMCS registers. When address disable is in effect, the number of signals that assert on the bus during all normal bus cycles to the associated address space is reduced, decreasing power consumption and reducing processor switching noise. On the Am188EM microcontroller, the address is driven on A015–A08 during the data portion of the bus cycle, regardless of the setting of the DA bits.

If the $\overline{\text{ADEN}}$ pin is pulled Low during processor reset, the value of the DA bits in the UMCS and LMCS registers is ignored and the address is driven on the AD bus for all accesses, thus preserving the industry-standard 80C186 and 80C188 microcontrollers' multiplexed address bus and providing support for existing emulation tools.

The following diagrams show the Am186EM and Am188EM microcontroller bus cycles when the address bus disable feature is in effect.

Figure 3 shows the affected signals during a normal read or write operation for an Am186EM microcontroller. The address and data will be multiplexed onto the AD bus.

Figure 4 shows an Am186EM microcontroller bus cycle when address bus disable is in effect. This results in having the AD bus operate in a nonmultiplexed address/data mode. The A bus will have the address during a read or write operation.

Figure 5 shows the affected signals during a normal read or write operation for an Am188EM microcontroller. The multiplexed address/data mode is compatible with the 80C186 and 80C188 microcontrollers and might be used to take advantage of existing logic or peripherals.

Figure 6 shows an Am188EM microcontroller bus cycle when address bus disable is in effect. The address and data is not multiplexed. The AD7–AD0 signals will have only data on the bus, while the AO bus will have the address during a read or write operation.

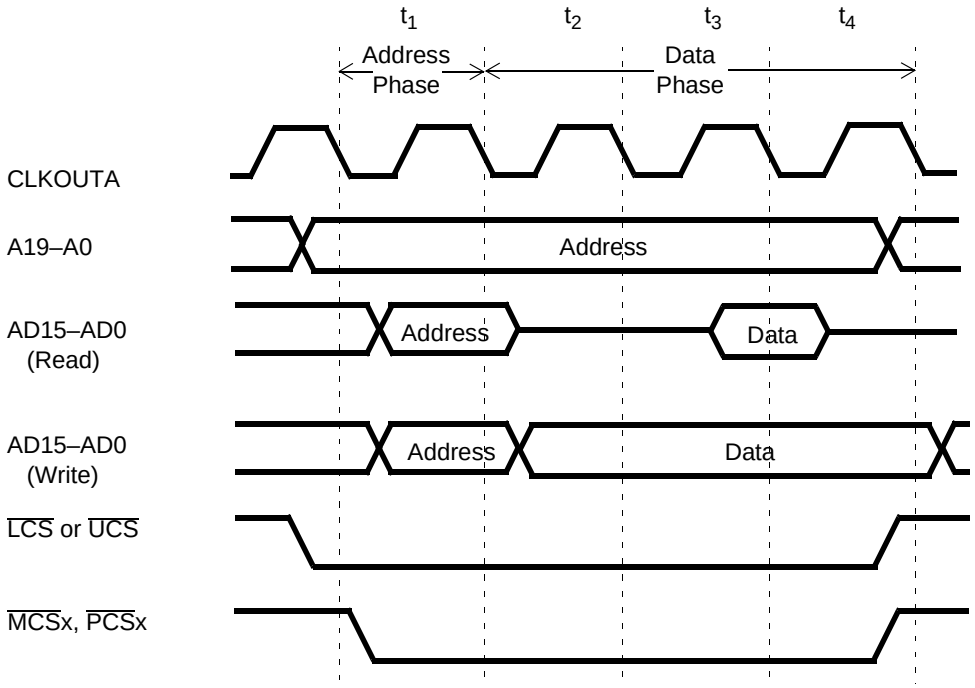


Figure 3. Am186EM Microcontroller Address Bus—Normal Read and Write Operation

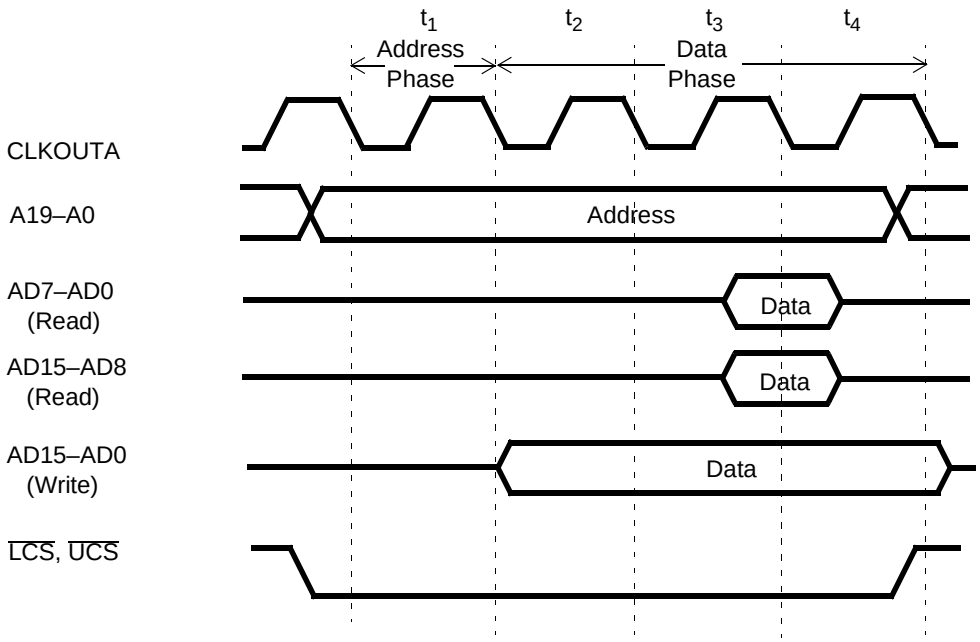


Figure 4. Am186EM Microcontroller—Read and Write with Address Bus Disable In Effect

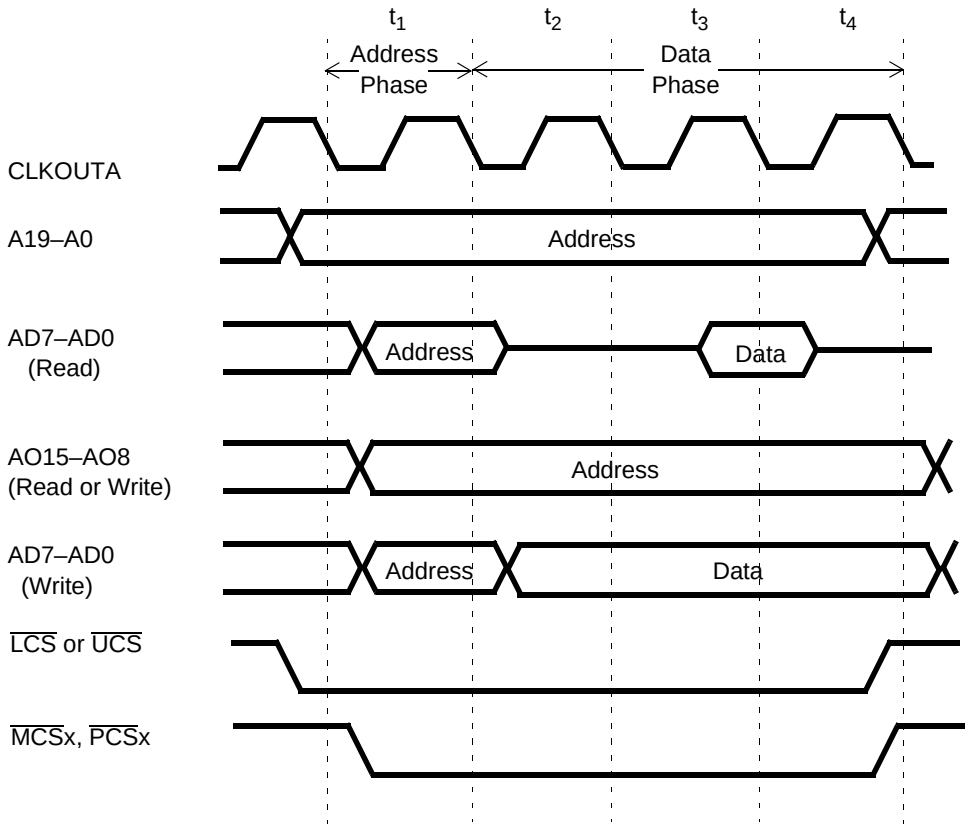


Figure 5. Am188EM Microcontroller Address Bus—Normal Read and Write Operation

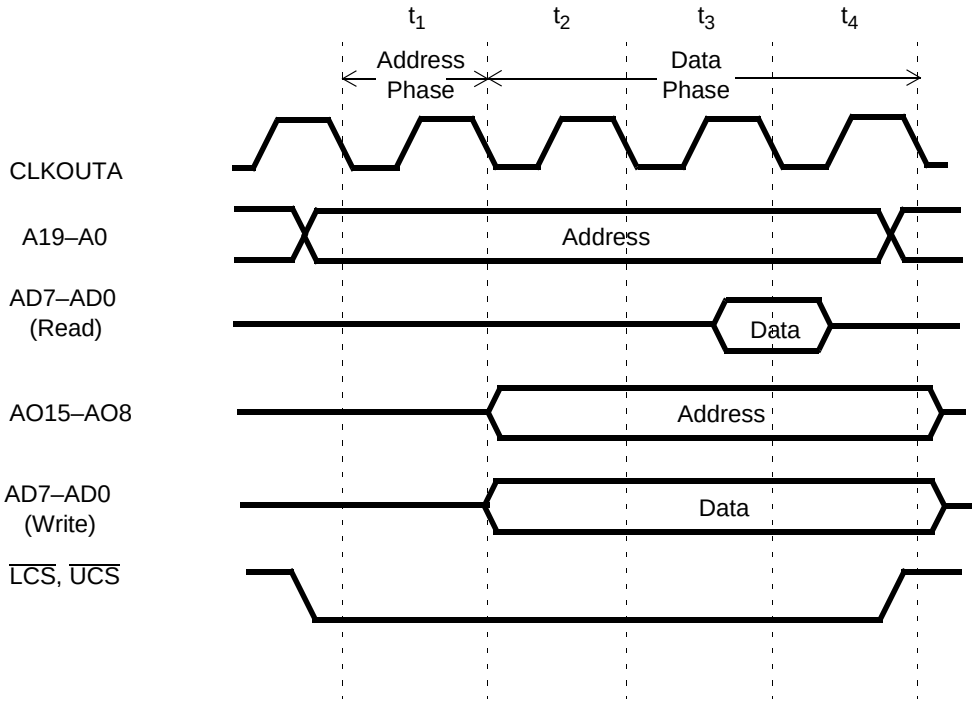


Figure 6. Am188EM Microcontroller—Read and Write with Address Bus Disable In Effect

BUS INTERFACE UNIT

The bus interface unit controls all accesses to external peripherals and memory devices. External accesses include those to memory devices, as well as those to memory-mapped and I/O-mapped peripherals and the peripheral control block. The Am186EM and Am188EM microcontrollers provide an enhanced bus interface unit with the following features:

- A nonmultiplexed address bus
- Separate byte write enables for high and low bytes in the Am186EM microcontroller only
- Pseudo Static RAM (PSRAM) support

The standard 80C186/188 multiplexed address and data bus requires system interface logic and an external address latch. On the Am186EM and Am188EM microcontrollers, new byte write enables, PSRAM control logic, and a new nonmultiplexed address bus can reduce design costs by eliminating this external logic.

Nonmultiplexed Address Bus

The nonmultiplexed address bus (A19–A0) is valid one-half CLKOUTA cycle in advance of the address on the AD bus. When used in conjunction with the modified $\overline{UCS}$ and $\overline{LCS}$ outputs and the byte write enable signals, the A19–A0 bus provides a seamless interface to SRAM, PSRAM, and Flash/EPROM memory systems.

Byte Write Enables

The Am186EM microcontroller provides the $\overline{WHB}$ (Write High Byte) and $\overline{WLB}$ (Write Low Byte) signals, which act as byte write enables.

$\overline{WHB}$ is the logical OR of $\overline{BHE}$ and $\overline{WR}$. $\overline{WHB}$ is Low when $\overline{BHE}$ and $\overline{WR}$ are both Low. $\overline{WLB}$ is the logical OR of AD0 and $\overline{WR}$. $\overline{WLB}$ is Low when AD0 and $\overline{WR}$ are both Low. $\overline{WB}$ is Low whenever a byte is written on the Am188EM microcontroller.

The byte write enables are driven in conjunction with the nonmultiplexed address bus as required for the write timing requirements of common SRAMs.

Pseudo Static RAM (PSRAM) Support

The Am186EM and Am188EM microcontrollers support the use of PSRAM devices in low memory chip-select (LCS) space only. When PSRAM mode is enabled, the timing for the $\overline{LCS}$ signal is modified by the chip-select control unit to provide a $\overline{CS}$ precharge period during PSRAM accesses. The 40-MHz timing of the Am186EM and Am188EM microcontrollers is appropriate to allow 70-ns PSRAM to run with one wait state. PSRAM mode is enabled through a bit in the Low Memory Chip-Select (LMCS) Register. The PSRAM feature is disabled on CPU reset.

In addition to the $\overline{LCS}$ timing changes for PSRAM precharge, the PSRAM devices also require periodic refresh of all internal row addresses to retain their data. Although refresh of PSRAM can be accomplished several ways, the Am186EM and Am188EM microcontrollers implement auto refresh only.

The Am186EM and Am188EM microcontrollers generate $\overline{RFSH}$, a refresh signal, to the PSRAM devices when PSRAM mode is enabled. No refresh address is required by the PSRAM when using the auto refresh mechanism. The $\overline{RFSH}$ signal is multiplexed with the $\overline{MCS}$3 signal pin. When PSRAM mode is enabled, $\overline{MCS}$3 is not available for use as a chip-select signal.

The refresh control unit must be programmed before accessing PSRAM in LCS space. The refresh counter in the Clock Prescaler (CDRAM) Register must be configured with the required refresh interval value. The ending address of LCS space and the ready and wait-state generation in the LMCS Register must also be programmed. The refresh counter reload value in the CDRAM Register should not be set to less than 18 (12h) in order to provide time for processor cycles within refresh. The refresh address counter must be set to 000000h to prevent another chip select from asserting.

$\overline{LCS}$ is held High during a refresh cycle. The A bus is not used during refresh cycles. The LMCS Register must be configured to external ready ignored (R2=1) with one wait state (R1–R0=01b), and the PSRAM mode enable bit (SE) must be set.

PERIPHERAL CONTROL BLOCK (PCB)

The integrated peripherals of the Am186EM and Am188EM microcontrollers are controlled by 16-bit read/write registers. The peripheral registers are contained within an internal 256-byte control block. The registers are physically located in the peripheral devices they control, but they are addressed as a single 256-byte block. Figure 7 shows a map of these registers.

Reading and Writing the PCB

Code that is intended to execute on the Am188EM microcontroller should perform all writes to the PCB registers as byte writes. These writes will transfer 16 bits of data to the PCB register even if an 8-bit register is named in the instruction. For example, `out dx, al` results in the value of `ax` being written to the port address in `dx`. Reads to the PCB should be done as word reads. Code written in this manner will run correctly on the Am188EM microcontroller and on the Am186EM microcontroller.

Unaligned reads and writes to the PCB result in unpredictable behavior on both the Am186EM and Am188EM microcontrollers.

For a complete description of all the registers in the PCB, see the *Am186EM and Am188EM Microcontrollers User's Manual*, order# 19713.

Offset (Hexadecimal)	Register Name
FE	Peripheral Control Block Relocation Register
F6	Reset Configuration Register
F4	Processor Release Level Register
F0	PDCON Register
E4	Enable RCU Register
E2	Clock Prescaler Register
E0	Memory Partition Register
DA	DMA 1 Control Register
D8	DMA 1 Transfer Count Register
D6	DMA 1 Destination Address High Register
D4	DMA 1 Destination Address Low Register
D2	DMA 1 Source Address High Register
D0	DMA 1 Source Address Low Register
CA	DMA 0 Control Register
C8	DMA 0 Transfer Count Register
C6	DMA 0 Destination Address High Register
C4	DMA 0 Destination Address Low Register
C2	DMA 0 Source Address High Register
C0	DMA 0 Source Address Low Register
A8	$\overline{PCS}$ and $\overline{MCS}$ Auxiliary Register
A6	Midrange Memory Chip Select Register
A4	Peripheral Chip Select Register
A2	Low Memory Chip Select Register
A0	Upper Memory Chip Select Register
88	Serial Port Baud Rate Divisor Register
86	Serial Port Receive Register
84	Serial Port Transmit Register
82	Serial Port Status Register
80	Serial Port Control Register

Changed from 80C186 microcontroller.

***Note**: Gaps in offset addresses indicate reserved registers.*

Figure 7. Peripheral Control Block Register Map

Offset (Hexadecimal)	Register Name
7A	PIO Data 1 Register
78	PIO Direction 1 Register
76	PIO Mode 1 Register
74	PIO Data 0 Register
72	PIO Direction 0 Register
70	PIO Mode 0 Register
66	Timer 2 Mode/Control Register
62	Timer 2 Maxcount Compare A Register
60	Timer 2 Count Register
5E	Timer 1 Mode/Control Register
5C	Timer 1 Maxcount Compare B Register
5A	Timer 1 Maxcount Compare A Register
58	Timer 1 Count Register
56	Timer 0 Mode/Control Register
54	Timer 0 Maxcount Compare B Register
52	Timer 0 Maxcount Compare A Register
50	Timer 0 Count Register
44	Serial Port Interrupt Control Register
42	Watchdog Timer Control Register
40	INT4 Control Register
3E	INT3 Control Register
3C	INT2 Control Register
3A	INT1 Control Register
38	INT0 Control Register
36	DMA 1 Interrupt Control Register
34	DMA 0 Interrupt Control Register
32	Timer Interrupt Control Register
30	Interrupt Status Register
2E	Interrupt Request Register
2C	In-service Register
2A	Priority Mask Register
28	Interrupt Mask Register
26	Poll Status Register
24	Poll Register
22	End-of-Interrupt Register
20	Interrupt Vector Register
18	Synchronous Serial Receive Register
16	Synchronous Serial Transmit 0 Register
14	Synchronous Serial Transmit 1 Register
12	Synchronous Serial Enable Register
10	Synchronous Serial Status Register

Changed from 80C186 microcontroller.

***Note**: Gaps in offset addresses indicate reserved registers.*

Figure 7. Peripheral Control Block Register Map (continued)

CLOCK AND POWER MANAGEMENT

The clock and power management unit of the Am186EM and Am188EM microcontrollers includes a phase-locked loop (PLL) and a second programmable system clock output (CLKOUTB).

Phase-Locked Loop (PLL)

In a traditional 80C186/188 design, the crystal frequency is twice that of the desired internal clock. Because of the internal PLL on the Am186EM and Am188EM microcontrollers, the internal clock generated by the Am186EM and Am188EM microcontrollers (CLKOUTA) is the same frequency as the crystal. The PLL takes the crystal inputs (X1 and X2) and generates a 45/55% (worst case) duty cycle intermediate system clock of the same frequency. This removes the need for an external 2x oscillator, reducing system cost. The PLL is reset by an on-chip power-on reset (POR) circuit.

Crystal-Driven Clock Source

The internal oscillator circuit of the Am186EM and Am188EM microcontrollers is designed to function with a parallel-resonant fundamental or third-overtone crystal. Because of the PLL, the crystal frequency should be equal to the processor frequency. Do not replace a crystal with an LC or RC equivalent.

The signals X1 and X2 are connected to an internal inverting amplifier (oscillator) which provides, along with the external feedback loading, the necessary phase shift (Figure 8). In such a positive feedback circuit, the inverting amplifier has an output signal (X2) 180 degrees out of phase of the input signal (X1).

The external feedback network provides an additional 180-degree phase shift. In an ideal system, the input to X1 will have 360 or zero degrees of phase shift. The external feedback network is designed to be as close to ideal as possible. If the feedback network is not providing necessary phase shift, negative feedback will dampen the output of the amplifier and negatively affect the operation of the clock generator. Values for the loading on X1 and X2 must be chosen to provide the necessary phase shift and crystal operation.

Selecting a Crystal

When selecting a crystal, the load capacitance should always be specified (C_L). This value can cause variance in the oscillation frequency from the desired specified value (resonance). The load capacitance and the loading of the feedback network have the following relationship:

$$C_L = \frac{(C_1 \cdot C_2)}{(C_1 + C_2)} + C_S$$

where C_S is the stray capacitance of the circuit. Placing the crystal and C_L in series across the inverting amplifier and tuning these values (C_1, C_2) allows the crystal to oscillate at resonance. This relationship is true for both fundamental and third-overtone operation. Finally, there is a relationship between C_1 and C_2. To enhance the oscillation of the inverting amplifier, these values need to be offset with the larger load on the output (X2). Equal values of these loads will tend to balance the poles of the inverting amplifier.

The characteristics of the inverting amplifier set limits on the following parameters for crystals:

ESR (Equivalent Series Resistance)..... 80 ohm max

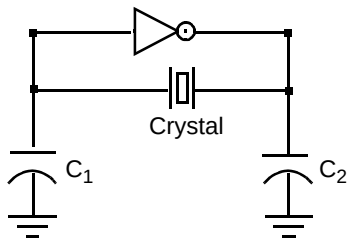
Drive Level.....1 mW max

The recommended range of values for C_1 and C_2 are as follows:

C_1.....15 pF ± 20%

C_2.....22 pF ± 20%

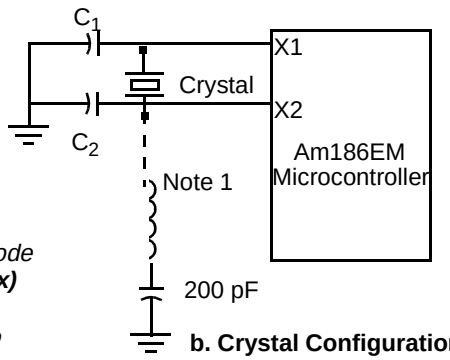
The specific values for C_1 and C_2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.



a. Inverting Amplifier Configuration

***Note 1**: Use for Third Overtone Mode*

XTAL Frequency	***L1 Value (Max)***
20 MHz	*12 µH ±20%*
25 MHz	*8.2 µH ±20%*
33 MHz	*4.7 µH ±20%*
40 MHz	*3.0 µH ±20%*



b. Crystal Configuration

Figure 8. Am186EM and Am188EM Microcontrollers Oscillator Configurations

External Source Clock

Alternately, the internal oscillator can be driven from an external clock source. This source should be connected to the input of the inverting amplifier (X1), with the output (X2) not connected.

System Clocks

The base system clock of the 80C186 and 80C188 microcontrollers is renamed CLKOUTA and the additional output is called CLKOUTB. CLKOUTA and CLKOUTB operate at either the processor frequency or the crystal input frequency. The output drivers for both clocks are individually programmable for disable. Figure 9 shows the organization of the clocks.

The second clock output (CLKOUTB) allows one clock to run at the crystal input frequency and the other clock to run at the power-save frequency. Individual drive enable bits allow selective enabling of just one or both of these clock outputs.

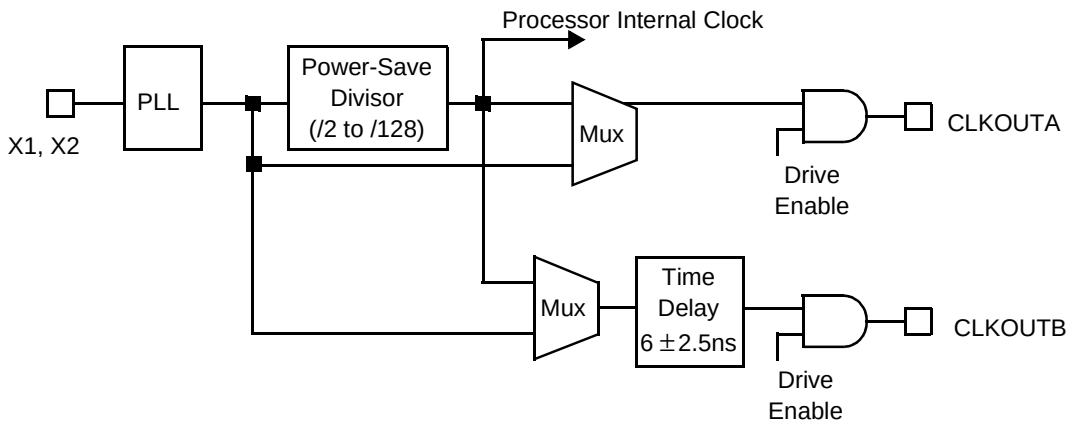


Figure 9. Clock Organization

Power-Save Operation

The power-save mode of the Am186EM and Am188EM microcontrollers reduces power consumption and heat dissipation, thereby extending battery life in portable systems. In power-save mode, operation of the CPU and internal peripherals continues at a slower clock frequency. When an interrupt occurs, the microcontroller automatically returns to its normal operating frequency on the internal clock's next rising edge of t_3. In order for an interrupt to be recognized, it must be valid before the internal clock's rising edge of t_3.

Note: *Power-save operation requires that clock-dependent devices be reprogrammed for clock frequency changes. Software drivers must be aware of clock frequency.*

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{RES}$ input pin Low. $\overline{RES}$ must be held Low for 1 ms during power-up to ensure proper device initialization. $\overline{RES}$ forces the Am186EM and Am188EM microcontrollers to terminate all execution and local bus activity. No instruction or bus activity occurs as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the microcontroller begins execution with the instruction at physical location FFFF0h. $\overline{RES}$ also sets some registers to predefined values.

The Reset Configuration Register

When the $\overline{RES}$ input is asserted Low, the contents of the address/data bus (AD15–AD0) are written into the Reset Configuration register. The system can place configuration information on the address/data bus using weak external pullup or pulldown resistors, or using an external driver that is enabled during reset. The processor does not drive the address/data bus during reset.

For example, the Reset Configuration register could be used to provide the software with the position of a configuration switch in the system. Using weak external pullup and pulldown resistors on the address and data bus, the system would provide the microcontroller with a value corresponding to the position of the jumper during a reset.

CHIP-SELECT UNIT

The Am186EM and Am188EM microcontrollers contain logic that provides programmable chip-select generation for both memories and peripherals. The logic can be programmed to provide ready and wait-state generation and latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they are generated by the CPU or by the integrated DMA unit.

The Am186EM and Am188EM microcontrollers provide six chip-select outputs for use with memory devices and six more for use with peripherals in either memory space or I/O space. The six chip selects for memory devices can be used to address three memory ranges. Each of the six peripheral chip selects addresses a 256-byte block that is offset from a programmable base address. A read or write access to the corresponding chip select register activates the chip selects.

Chip-Select Timing

The timing for the $\overline{UCS}$ and $\overline{LCS}$ outputs is modified from the original 80C186 microcontroller. These outputs now assert in conjunction with the nonmultiplexed address bus for normal memory timing. To allow these outputs to be available earlier in the bus cycle, the number of programmable memory size selections has been reduced.

Ready and Wait-State Programming

The Am186EM and Am188EM microcontrollers can be programmed to sense a ready signal for each of the peripheral or memory chip-select lines. The ready signal can be either the ARDY or SRDY signal. Each chip-select control register (UMCS, LMCS, MMCS, PACS, and MPCS) contains a single-bit field that determines whether the external ready signal is required or ignored.

The number of wait states to be inserted for each access to a peripheral or memory region is programmable. The chip-select control registers for $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS}$3–$\overline{MCS}$0, $\overline{PCS}$6, and $\overline{PCS}$5 contain a two-bit field that determines the number of wait states from zero to three to be inserted. $\overline{PCS}$3–$\overline{PCS}$0 use three bits to provide additional values of 5, 7, 9, and 15 wait states.

When external ready is required, internally programmed wait states will always complete before external ready can terminate or extend a bus cycle. For example, if the internal wait states are set to insert two wait states, the processor samples the external ready pin during the first wait cycle. If external ready is asserted at that time, the access completes after six cycles (four cycles plus two wait states). If external ready is not asserted during the first wait state, the access is extended until ready is asserted, which is followed by one more wait state followed by t_4.

Chip-Select Overlap

Although programming the various chip selects on the Am186EM and Am188EM microcontrollers so that multiple chip select signals are asserted for the same physical address is not recommended, it may be unavoidable in some systems. In such systems, the chip selects whose assertions overlap must have the same configuration for ready (external ready required or not required) and the number of wait states to be inserted into the cycle by the processor.

The peripheral control block (PCB) is accessed using internal signals. These internal signals function as chip selects configured with zero wait states and no external ready. Therefore, the PCB can be programmed to addresses that overlap external chip select signals if those external chip selects are programmed to zero wait states with no external ready required.

When overlapping an additional chip select with either the $\overline{LCS}$ or $\overline{UCS}$ chip selects, it must be noted that setting the Disable Address (DA) bit in the LMCS or UMCS register will disable the address from being driven on the AD bus for all accesses for which the associated chip select is asserted, including any accesses for which multiple chip selects assert.

The $\overline{MCS}$ and $\overline{PCS}$ chip select pins can be configured as either chip selects (normal function) or as PIO inputs or outputs. It should be noted; however, that the ready and wait state generation logic for these chip selects is in effect regardless of their configurations as chip selects or PIOs. This means that if these chip selects are enabled (by a read or write to the MMCS and MPCS for the $\overline{MCS}$ chip selects, or by a read or write to the PACS and MPCS registers for the $\overline{PCS}$ chip selects), the ready and wait state programming for these signals must agree with the programming for any other chip selects with which their assertion would overlap if they were configured as chip selects.

Although the $\overline{PCS}$4 signal is not available on an external pin, the ready and wait state logic for this signal still exists internal to the part. For this reason, the $\overline{PCS}$4 address space must follow the rules for overlapping chip selects. The ready and wait-state logic for $\overline{PCS}$6–$\overline{PCS}$5 is disabled when these signals are configured as address bits A2–A1.

Failure to configure overlapping chip selects with the same ready and wait state requirements may cause the processor to hang with the appearance of waiting for a ready signal. This behavior may occur even in a system in which ready is always asserted (ARDY or SRDY tied High).

Configuring $\overline{PCS}$ in I/O space with $\overline{LCS}$ or any other chip select configured for memory address 0 is not considered overlapping of the chip selects. Overlapping chip selects refers to configurations where more than one chip select asserts for the same physical address.

Upper Memory Chip Select

The Am186EM and Am188EM microcontrollers provide a $\overline{UCS}$ chip select for the top of memory. On reset, the Am186EM and Am188EM microcontrollers begin fetching and executing instructions starting at memory location FFFF0h. Therefore, upper memory is usually used as instruction memory. To facilitate this usage, $\overline{UCS}$ defaults to active on reset, with a default memory range of 64 Kbytes from F0000h to FFFFFh, with external ready required and three wait states automatically inserted. The $\overline{UCS}$ memory range always ends at FFFFFh. The lower boundary is programmable.

Low Memory Chip Select

The Am186EM and Am188EM microcontrollers provide an $\overline{LCS}$ chip select for the bottom of memory. Since the interrupt vector table is located at the bottom of memory starting at 00000h, the $\overline{LCS}$ pin is usually used to control data memory. The $\overline{LCS}$ pin is not active on reset.

Midrange Memory Chip Selects

The Am186EM and Am188EM microcontrollers provide four chip selects, $\overline{MCS}$3–$\overline{MCS}$0, for use in a user-locatable memory block. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the $\overline{UCS}$ and $\overline{LCS}$ chip selects, as well as the address range of the Peripheral Chip Selects, $\overline{PCS}$6, $\overline{PCS}$5, and $\overline{PCS}$3–$\overline{PCS}$0, if they are mapped to memory. The $\overline{MCS}$ address range can overlap the $\overline{PCS}$ address range if the $\overline{PCS}$ chip selects are mapped to I/O space.

Unlike the $\overline{UCS}$ and $\overline{LCS}$ chip selects, the $\overline{MCS}$ outputs assert with the multiplexed AD address bus.

Peripheral Chip Selects

The Am186EM and Am188EM microcontrollers provide six chip selects, $\overline{PCS}$6–$\overline{PCS}$5 and $\overline{PCS}$3–$\overline{PCS}$0, for use within a user-locatable memory or I/O block. $\overline{PCS}$4 is not available on the Am186EM and Am188EM microcontrollers. The base address of the memory block can be located anywhere within the 1-Mbyte memory address space, exclusive of the areas associated with the $\overline{UCS}$, $\overline{LCS}$, and $\overline{MCS}$ chip selects, or they can be configured to access the 64 Kbyte I/O space.

The $\overline{PCS}$ pins are not active on reset. $\overline{PCS}$6–$\overline{PCS}$5 can have from zero to three wait states. $\overline{PCS}$3–$\overline{PCS}$0 can have four additional wait-state values—5, 7, 9, and 15.

Unlike the $\overline{UCS}$ and $\overline{LCS}$ chip selects, the $\overline{PCS}$ outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers.

REFRESH CONTROL UNIT

The Refresh Control Unit (RCU) automatically generates refresh bus cycles. After a programmable period of time, the RCU generates a memory read request to the bus interface unit. The RCU is fixed to three wait states for the PSRAM auto refresh mode.

If the HLDA pin is active when a refresh request is generated (indicating a bus hold condition), then the Am186EM and Am188EM microcontrollers deactivate the HLDA pin in order to perform a refresh cycle. The external bus master must remove the HOLD signal for at least one clock in order to allow the refresh cycle to execute. The sequence of HLDA going inactive while HOLD is being held active can be used to signal a pending refresh request.

INTERRUPT CONTROL UNIT

The Am186EM and Am188EM microcontrollers can receive interrupt requests from a variety of sources, both internal and external. The internal interrupt controller arranges these requests by priority and presents them one at a time to the CPU.

There are six external interrupt sources on the Am186EM and Am188EM microcontrollers—five maskable interrupt pins and one nonmaskable interrupt pin. In addition, there are six total internal interrupt sources—three timers, two DMA channels, and the asynchronous serial port—that are not connected to external pins.

The Am186EM and Am188EM microcontrollers provide three interrupt sources not present on the Am186 and Am188 microcontrollers. The first is an additional external interrupt pin (INT4). This pin operates much like the already existing interrupt pins (INT3–INT0). The second is an internal watchdog timer interrupt. The third is an internal interrupt from the asynchronous serial port.

The five maskable interrupt request pins can be used as direct interrupt requests, or they can be cascaded with an 82C59A-compatible external interrupt controller if more inputs are needed. An external interrupt controller can be used as the system master by programming the internal interrupt controller to operate in slave mode. In all cases, nesting can be enabled so that interrupt service routines for lower priority interrupts are interrupted by a higher priority interrupt.

TIMER CONTROL UNIT

There are three 16-bit programmable timers in the Am186EM and Am188EM microcontrollers. Timer 0 and timer 1 are connected to four external pins (each one has an input and an output). These two timers can be used to count or time external events, or to generate nonrepetitive or variable-duty-cycle waveforms. In addition, timer 1 can be configured as a watchdog timer interrupt.

The watchdog timer interrupt provides a mechanism for detecting software crashes or hangs. The TMROUT1 output is internally connected to the watchdog timer interrupt. The TIMER1 count register must then be reloaded at intervals less than the TIMER1 max count to assure the watchdog interrupt is not taken. If the code crashes or hangs, the TIMER1 countdown will cause a watchdog interrupt.

Timer 2 is not connected to any external pins. It can be used for real-time coding and time-delay applications. It can also be used as a prescale to timers 0 and 1 or as a DMA request source.

The timers are controlled by eleven 16-bit registers in the peripheral control block. A timer's timer-count register contains the current value of that timer. The timer-count register can be read or written with a value at any time, regardless of whether the timer is running. The microcontroller increments the value of the timer-count register each time a timer event occurs.

Each timer also has a maximum-count register that defines the maximum value the timer will reach. When the timer reaches the maximum value, it resets to 0 during the same clock cycle—the value in the maximum-count register is never stored in the timer-count register. Also, timers 0 and 1 have a secondary maximum-count register. Using both the primary and secondary maximum-count registers lets the timer alternate between two maximum values.

If the timer is programmed to use only the primary maximum-count register, the timer output pin switches Low for one clock cycle after the maximum value is reached. If the timer is programmed to use both of its maximum-count registers, the output pin indicates which maximum-count register is currently in control, thereby creating a waveform. The duty cycle of the waveform depends on the values in the maximum-count registers.

Each timer is serviced every fourth clock cycle, so a timer can operate at a speed of up to one-quarter the internal clock frequency. A timer can be clocked externally at this same frequency; however, because of internal synchronization and pipelining of the timer circuitry, the timer output may take up to six clock cycles to respond to the clock or gate input.

DIRECT MEMORY ACCESS (DMA)

Direct memory access (DMA) permits transfer of data between memory and peripherals without CPU involvement. The DMA unit in the Am186EM and Am188EM microcontrollers, shown in Figure 10, provides two high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., memory to I/O) or within the same space (e.g., memory-to-memory or I/O-to-I/O). In addition, either bytes or words can be transferred to or from even or odd addresses on the Am186EM microcontroller. The Am188EM microcontroller does not support word transfers. Only two bus cycles (a minimum of eight clocks) are necessary for each data transfer.

Each channel accepts a DMA request from one of three sources—the channel request pin (DRQ1–DRQ0), timer 2, or the system software. The channels can be programmed with different priorities in the event of a simultaneous DMA request or if there is a need to interrupt transfers on the other channel.

DMA Operation

Each channel has six registers in the peripheral control block that define specific channel operations. The DMA registers consist of a 20-bit source address (2 registers), a 20-bit destination address (2 registers), a 16-bit transfer count register, and a 16-bit control register.

The DMA transfer count register (DTC) specifies the number of DMA transfers to be performed. Up to 64K byte or word transfers can be performed with automatic termination. The DMA control registers define the channel operation. All registers can be modified during any DMA activity. Any changes made to the DMA registers are reflected immediately in DMA operation.

Table 6. Am186EM Microcontroller Maximum DMA Transfer Rates

Type of Synchronization Selected	Maximum DMA Transfer Rate (Mbyte/s)			
	40 MHz	33 MHz	25 MHz	20 MHz
Unsynchronized	10	8.25	6.25	5
Source Synch	10	8.25	6.25	5
Destination Synch (CPU needs bus)	6.6	5.5	4.16	3.3
Destination Synch (CPU does not need bus)	8	6.6	5	4

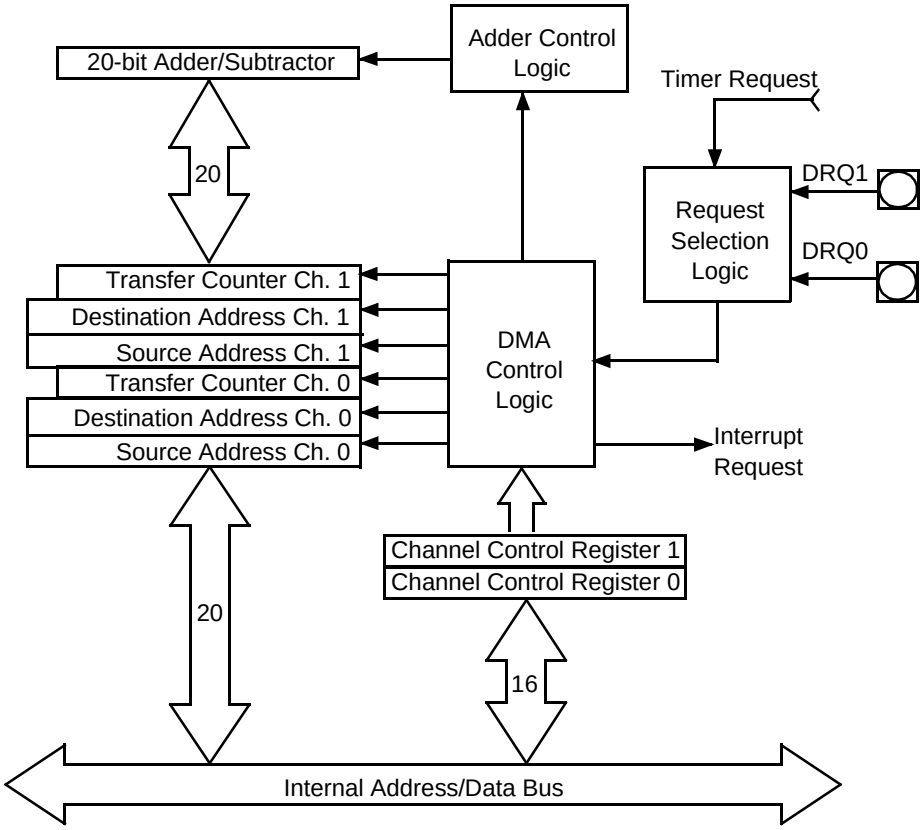


Figure 10. DMA Unit Block Diagram

DMA Channel Control Registers

Each DMA control register determines the mode of operation for the particular DMA channel. This register specifies the following:

- The mode of synchronization
- Whether bytes or words are transferred
- If an interrupt is generated after the last transfer
- If DMA activity ceases after a programmed number of DMA cycles
- The relative priority of the DMA channel with respect to the other DMA channel
- Whether the source address is incremented, decremented, or maintained constant after each transfer
- Whether the source address addresses memory or I/O space
- Whether the destination address is incremented, decremented, or maintained constant after transfers
- Whether the destination address addresses memory or I/O space

DMA Priority

The DMA channels can be programmed so that one channel is always given priority over the other, or they can be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles, except between locked memory accesses or word accesses to odd memory locations. However, an external bus hold takes priority over an internal DMA cycle.

Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time suffers during sequences of continuous DMA cycles. An NMI request, however, causes all internal DMA activity to halt. This allows the CPU to respond quickly to the NMI request.

ASYNCHRONOUS SERIAL PORT

The Am186EM and Am188EM microcontrollers provide an asynchronous serial port. The asynchronous serial port is a two-pin interface that permits full-duplex bidirectional data transfer. The asynchronous serial port supports the following features:

- Full-duplex operation
- 7-bit or 8-bit data transfers
- Odd, even, or no parity
- 1 or 2 stop bits

If additional RS-232 signals are required, they can be created with available PIO pins. The asynchronous serial port transmit and receive sections are double buffered. Break character, framing, parity, and overrun error detection are provided. Exception interrupt generation is programmable by the user.

The transmit/receive clock is based on the internal processor clock, which is divided down internally to the serial port operating frequency. The serial port permits 7-bit and 8-bit data transfers. DMA transfers through the serial port are not supported.

The serial port generates one interrupt for any of three serial port events—transmit complete, data received, and error.

The serial port can be used in power-save mode, but the software must adjust the transfer rate to correctly reflect the new internal operating frequency and must ensure that the serial port does not receive any information while the frequency is being changed.

SYNCHRONOUS SERIAL INTERFACE

The synchronous serial interface (SSI) lets the Am186EM and Am188EM microcontrollers communicate with application-specific integrated circuits (ASICs) that require reprogrammability but are short on pins. This four-pin interface permits half-duplex, bidirectional data transfer at speeds of up to 20 Mbits/sec.

Unlike the asynchronous serial port, the SSI operates in a master/slave configuration. The Am186EM and Am188EM microcontrollers are the master port.

The SSI interface provides four pins for communicating with system components: two enables (SDEN0 and SDEN1), a clock (SCLK), and a data pin (SDATA). Five registers are used to control and monitor the interface.

Four-Pin Interface

The two enable pins SDEN1–SDEN0 can be used directly as enables for up to two peripheral devices.

Transmit and receive operations are synchronized between the master (Am186EM and Am188EM microcontrollers) and slave (peripheral) by means of the SCLK output. SCLK is derived from the internal processor clock and is the processor clock divided by 2, 4, 8, or 16.

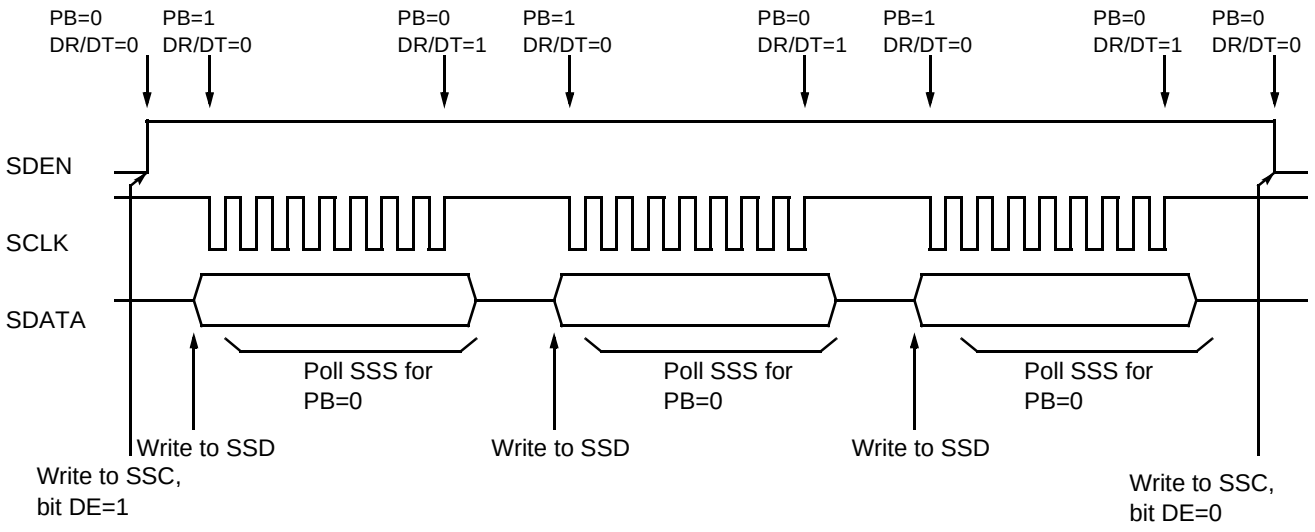


Figure 11. Synchronous Serial Interface Multiple Write

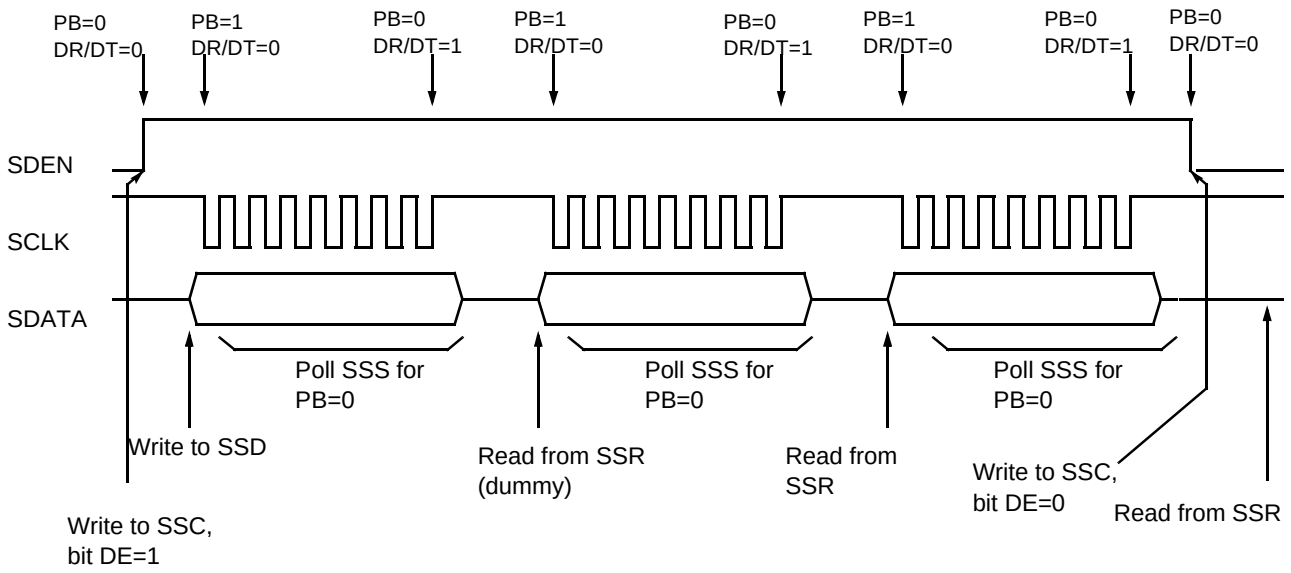


Figure 12. Synchronous Serial Interface Multiple Read

PROGRAMMABLE I/O (PIO) PINS

There are 32 pins on the Am186EM and Am188EM microcontrollers that are available as user multipurpose signals. Table 2 and Table 3 on page 30 list the PIO pins. Each of these pins can be used as a user-programmable input or output signal if the normal shared function is not needed.

If a pin is enabled to function as a PIO signal, the preassigned signal function is disabled and does not affect the level on the pin. A PIO signal can be configured to operate as an input or output with or without a weak pullup or pulldown, or as an open-drain output.

After power-on reset, the PIO pins default to various configurations. The column titled *Power-On Reset Status* in Table 2 and Table 3 on page 30 lists the defaults for the PIOs. The system initialization code must reconfigure the PIOs as required.

The A19–A17 address pins default to normal operation on power-on reset, allowing the processor to correctly begin fetching instructions at the boot address FFFF0h. The DT/$\overline{R}$, $\overline{DEN}$, and SRDY pins also default to normal operation on power-on reset.

Note that emulators use A19, A18, A17, S6, and $\overline{UZI}$.

If the AD15–AD0 bus override is enabled on power-on reset, then S6/$\overline{CLKDIV}$2 and $\overline{UZI}$ revert to normal operation instead of PIO input with pullup. If $\overline{BHE}$/$\overline{ADEN}$ (186) or $\overline{RFSH}$2/$\overline{ADEN}$ (188) is held Low during power-on reset the AD15–AD0 bus override is enabled.

ABSOLUTE MAXIMUM RATINGS

Storage temperature

Am186EM/Am188EM ..... –65°C to +125°C
Am186EMLV/Am188EMLV..... –65°C to +125°C

Voltage on any pin with respect to ground

Am186/188EM ..... –0.5 V to V_{cc} +0.5 V
Am186/188EMLV..... –0.5 V to V_{cc} +0.5 V

Note: *Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

OPERATING RANGES

Operating Ranges define those limits between which the functionality of the device is guaranteed.

Am186EM/Am188EM Microcontrollers

Commercial (T_C) .....0°C to +100°C
Industrial* (T_A).....–40°C to +85°C
V_{CC} up to 33 MHz..... 5 V ± 10%
V_{CC} greater than 33 MHz..... 5 V ± 5%

Am186EMLV/Am188EMLV Microcontrollers

Commercial (T_A) .....0°C to +70°C
V_{CC} up to 25 MHz..... 3.3 V ± 0.3 V

Where: T_C = case temperature
T_A = ambient temperature

**Industrial versions of Am186EM and Am188EM microcontrollers are available in 20 and 25 MHz operating frequencies only.*

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Symbol	Parameter Description	Test Conditions	Preliminary Min	Preliminary Max	Unit
V_{IL}	Input Low Voltage (Except X1)		–0.5	0.8	V
V_{IL1}	Clock Input Low Voltage (X1)		–0.5	0.8	V
V_{IH}	Input High Voltage (Except $\overline{RES}$ and X1)		2.0	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage ($\overline{RES}$)		2.4	V_{CC} + 0.5	V
V_{IH2}	Clock Input High Voltage (X1)		V_{CC} – 0.8	V_{CC} + 0.5	V
V_{OL}	**Output Low Voltage**				
	Am186EM and Am188EM	I_{OL} = 2.5 mA ($\overline{S2}$–$\overline{S0}$) I_{OL} = 2.0 mA (others)		0.45	V
	Am186EMLV and Am188EMLV	I_{OL} = 1.5 mA ($\overline{S2}$–$\overline{S0}$) I_{OL} = 1.0 mA (others)		0.45	V
V_{OH}	**Output High Voltage**[a]				
	Am186EM and Am188EM	I_{OH} = –2.4 mA @ 2.4 V	2.4	V_{CC} +0.5	V
		I_{OH} = –200 µA @ V_{CC}–0.5	V_{CC}–0.5	V_{CC}	V
	Am186EMLV and Am188EMLV	I_{OH} = –200 µA @ V_{CC}–0.5	V_{CC}–0.5	V_{CC}	V
I_{CC}	**Power Supply Current @ 0°C**				
	Am186EM and Am188EM	V_{CC} = 5.5 V [b]		5.9	mA/MHz
	Am186EMLV and Am188EMLV	V_{CC} = 3.6 V [b]		2.75	mA/MHz
V_{OL}	Output Low Voltage	I_{OL} = 2.5 mA ($\overline{S2}$–$\overline{S0}$) I_{OL} = 2.0 mA (others)		0.45	V
I_{LI}	Input Leakage Current @ 0.5 MHz	0.45 V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current @ 0.5 MHz	0.45 V ≤ V_{OUT} ≤ V_{CC}[d]		±10	µA
V_{CLO}	Clock Output Low	I_{CLO} = 4.0 mA		0.45	V
V_{CHO}	Clock Output High	I_{CHO} = –500 µA	V_{CC} – 0.5		V

Notes:

a *The* $\overline{LCS}$/$\overline{ONCE}$0, $\overline{MCS}$3–$\overline{MCS}$0, $\overline{UCS}$/$\overline{ONCE}$1, *and* $\overline{RD}$ *pins have weak internal pullup resistors. Loading the* $\overline{LCS}$/$\overline{ONCE}$0 *and* $\overline{UCS}$/$\overline{ONCE1}$ *pins in excess of* I_{OH} *= –200 µA during reset can cause the device to go into ONCE mode.*

b *Current is measured with the device in RESET with* X1 *and* X2 *driven, and all other non-power pins open but held High or Low.*

c *Power supply current for the Am186EMLV and Am188EMLV microcontrollers, which are available in 20 and 25 MHz operating frequencies only.*

d *Testing is performed with the pins floating, either during HOLD or by invoking the ONCE mode.*

DC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE (continued)

Symbol	Parameter Description	Test Conditions	Preliminary Typical	Unit
Nominal I_{CC}	Typical Power Supply Current @ 25°C	V_{CC} = 5.5 V [a]	4.5	mA/ MHz
Nominal I_{CC}	Am186EMLV and Am188EMLV Typical Power Supply Current @ 25°C	V_{CC} = 3.6 V [a] [b]	3.0	mA/ MHz
Peak I_{CC}	Measured Peak I_{CC}	V_{CC} = 5.5 V [c]	5.9	mA/ MHz
Peak I_{CC}	Am186EMLV and Am188EMLV Measured Peak I_{CC}	V_{CC} = 3.6 V [b] [c]	4.0	mA/ MHz

a Measured with a device running. Not tested and not guaranteed.

b Power supply current for the Am186EMLV and Am188EMLV microcontrollers, which are available in 20 and 25 MHz operating frequencies only.

c Power is measured while device is operating. Not tested and not guaranteed.

Capacitance

Symbol	Parameter Description	Test Conditions	Preliminary Min	Preliminary Max	Unit
C_{IN}	Input Capacitance	@ 1 MHz		10	pF
C_{IO}	Output or I/O Capacitance	@ 1 MHz		20	pF

Note:
Capacitance limits are guaranteed by characterization.

Power Supply Current

For the typical system specification shown in Figure 13, I_{CC} has been measured at 3.0 mA per MHz of system clock. For the typical system specification shown in Figure 14, I_{CC} has been measured at 4.5 mA per MHz of system clock. The typical system is measured while the system is executing code in a typical application with maximum voltage and at room temperature. Actual power supply current is dependent on system design and may be greater or less than the typical I_{CC} figure presented here.

Typical current in Figure 13 is given by:
..... $I_{CC} = 3.0$ mA · freq(MHz).

Typical current in Figure 14 is given by:
..... $I_{CC} = 4.5$ mA · freq(MHz).

Please note that dynamic I_{CC} measurements are dependent upon chip activity, operating frequency, output buffer logic, and capacitive/resistive loading of the outputs. For these I_{CC} measurements, the devices were set to the following modes:

- No DC loads on the output buffers
- Output capacitive load set to 35 pF
- AD bus set to data only
- PIOs are disabled
- Timer, serial port, refresh, and DMA are enabled

Table 7 shows the variables that are used to calculate the typical power consumption value for each version of the Am186EMLV and Am188EMLV microcontrollers.

Table 7. Typical Power Consumption Calculation for the Am186EMLV and Am188EMLV

MHz · I_{CC} · Volts / 1000 = P			Typical Power in Watts
MHz	Typical I_{CC}	Volts	
16	3.0	3.6	0.173
20	3.0	3.6	0.216
25	3.0	3.6	0.270

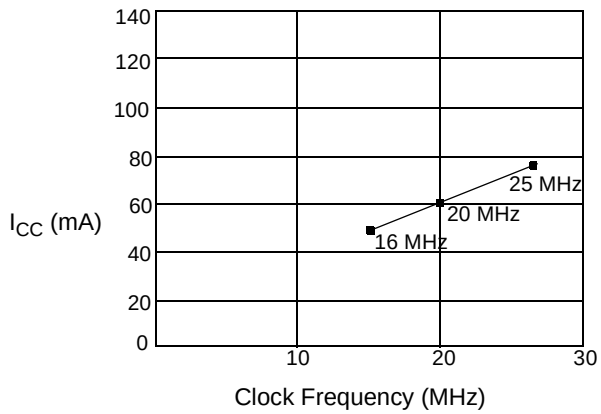


Figure 13. Typical I_{CC} Versus Frequency for the Am186EMLV and Am188EMLV

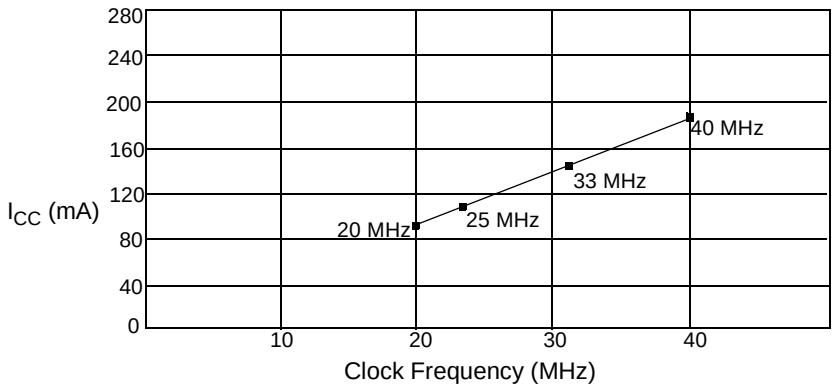


Figure 14. Typical I_{CC} Versus Frequency for the Am186EM and Am188EM

THERMAL CHARACTERISTICS

TQFP Package

The Am186EM and Am188EM microcontrollers are specified for operation with case temperature ranges from 0°C to +100°C for a commercial temperature device. Case temperature is measured at the top center of the package as shown in Figure 15. The various temperatures and thermal resistances can be determined using the equations in Figure 16 with information given in Table 8.

θ_{JA} is the sum of θ_{JC} and θ_{CA}. θ_{JC} is the internal thermal resistance of the assembly. θ_{CA} is the case to ambient thermal resistance.

The variable P is power in watts. Typical power supply current (I_{CC}) for the Am186EM and Am188EM microcontrollers is 5.9 mA per MHz of clock frequency.

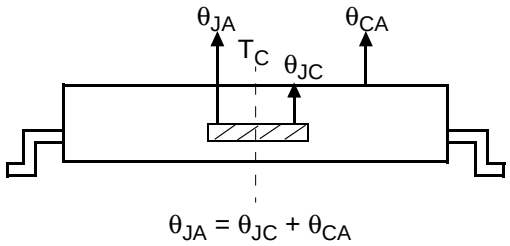


Figure 15. Thermal Resistance (°C/Watt)

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$
$$P = 5.9\ \text{mA} \cdot \text{freq (MHz)} \cdot V_{CC}$$
$$T_J = T_C + (P \cdot \theta_{JC})$$
$$T_J = T_A + (P \cdot \theta_{JA})$$
$$T_C = T_J - (P \cdot \theta_{JC})$$
$$T_C = T_A + (P \cdot \theta_{CA})$$
$$T_A = T_J - (P \cdot \theta_{JA})$$
$$T_A = T_C - (P \cdot \theta_{CA})$$

Figure 16. Thermal Characteristics Equations

Table 8. Thermal Characteristics (°C/Watt)

Package/Board	Airflow (Linear Feet per Minute)	θ_{JC}	θ_{CA}	θ_{JA}
PQFP/2-Layer	0 fpm	7	38	45
	200 fpm	7	32	39
	400 fpm	7	28	35
	600 fpm	7	26	33
TQFP/2-Layer	0 fpm	10	46	56
	200 fpm	10	36	46
	400 fpm	10	30	40
	600 fpm	10	28	38
PQFP/4-Layer to 6-Layer	0 fpm	5	18	23
	200 fpm	5	16	21
	400 fpm	5	14	19
	600 fpm	5	12	17
TQFP/4-Layer to 6-Layer	0 fpm	6	24	30
	200 fpm	6	22	28
	400 fpm	6	20	26
	600 fpm	6	18	24

Typical Ambient Temperatures

The typical ambient temperature specifications are based on the following assumptions and calculations:

The commercial operating range of the Am186EM and Am188EM microcontrollers is a case temperature T_C of 0 to 100 degrees Centigrade. T_C is measured at the top center of the package. An increase in the ambient temperature causes a proportional increase in T_C.

The 40-MHz microcontroller is specified as 5.0 V, plus or minus 5%. Therefore, 5.25 V is used for calculating typical power consumption on the 40-MHz microcontroller.

Microcontrollers up to 33 MHz are specified as 5.0 V, plus or minus 10%. Therefore, 5.5 V is used for calculating typical power consumption up to 33 MHz.

Typical power supply current (I_{CC}) in normal usage is estimated at 5.9 mA per MHz of microcontroller clock rate.

Typical power consumption (watts) = (5.9 mA/MHz) times microcontroller clock rate times voltage divided by 1000.

Table 9 shows the variables that are used to calculate the typical power consumption value for each version of the Am186EM and Am188EM microcontrollers.

Table 9. Typical Power Consumption Calculation

$P = MHz \cdot I_{CC} \cdot Volts / 1000$			Typical Power (P) in Watts
MHz	Typical I_{CC}	Volts	
40	5.9	5.25	1.239
33	5.9	5.5	1.07085
25	5.9	5.5	0.81125
20	5.9	5.5	0.649

Thermal resistance is a measure of the ability of a package to remove heat from a semiconductor device. A safe operating range for the device can be calculated using the following formulas from Figure 16 and the variables in Table 8.

By using the maximum case rating T_C, the typical power consumption value from Table 9, and θ_{JC} from Table 8, the junction temperature T_J can be calculated by using the following formula from Figure 16.

$T_J = T_C + (P \cdot \theta_{JC})$

Table 10 shows T_J values for the various versions of the Am186EM and Am188EM microcontrollers. The column titled *Speed/Pkg/Board* in Table 10 indicates the clock speed in MHz, the type of package (P for PQFP and T for TQFP), and the type of board (2 for 2-layer and 4–6 for 4-layer to 6-layer).

Table 10. Junction Temperature Calculation

Speed/ Pkg/ Board	$T_J = T_C + (P \cdot \theta_{JC})$			
	T_C	P	θ_{JC}	T_J
40/P2	100	1.239	7	108.7
40/T2	100	1.239	10	112.4
40/P4–6	100	1.239	5	106.2
40/T4–6	100	1.239	6	107.4
33/P2	100	1.07085	7	107.5
33/T2	100	1.07085	10	110.7
33/P4–6	100	1.07085	5	105.3
33/T4–6	100	1.07085	6	106.4
25/P2	100	0.81125	7	105.7
25/T2	100	0.81125	10	108.1
25/P4–6	100	0.81125	5	104.1
25/T4–6	100	0.81125	6	104.9
20/P2	100	0.649	7	104.5
20/T2	100	0.649	10	106.5
20/P4–6	100	0.649	5	103.2
20/T4–6	100	0.649	6	103.9

By using T_J from Table 10, the typical power consumption value from Table 9, and a θ_{JA} value from Table 8, the typical ambient temperature T_A can be calculated using the following formula from Figure 16.

$T_A = T_J – (P \cdot \theta_{JA})$

For example, T_A for a 40-MHz PQFP design with a 2-layer board and 0 fpm airflow is calculated as follows:

$T_A = 108.673 – (1.239 \cdot 45)$
$T_A = 52.918$

In this calculation, T_J comes from Table 10, P comes from Table 9, and θ_{JA} comes from Table 8. See Table 11.

T_A for a 33-MHz TQFP design with a 4-layer to 6-layer board and 200 fpm airflow is calculated as follows:

$T_A = 106.4251 – (1.07085 \cdot 28)$
$T_A = 76.4413$

See Table 14 for the result of this calculation.

Table 11 through Table 14 and Figure 17 through Figure 20 show T_A based on the preceding assumptions and calculations for a range of θ_{JA} values with airflow from 0 linear feet per minute to 600 linear feet per minute.

Table 11 shows typical maximum ambient temperatures in degrees Centigrade for a PQFP package used with a 2-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 17 illustrates the typical temperatures in Table 11.

Table 11. Typical Ambient Temperatures for PQFP with 2-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
40 MHz	1.239	52.918	60.352	65.308	67.786
33 MHz	1.07085	59.3077	65.7328	70.0162	72.1579
25 MHz	0.81125	69.1725	74.04	77.285	78.9075
20 MHz	0.649	75.338	79.232	81.828	83.126

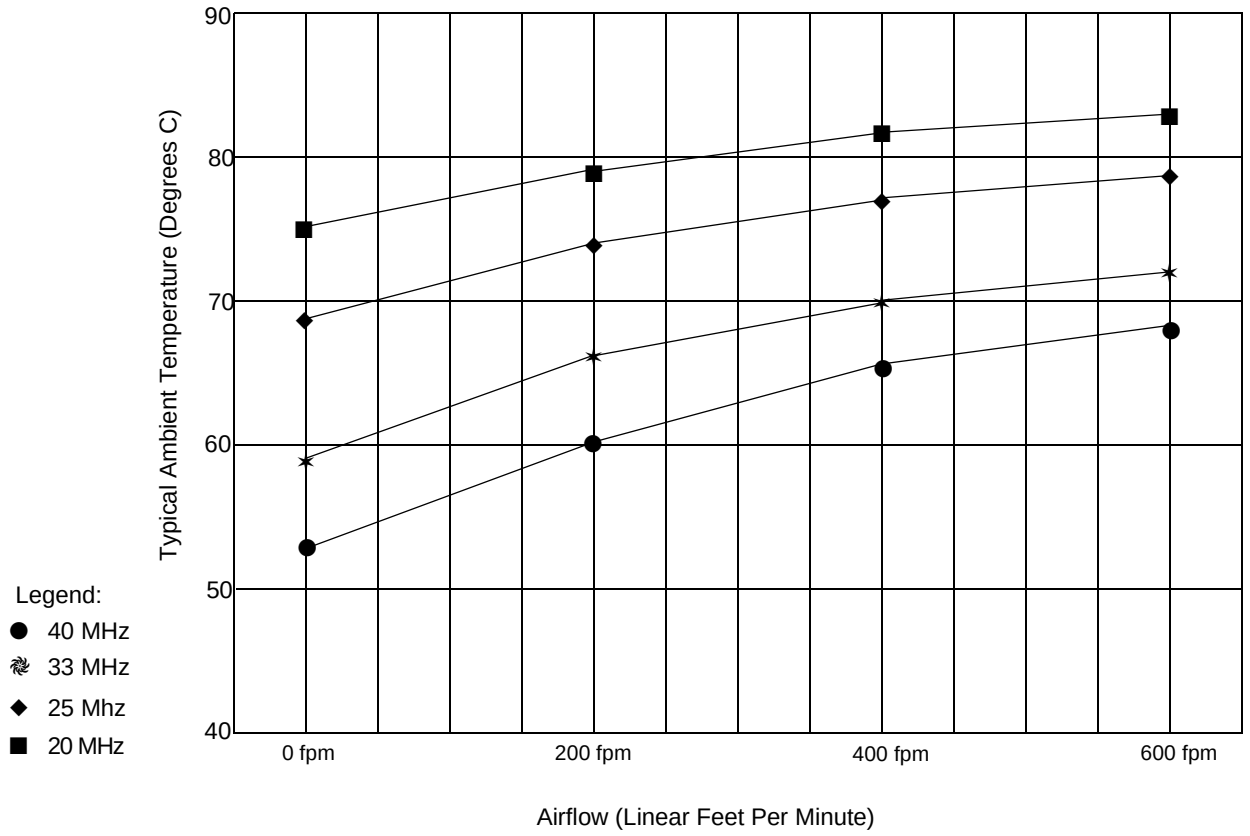


Figure 17. Typical Ambient Temperatures for PQFP with 2-Layer Board

Table 12 shows typical maximum ambient temperatures in degrees Centigrade for a TQFP package used with a 2-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 18 illustrates the typical temperatures in Table 12.

Table 12. Typical Ambient Temperatures for TQFP with 2-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
40 MHz	1.239	43.006	55.396	62.83	65.308
33 MHz	1.07085	50.7409	61.4494	67.8745	70.0162
25 MHz	0.81125	62.6825	70.795	75.6625	77.285
20 MHz	0.649	70.146	76.636	80.53	81.828

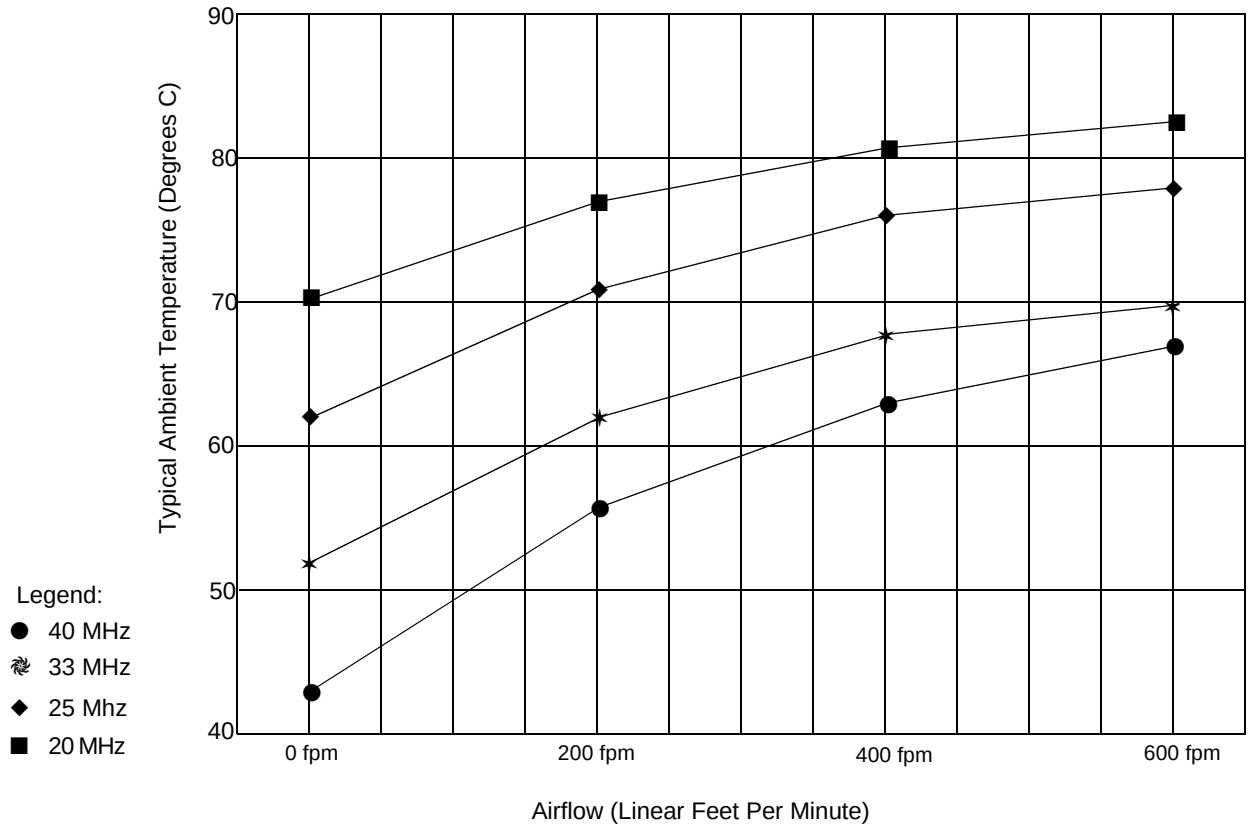


Figure 18. Typical Ambient Temperatures for TQFP with 2-Layer Board

Table 13 shows typical maximum ambient temperatures in degrees Centigrade for a PQFP package used with a 4-layer to 6-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 19 illustrates the typical temperatures in Table 13.

Table 13. Typical Ambient Temperatures for PQFP with 4-Layer to 6-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
40 MHz	1.239	77.698	80.176	82.654	85.132
33 MHz	1.07085	80.7247	82.8664	85.0081	87.1498
25 MHz	0.81125	85.3975	87.02	88.6425	90.265
20 MHz	0.649	88.318	89.616	90.914	92.212

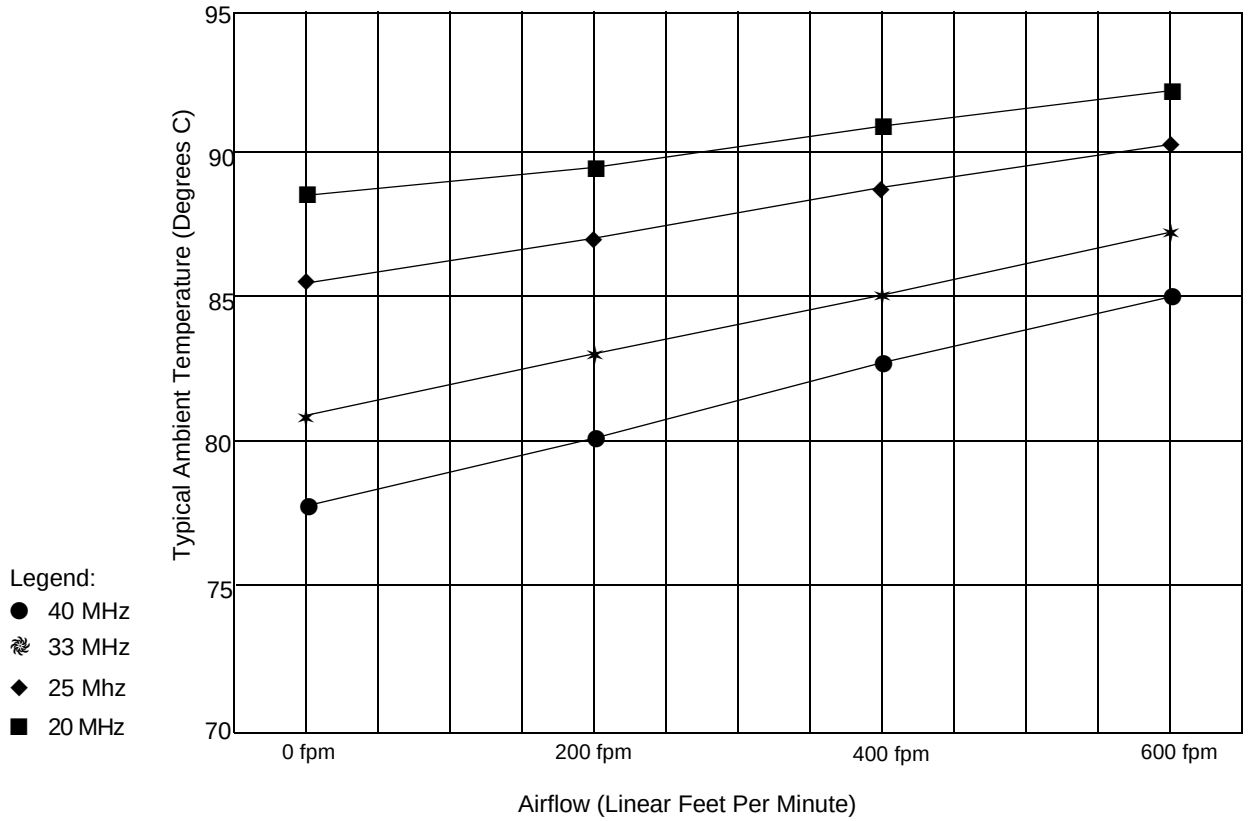


Figure 19. Typical Ambient Temperatures for PQFP with 4-Layer to 6-Layer Board

Table 14 shows typical maximum ambient temperatures in degrees Centigrade for a TQFP package used with a 4-layer to 6-layer board. The typical ambient temperatures are based on a 100-degree Centigrade maximum case temperature. Figure 20 illustrates the typical temperatures in Table 14.

Table 14. Typical Ambient Temperatures for TQFP with 4-Layer to 6-Layer Board

Microcontroller Speed	Typical Power (Watts)	Linear Feet per Minute Airflow			
		0 fpm	200 fpm	400 fpm	600 fpm
40 MHz	1.239	70.264	72.742	75.22	77.698
33 MHz	1.07085	74.2996	76.4413	78.583	80.7247
25 MHz	0.81125	80.53	82.1525	83.775	85.3975
20 MHz	0.649	84.424	85.722	87.02	88.318

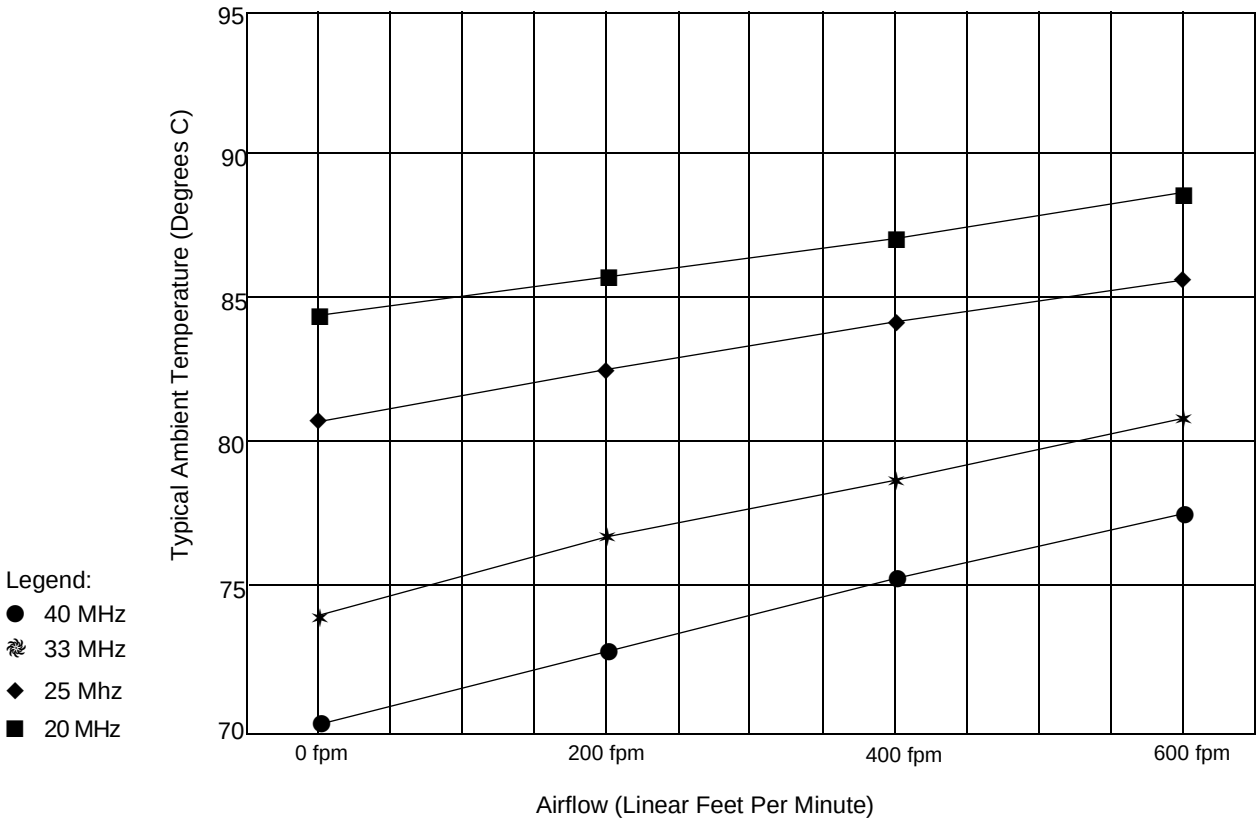


Figure 20. Typical Ambient Temperatures for TQFP with 4-Layer to 6-Layer Board

COMMERCIAL SWITCHING CHARACTERISTICS AND WAVEFORMS

In the switching waveforms that follow, several abbreviations are used to indicate the specific periods of a bus cycle. These periods are referred to as time states. A typical bus cycle is composed of four consecutive time states: t_1, t_2, t_3, and t_4. Wait states, which represent multiple t_3 states, are referred to as t_w states. When no bus cycle is pending, an idle (t_i) state occurs.

In the switching parameter descriptions, the *multiplexed* address is referred to as the AD address bus; the *demultiplexed* address is referred to as the A address bus.

Key to Switching Waveforms

WAVEFORM	INPUT	OUTPUT
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance *Off* State
	Invalid	Invalid

Alphabetical Key to Switching Parameter Symbols

Parameter Symbol	No.	Description	Parameter Symbol	No.	Description
t_{ARYCH}	49	ARDY Resolution Transition Setup Time	t_{CLDX}	2	Data in Hold
t_{ARYCHL}	51	ARDY Inactive Holding Time	t_{CLEV}	71	CLKOUTA Low to SDEN Valid
t_{ARYLCL}	52	ARDY Setup Time	t_{CLHAV}	62	HLDA Valid Delay
t_{AVBL}	87	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low	t_{CLRF}	82	CLKOUTA High to $\overline{RFSH}$ Invalid
t_{AVCH}	14	AD Address Valid to Clock High	t_{CLRH}	27	$\overline{RD}$ Inactive Delay
t_{AVLL}	12	AD Address Valid to ALE Low	t_{CLRL}	25	$\overline{RD}$ Active Delay
t_{AVRL}	66	A Address Valid to $\overline{RD}$ Low	t_{CLSH}	4	Status Inactive Delay
t_{AVWL}	65	A Address Valid to $\overline{WR}$ Low	t_{CLSL}	72	CLKOUTA Low to SCLK Low
t_{AZRL}	24	AD Address Float to $\overline{RD}$ Active	t_{CLSRY}	48	SRDY Transition Hold Time
t_{CH1CH2}	45	CLKOUTA Rise Time	t_{CLTMV}	55	Timer Output Delay
t_{CHAV}	68	CLKOUTA High to A Address Valid	t_{COAOB}	83	CLKOUTA to CLKOUTB Skew
t_{CHCK}	38	X1 High Time	t_{CVCTV}	20	Control Active Delay 1
t_{CHCL}	44	CLKOUTA High Time	t_{CVCTX}	31	Control Inactive Delay
t_{CHCSV}	67	CLKOUTA High to $\overline{LCS}$/$\overline{UCS}$ Valid	t_{CVDEX}	21	$\overline{DEN}$ Inactive Delay
t_{CHCSX}	18	$\overline{MCS}$/$\overline{PCS}$ Inactive Delay	t_{CXCSX}	17	$\overline{MCS}$/$\overline{PCS}$ Hold from Command Inactive
t_{CHCTV}	22	Control Active Delay 2	t_{DVCL}	1	Data in Setup
t_{CHCV}	64	Command Lines Valid Delay (after Float)	t_{DVSH}	75	Data Valid to SCLK High
t_{CHCZ}	63	Command Lines Float Delay	t_{DXDL}	19	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low
t_{CHDX}	8	Status Hold Time	t_{HVCL}	58	HOLD Setup
t_{CHLH}	9	ALE Active Delay	t_{INVCH}	53	Peripheral Setup Time
t_{CHLL}	11	ALE Inactive Delay	t_{INVCL}	54	DRQ Setup Time
t_{CHRFD}	79	CLKOUTA High to $\overline{RFSH}$ valid	t_{LCRF}	86	$\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay
t_{CHSV}	3	Status Active Delay	t_{LHAV}	23	ALE High to Address Valid
t_{CICOA}	69	X1 to CLKOUTA Skew	t_{LHLL}	10	ALE Width
t_{CICOB}	70	X1 to CLKOUTB Skew	t_{LLAX}	13	AD Address Hold from ALE Inactive
t_{CKHL}	39	X1 Fall Time	t_{LOCK}	61	Maximum PLL Lock Time
t_{CKIN}	36	X1 Period	t_{LRLL}	84	$\overline{LCS}$ Precharge Pulse Width
t_{CKLH}	40	X1 Rise Time	t_{RESIN}	57	$\overline{RES}$ Setup Time
t_{CL2CL1}	46	CLKOUTA Fall Time	t_{RFCY}	85	$\overline{RFSH}$ Cycle Time
t_{CLARX}	50	ARDY Active Hold Time	t_{RHAV}	29	$\overline{RD}$ Inactive to AD Address Active
t_{CLAV}	5	AD Address Valid Delay	t_{RHDX}	59	$\overline{RD}$ High to Data Hold on AD Bus
t_{CLAX}	6	Address Hold	t_{RHLH}	28	$\overline{RD}$ Inactive to ALE High
t_{CLAZ}	15	AD Address Float Delay	t_{RLRH}	26	$\overline{RD}$ Pulse Width
t_{CLCH}	43	CLKOUTA Low Time	t_{SHDX}	77	SCLK High to SPI Data Hold
t_{CLCK}	37	X1 Low Time	t_{SLDV}	78	SCLK Low to SPI Data Valid
t_{CLCL}	42	CLKOUTA Period	t_{SRYCL}	47	SRDY Transition Setup Time
t_{CLCLX}	80	$\overline{LCS}$ Inactive Delay	t_{WHDEX}	35	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive
t_{CLCSL}	81	$\overline{LCS}$ Active Delay	t_{WHDX}	34	Data Hold after $\overline{WR}$
t_{CLCSV}	16	$\overline{MCS}$/$\overline{PCS}$ Active Delay	t_{WHLH}	33	$\overline{WR}$ Inactive to ALE High
t_{CLDOX}	30	Data Hold Time	t_{WLWH}	32	$\overline{WR}$ Pulse Width
t_{CLDV}	7	Data Valid Delay			

Note:
The following parameters are not defined or used as this time: 41, 56, 60, 73, 74, 76.

Numerical Key to Switching Parameter Symbols

Number	Parameter Symbol	Description	Number	Parameter Symbol	Description
1	t_{DVCL}	Data in Setup	43	t_{CLCH}	CLKOUTA Low Time
2	t_{CLDX}	Data in Hold	44	t_{CHCL}	CLKOUTA High Time
3	t_{CHSV}	Status Active Delay	45	t_{CH1CH2}	CLKOUTA Rise Time
4	t_{CLSH}	Status Inactive Delay	46	t_{CL2CL1}	CLKOUTA Fall Time
5	t_{CLAV}	AD Address Valid Delay	47	t_{SRYCL}	SRDY Transition Setup Time
6	t_{CLAX}	Address Hold	48	t_{CLSRY}	SRDY Transition Hold Time
7	t_{CLDV}	Data Valid Delay	49	t_{ARYCH}	ARDY Resolution Transition Setup Time
8	t_{CHDX}	Status Hold Time	50	t_{CLARX}	ARDY Active Hold Time
9	t_{CHLH}	ALE Active Delay	51	t_{ARYCHL}	ARDY Inactive Holding Time
10	t_{LHLL}	ALE Width	52	t_{ARYLCL}	ARDY Setup Time
11	t_{CHLL}	ALE Inactive Delay	53	t_{INVCH}	Peripheral Setup Time
12	t_{AVLL}	AD Address Valid to ALE Low	54	t_{INVCL}	DRQ Setup Time
13	t_{LLAX}	AD Address Hold from ALE Inactive	55	t_{CLTMV}	Timer Output Delay
14	t_{AVCH}	AD Address Valid to Clock High	57	t_{RESIN}	$\overline{RES}$ Setup Time
15	t_{CLAZ}	AD Address Float Delay	58	t_{HVCL}	HOLD Setup
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive	61	t_{LOCK}	Maximum PLL Lock Time
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	62	t_{CLHAV}	HLDA Valid Delay
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	63	t_{CHCZ}	Command Lines Float Delay
20	t_{CVCTV}	Control Active Delay 1	64	t_{CHCV}	Command Lines Valid Delay (after Float)
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low
22	t_{CHCTV}	Control Active Delay 2	66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low
23	t_{LHAV}	ALE High to Address Valid	67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	68	t_{CHAV}	CLKOUTA High to Address Valid
25	t_{CLRL}	$\overline{RD}$ Active Delay	69	t_{CICOA}	X1 to CLKOUTA Skew
26	t_{RLRH}	$\overline{RD}$ Pulse Width	70	t_{CICOB}	X1 to CLKOUTB Skew
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	71	t_{CLEV}	CLKOUTA Low to SDEN Valid
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High	72	t_{CLSL}	CLKOUTA Low to SCLK Low
29	t_{RHAV}	$\overline{RD}$ Inactive to AD address Active	75	t_{DVSH}	Data Valid to SCLK High
30	t_{CLDOX}	Data Hold Time	77	t_{SHDX}	SCLK High to SPI Data Hold
31	t_{CVCTX}	Control Inactive Delay	78	t_{SLDV}	SCLK Low to SPI Data Valid
32	t_{WLWH}	$\overline{WR}$ Pulse Width	79	t_{CHRFD}	CLKOUTA High to $\overline{RFSH}$ Valid
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High	80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay
34	t_{WHDX}	Data Hold after $\overline{WR}$	81	t_{CLCSL}	$\overline{LCS}$ Active Delay
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	82	t_{CLRF}	CLKOUTA High to $\overline{RFSH}$ Invalid
36	t_{CKIN}	X1 Period	83	t_{COAOB}	CLKOUTA to CLKOUTB Skew
37	t_{CLCK}	X1 Low Time	84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width
38	t_{CHCK}	X1 High Time	85	t_{RFCY}	$\overline{RFSH}$ Cycle Time
39	t_{CKHL}	X1 Fall Time	86	t_{LCRF}	$\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay
40	t_{CKLH}	X1 Rise Time	87	t_{AVBL}	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low
42	t_{CLCL}	CLKOUTA Period			

Note:
The following parameters are not defined or used at this time: 41, 56, 60, 73, 74, and 76.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Read Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	10		10		ns
2	t_{CLDX}	Data in Hold[c]	3		3		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	25	0	20	ns
4	t_{CLSH}	Status Inactive Delay	0	25	0	20	ns
5	t_{CLAV}	AD Address Valid Delay and BHE	0	25	0	20	ns
6	t_{CLAX}	Address Hold	0	25	0	20	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	$t_{CHCL}-2$		$t_{CHCL}-2$		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	25	$t_{CLAX}=0$	20	ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	25	0	20	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	25	0	20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	25	0	20	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	25	0	20	ns
22	t_{CHCTV}	Control Active Delay 2[b]	0	25	0	20	ns
23	t_{LHAV}	ALE High to Address Valid	20		15		ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	25	0	20	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=85$		$2t_{CLCL}-15=65$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	25	0	20	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
29	t_{RHAV}	$\overline{RD}$ Inactive to AD Address Active[a]	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus[c]	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low[a]	$2t_{CLCL}-15=85$		$2t_{CLCL}-15=65$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	25	0	20	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	25	0	20	ns

Note:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, *and* $\overline{WLB}$ *signals.*

c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Read Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	8		5		ns
2	t_{CLDX}	Data in Hold[c]	3		2		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	15	0	12	ns
4	t_{CLSH}	Status Inactive Delay	0	15	0	12	ns
5	t_{CLAV}	AD Address Valid Delay and BHE	0	15	0	12	ns
6	t_{CLAX}	Address Hold	0	25	0	20	ns
7	t_{CLDV}	Data Valid Delay	0	15	0	12	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	$t_{CHCL}-2$		$t_{CHCL}-2$		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	15	$t_{CLAX}=0$	12	ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	15	0	12	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	15	0	12	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	15	0	12	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	15	0	12	ns
22	t_{CHCTV}	Control Active Delay 2[b]	0	15	0	12	ns
23	t_{LHAV}	ALE High to Address Valid	10		7.5		ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	15	0	10	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=45$		$2t_{CLCL}-10=40$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	15	0	12	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-3$		$t_{CLCH}-2$		ns
29	t_{RHAV}	$\overline{RD}$ Inactive to AD Address Active[a]	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus[c]	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low[a]	$2t_{CLCL}-15=45$		$2t_{CLCL}-10=40$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	15	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	15	0	10	ns

Notes:

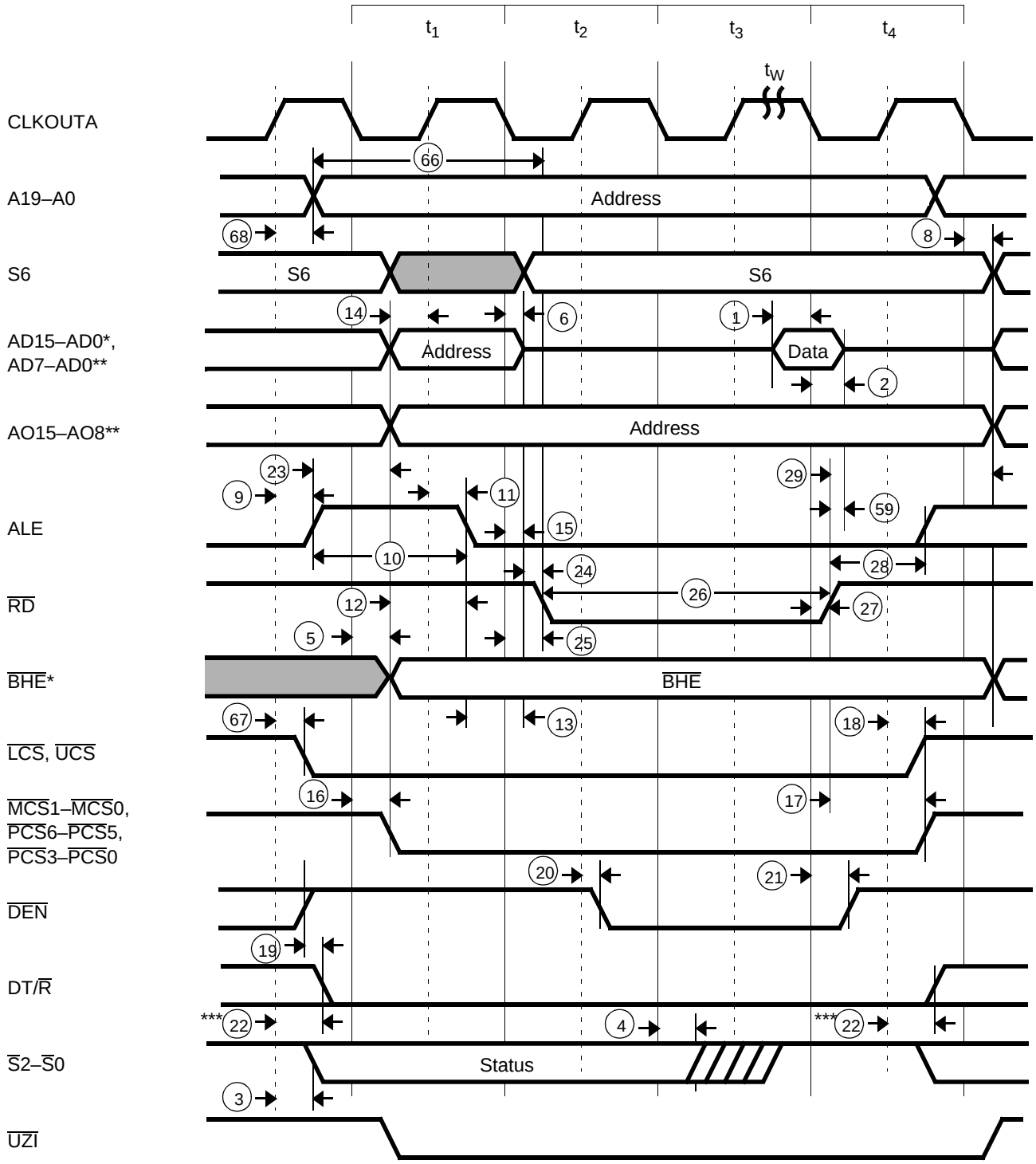
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, *and* $\overline{WLB}$ *signals.*

c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

Read Cycle Waveforms



Notes:

* *Am186EM microcontroller only*

** *Am188EM microcontroller only*

*** *Changes in t_4 phase of the clock preceding next bus cycle if followed by read, INTA, or halt*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Write Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	25	0	20	ns
4	t_{CLSH}	Status Inactive Delay	0	25	0	20	ns
5	t_{CLAV}	AD Address Valid Delay and BHE	0	25	0	20	ns
6	t_{CLAX}	Address Hold	0	25	0	20	ns
7	t_{CLDV}	Data Valid Delay	0	25	0	20	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	t_{CHCL}		t_{CHCL}		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	25	0	20	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	t_{CLCH}		t_{CLCH}		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	25	0	20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	25	0	20	ns
22	t_{CHCTV}	Control Active Delay 2	0	25	0	20	ns
23	t_{LHAV}	ALE High to Address Valid	20		15		ns
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	25	0	20	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10=90$		$2t_{CLCL}-10=70$		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[a]	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[a]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL}-3$		$t_{CLCL}+t_{CHCL}-3$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	25	0	20	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	25	0	20	ns
87	t_{AVBL}	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low	$t_{CHCL}-3$	25	$t_{CHCL}-3$	20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{INTA}1$–$\overline{INTA}0$, $\overline{WR}$, $\overline{WHB}$, *and* $\overline{WLB}$ *signals.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Write Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	15	0	12	ns
4	t_{CLSH}	Status Inactive Delay	0	15	0	12	ns
5	t_{CLAV}	AD Address Valid Delay and BHE	0	15	0	12	ns
6	t_{CLAX}	Address Hold	0	25	0	20	ns
7	t_{CLDV}	Data Valid Delay	0	15	0	12	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
12	t_{AVLL}	AD Address Valid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
13	t_{LLAX}	AD Address Hold from ALE Inactive[a]	t_{CHCL}		t_{CHCL}		ns
14	t_{AVCH}	AD Address Valid to Clock High	0		0		ns
16	t_{CLCSV}	$\overline{MCS}/\overline{PCS}$ Active Delay	0	15	0	12	ns
17	t_{CXCSX}	$\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a]	t_{CLCH}		t_{CLCH}		ns
18	t_{CHCSX}	$\overline{MCS}/\overline{PCS}$ Inactive Delay	0	15	0	12	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	15	0	12	ns
22	t_{CHCTV}	Control Active Delay 2	0	15	0	12	ns
23	t_{LHAV}	ALE High to Address Valid	10		7.5		ns
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	15	0	12	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10=50$		$2t_{CLCL}-10=40$		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[a]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[a]	$t_{CLCL}-10=20$		$t_{CLCL}-10=15$		ns
35	t_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[a]	$t_{CLCH}-5$		t_{CLCH}		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL}-3$		$t_{CLCL}+t_{CHCL}-1.25$		ns
67	t_{CHCSV}	CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid	0	15	0	10	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	15	0	10	ns
87	t_{AVBL}	A Address Valid to WHB, WLB Low	$t_{CHCL}-3$	15	$t_{CHCL}-1.25$	12	ns

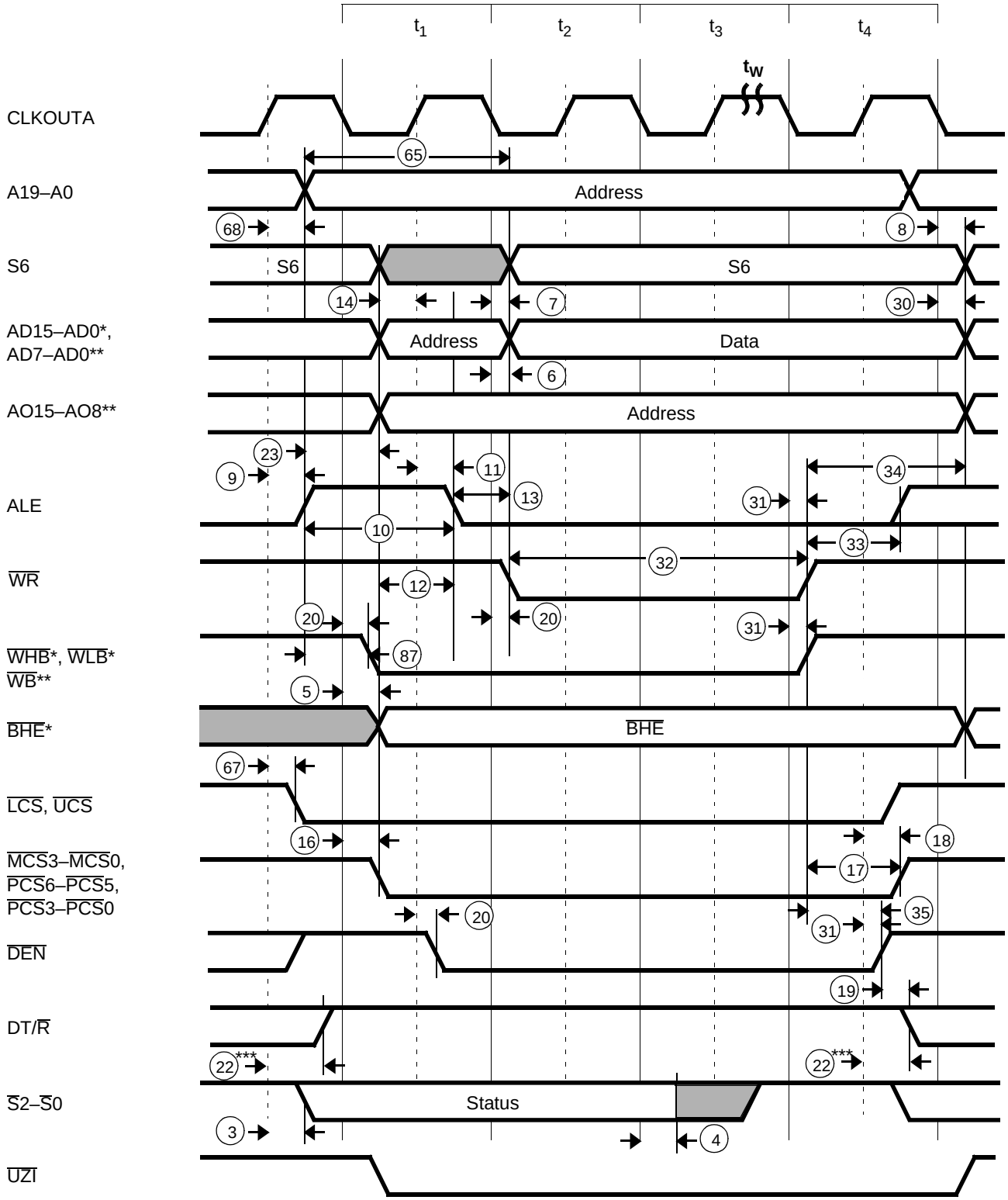
Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, *and* $\overline{WLB}$ *signals.*

Write Cycle Waveforms



Note:

* *Am186EM microcontroller only*

** *Am188EM microcontroller only*

*** *Changes in t_4 phase of the clock preceding next bus cycle if followed by read, INTA, or halt.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

PSRAM Read Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	10		10		ns
2	t_{CLDX}	Data in Hold[b]	3		3		ns
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay and BHE	0	25	0	20	ns
7	t_{CLDV}	Data Valid Delay	0	25	0	20	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
23	t_{LHAV}	ALE High to Address Valid	20		15		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	25	0	20	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	25	0	20	ns
84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width	$t_{CLCL}+t_{CLCH}-3$		$t_{CLCL}+t_{CLCH}-3$		ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	25	0	20	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=85$		$2t_{CLCL}-15=65$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	25	0	20	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus[b]	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low	$2t_{CLCL}-15=85$		$2t_{CLCL}-15=65$		ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	25	0	20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

SWITCHING CHARACTERISTICS over Commercial operating range

PSRAM Read Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	8		5		ns
2	t_{CLDX}	Data in Hold[b]	3		2		ns
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay and BHE	0	15	0	12	ns
7	t_{CLDV}	Data Valid Delay	0	15	0	12	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
23	t_{LHAV}	ALE High to Address Valid	10		7.5		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	15	0	12	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	15	0	12	ns
84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width	$t_{CLCL}+t_{CLCH}-3$		$t_{CLCL}+t_{CLCH}-1.25$		ns
Read Cycle Timing Responses							
24	t_{AZRL}	AD Address Float to $\overline{RD}$ Active	0		0		ns
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	15	0	10	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=45$		$2t_{CLCL}-10=40$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	15	0	12	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[a]	$t_{CLCH}-3$		$t_{CLCH}-1.25$		ns
59	t_{RHDX}	$\overline{RD}$ High to Data Hold on AD Bus[b]	0		0		ns
66	t_{AVRL}	A Address Valid to $\overline{RD}$ Low	$2t_{CLCL}-15=45$		$2t_{CLCL}-10=40$		ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	15	0	10	ns

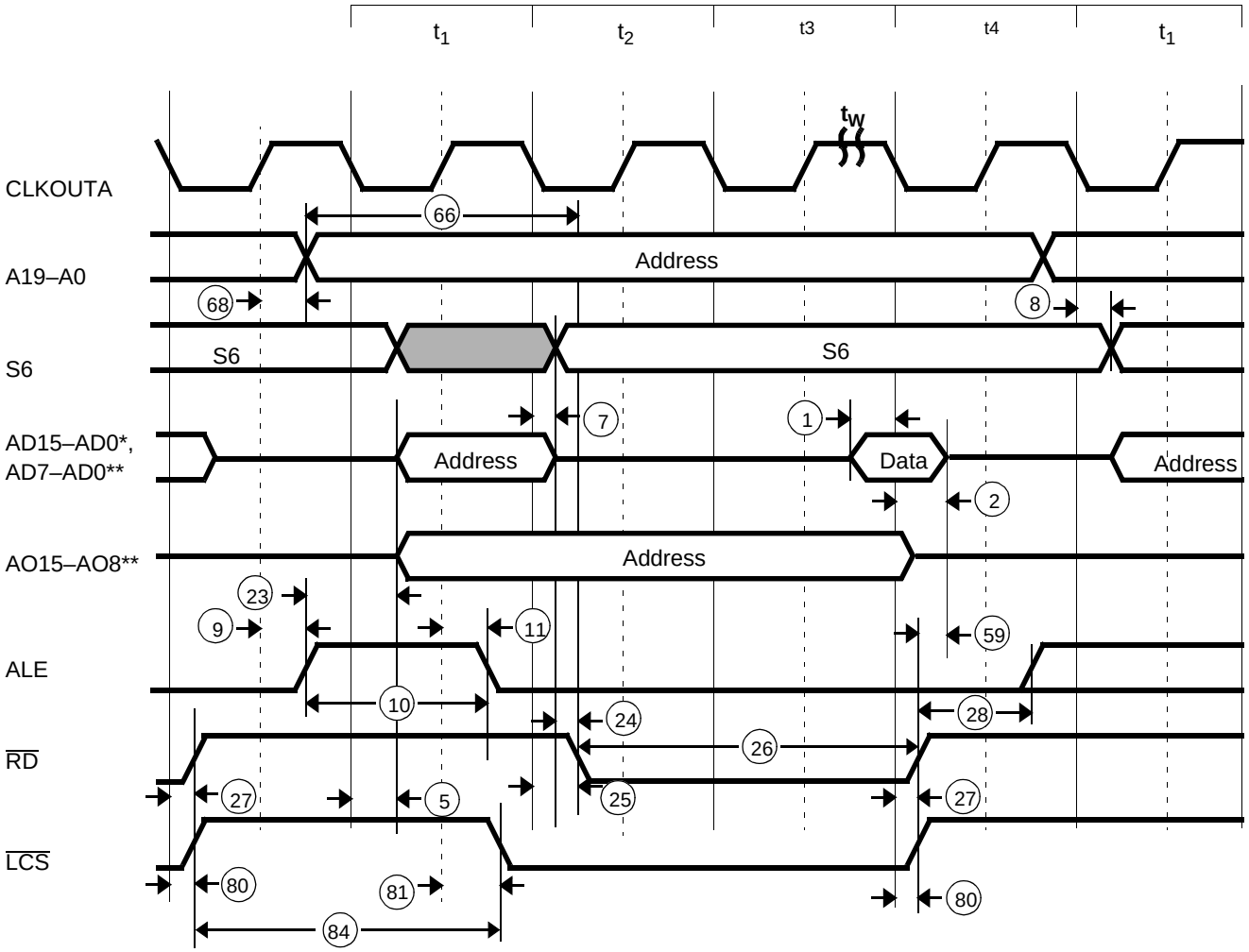
Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.

PSRAM Read Cycle Waveforms



Notes:

* *Am186EM microcontroller only*

** *Am188EM microcontroller only*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

PSRAM Write Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay and BHE	0	25	0	20	ns
7	t_{CLDV}	Data Valid Delay	0	25	0	20	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
23	t_{LHAV}	ALE High to Address Valid	20		15		ns
20	t_{CVCTV}	Control Active Delay 1[(b)]	0	25	0	20	ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	25	0	20	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	25	0	20	ns
84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width	$t_{CLCL} + t_{CLCH} -3$		$t_{CLCL} + t_{CLCH} - 3$		
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[(b)]	0	25	0	20	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10 =90$		$2t_{CLCL}-10 =70$		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[(a)]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[(a)]	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL} -3$		$t_{CLCL}+t_{CHCL} -3$		ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	25	0	20	ns
87	t_{AVBL}	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low	$t_{CHCL}-3$	25	$t_{CHCL}-3$	20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{WR}$, $\overline{WHB}$, *and* $\overline{WLB}$ *signals.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

PSRAM Write Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
5	t_{CLAV}	AD Address Valid Delay and BHE	0	15	0	12	ns
7	t_{CLDV}	Data Valid Delay	0	15	0	12	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
20	t_{CVCTV}	Control Active Delay 1[(b)]	0	15	0	12	ns
23	t_{LHAV}	ALE High to Address Valid	10		7.5		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	15	0	12	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	15	0	12	ns
84	t_{LRLL}	$\overline{LCS}$ Precharge Pulse Width	$t_{CLCL} + t_{CLCH} -3$		$t_{CLCL} + t_{CLCH} -1.25$		
Write Cycle Timing Responses							
30	t_{CLDOX}	Data Hold Time	0		0		ns
31	t_{CVCTX}	Control Inactive Delay[(b)]	0	15	0	12	ns
32	t_{WLWH}	$\overline{WR}$ Pulse Width	$2t_{CLCL}-10 =50$		$2t_{CLCL}-10 =40$		ns
33	t_{WHLH}	$\overline{WR}$ Inactive to ALE High[(a)]	$t_{CLCH}-2$		$t_{CLCH}-2$		ns
34	t_{WHDX}	Data Hold after $\overline{WR}$[(a)]	$t_{CLCL}-10=20$		$t_{CLCL}-10=15$		ns
65	t_{AVWL}	A Address Valid to $\overline{WR}$ Low	$t_{CLCL}+t_{CHCL} -3$		$t_{CLCL}+t_{CHCL} -1.25$		ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	15	0	10	ns
87	t_{AVBL}	A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low	$t_{CHCL}-3$	15	$t_{CHCL}-1.25$	12	ns

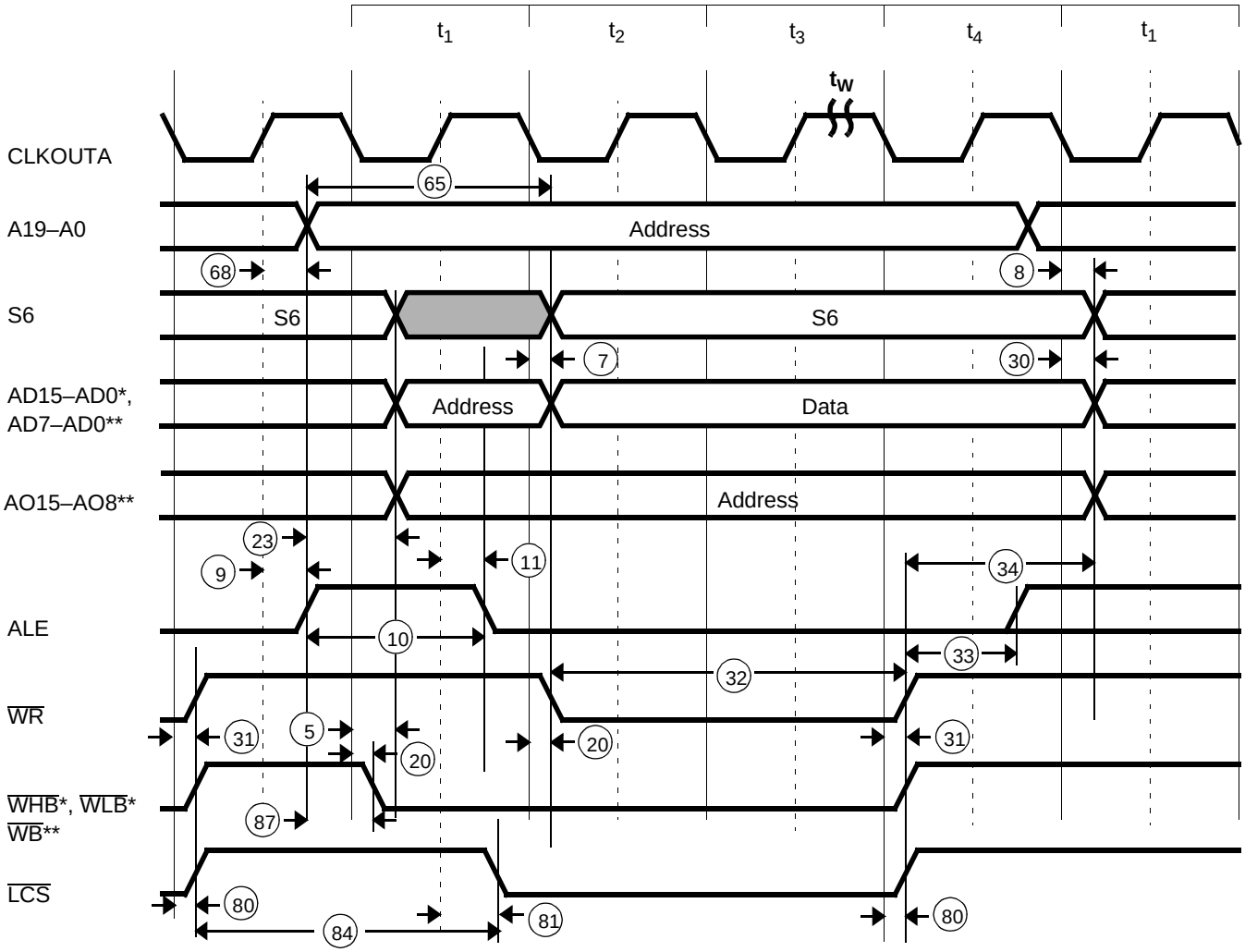
Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$, $\overline{WR}$, $\overline{WHB}$, *and* $\overline{WLB}$ *signals.*

PSRAM Write Cycle Waveforms



Notes:

* *Am186EM microcontroller only*

** *Am188EM microcontroller only*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

PSRAM Refresh Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
Read/Write Cycle Timing Responses							
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	25	0	20	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=85$		$2t_{CLCL}-15=65$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	25	0	20	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[(a)]	$t_{CLCH}-3$		$t_{CLCH}-3$		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	25	0	20	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	25	0	20	ns
Refresh Timing Cycle Parameters							
79	t_{CLRFD}	CLKOUTA Low to $\overline{RFSH}$ Valid	0	25	0	20	ns
82	t_{CLRF}	CLKOUTA High to $\overline{RFSH}$ Invalid	0	25	0	20	ns
85	t_{RFCY}	$\overline{RFSH}$ Cycle Time	$6 \bullet t_{CLCL}$		$6 \bullet t_{CLCL}$		ns
86	t_{LCRF}	$\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay	$2t_{CLCL}-3$		$2t_{CLCL}-3$		

Note:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

PSRAM Refresh Cycle (33 MHz and 40 MHz)

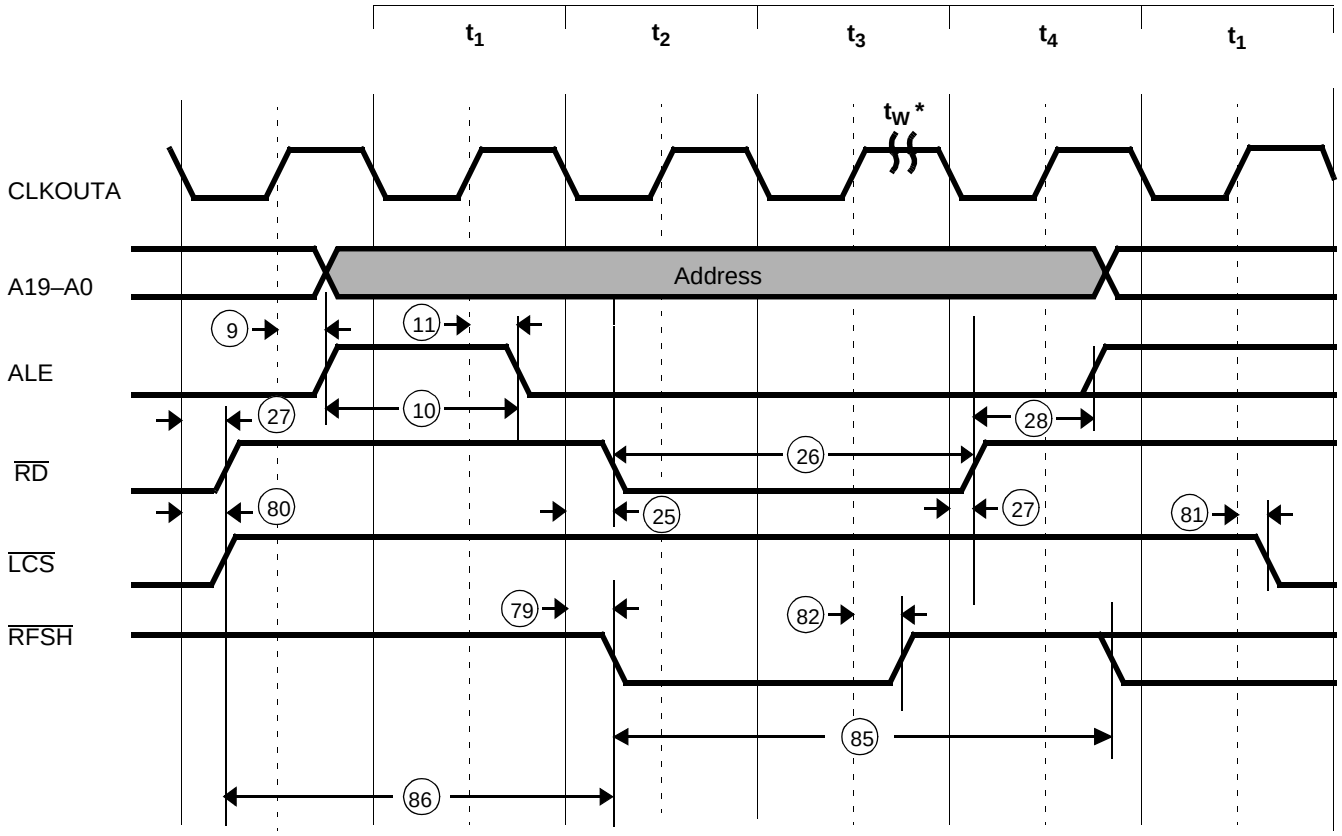
Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
Read/Write Cycle Timing Responses							
25	t_{CLRL}	$\overline{RD}$ Active Delay	0	15	0	10	ns
26	t_{RLRH}	$\overline{RD}$ Pulse Width	$2t_{CLCL}-15=45$		$2t_{CLCL}-10=40$		ns
27	t_{CLRH}	$\overline{RD}$ Inactive Delay	0	15	0	12	ns
28	t_{RHLH}	$\overline{RD}$ Inactive to ALE High[(a)]	$t_{CLCH}-3$		$t_{CLCH}-2$		ns
80	t_{CLCLX}	$\overline{LCS}$ Inactive Delay	0	15	0	12	ns
81	t_{CLCSL}	$\overline{LCS}$ Active Delay	0	15	0	12	ns
Refresh Timing Cycle Parameters							
79	t_{CLRFD}	CLKOUTA Low to $\overline{RFSH}$ Valid	0	15	0	12	ns
82	t_{CLRF}	CLKOUTA High to $\overline{RFSH}$ Invalid	0	15	0	12	ns
85	t_{RFCY}	$\overline{RFSH}$ Cycle Time	$6 \bullet t_{CLCL}$		$6 \bullet t_{CLCL}$		ns
86	t_{LCRF}	$\overline{LCS}$ Inactive to $\overline{RFSH}$ Active Delay	$2t_{CLCL}-3$		$2t_{CLCL}-1.25$		

Note:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

PSRAM Refresh Cycle Waveforms



Note:

***** *The period tw is fixed at 3 wait states for PSRAM auto refresh only.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Interrupt Acknowledge Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	10		10		ns
2	t_{CLDX}	Data in Hold	3		3		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	25	0	20	ns
4	t_{CLSH}	Status Inactive Delay	0	25	0	20	ns
7	t_{CLDV}	Data Valid Delay	0	25	0	20	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
12	t_{AVLL}	AD Address Invalid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	25	$t_{CLAX}=0$	20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	25	0	20	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	25	0	20	ns
22	t_{CHCTV}	Control Active Delay 2[c]	0	25	0	20	ns
23	t_{LHAV}	ALE High to Address Valid	20		15		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	25	0	20	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	25	0	20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{INTA}1$–$\overline{INTA}0$ *signals.*

c This parameter applies to the $\overline{DEN}$ and DT/$\overline{R}$ *signals.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Interrupt Acknowledge Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Requirements							
1	t_{DVCL}	Data in Setup	8		5		ns
2	t_{CLDX}	Data in Hold	3		2		ns
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	15	0	12	ns
4	t_{CLSH}	Status Inactive Delay	0	15	0	12	ns
7	t_{CLDV}	Data Valid Delay	0	15	0	12	ns
8	t_{CHDX}	Status Hold Time	0		0		ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
12	t_{AVLL}	AD Address Invalid to ALE Low[a]	t_{CLCH}		t_{CLCH}		ns
15	t_{CLAZ}	AD Address Float Delay	$t_{CLAX}=0$	15	$t_{CLAX}=0$	12	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a]	0		0		ns
20	t_{CVCTV}	Control Active Delay 1[b]	0	15	0	12	ns
21	t_{CVDEX}	$\overline{DEN}$ Inactive Delay	0	15	0	12	ns
22	t_{CHCTV}	Control Active Delay 2[c]	0	15	0	12	ns
23	t_{LHAV}	ALE High to Address Valid	10		7.5		ns
31	t_{CVCTX}	Control Inactive Delay[b]	0	15	0	12	ns
68	t_{CHAV}	CLKOUTA High to A Address Valid	0	15	0	10	ns

Notes:

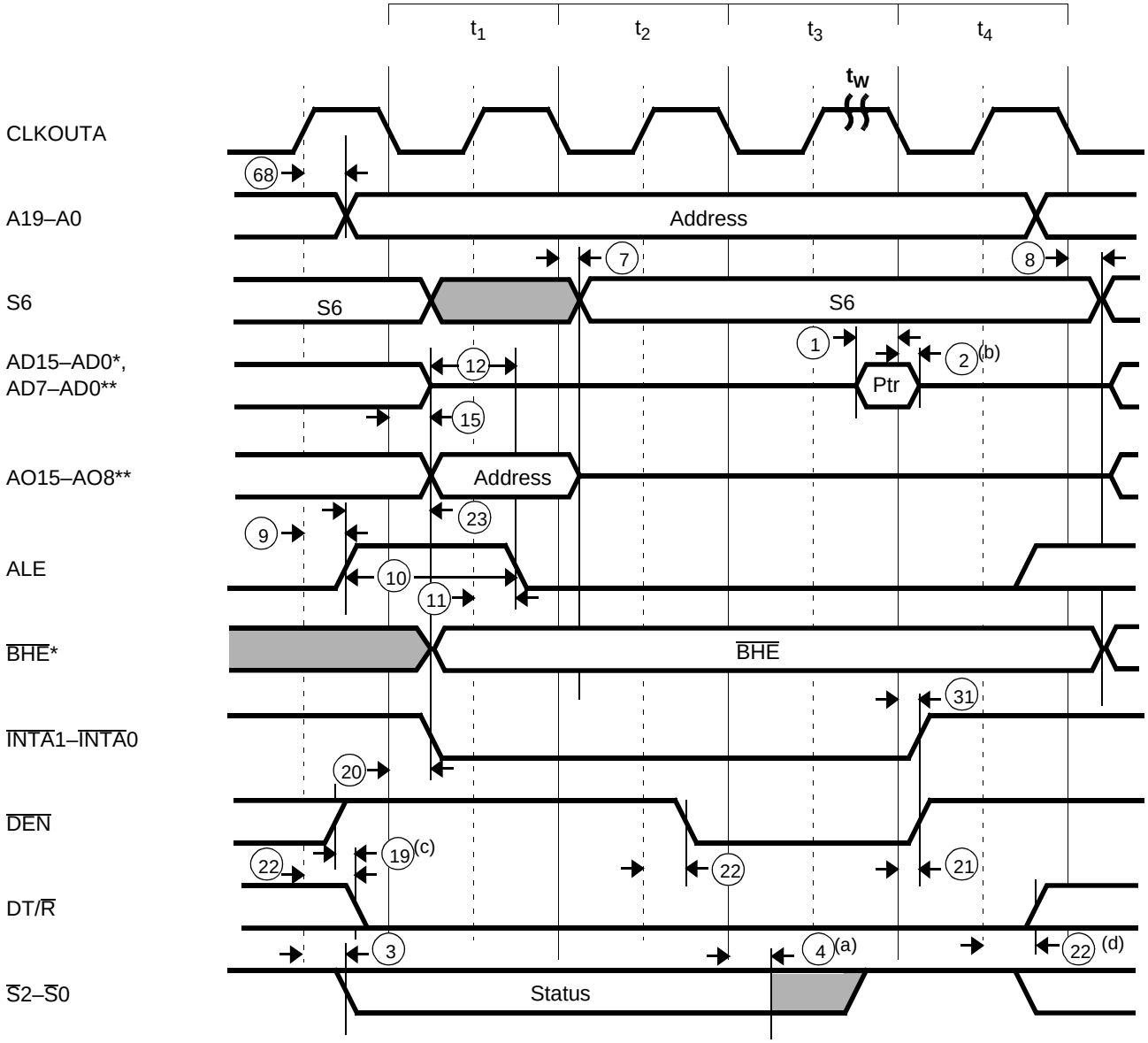
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{INTA}1$–$\overline{INTA}0$ *signals.*

c This parameter applies to the $\overline{DEN}$ and DT/$\overline{R}$ *signals.*

Interrupt Acknowledge Cycle Waveforms



Notes:

* *Am186EM microcontroller only*

** *Am188EM microcontroller only*

a *The status bits become inactive in the state preceding t_4.*

b *The data hold time lasts only until the interrupt acknowledge signal deasserts, even if the interrupt acknowledge transition occurs prior to t_{CLDX} (min).*

c *This parameter applies for an interrupt acknowledge cycle that follows a write cycle.*

d *If followed by a write cycle, this change occurs in the state preceding that write cycle.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Software Halt Cycle (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	25	0	20	ns
4	t_{CLSH}	Status Inactive Delay	0	25	0	20	ns
5	t_{CLAV}	AD Address Invalid Delay and BHE	0	25	0	20	ns
9	t_{CHLH}	ALE Active Delay		25		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=40$		$t_{CLCL}-10=30$		ns
11	t_{CHLL}	ALE Inactive Delay		25		20	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[(a)]	0		0		ns
22	t_{CHCTV}	Control Active Delay 2[(b)]	0	25	0	20	ns
68	t_{CHAV}	CLKOUTA High to A Address Invalid	0	25	0	20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$ *signal.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Software Halt Cycle (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
General Timing Responses							
3	t_{CHSV}	Status Active Delay	0	15	0	12	ns
4	t_{CLSH}	Status Inactive Delay	0	15	0	12	ns
5	t_{CLAV}	AD Address Invalid Delay and BHE	0	15	0	12	ns
9	t_{CHLH}	ALE Active Delay		15		12	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-10=20$		$t_{CLCL}-5=20$		ns
11	t_{CHLL}	ALE Inactive Delay		15		12	ns
19	t_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[(a)]	0		0		ns
22	t_{CHCTV}	Control Active Delay 2[(b)]	0	15	0	12	ns
68	t_{CHAV}	CLKOUTA High to A Address Invalid	0	15	0	10	ns

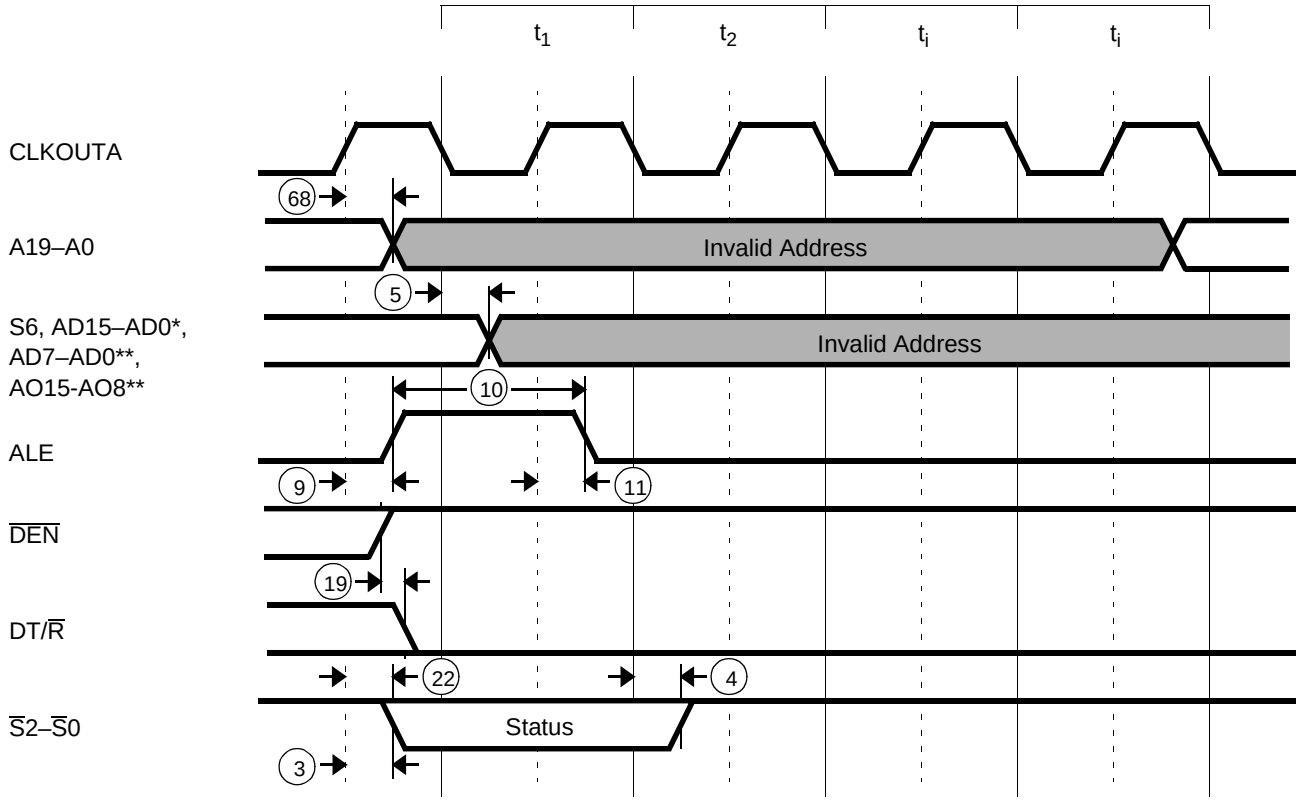
Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a Equal loading on referenced pins.

b This parameter applies to the $\overline{DEN}$ *signal.*

Software Halt Cycle Waveforms



Notes:

* *Am186EM microcontroller only*

** *Am188EM microcontroller only*

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Clock (20 MHZ and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
CLKIN Requirements							
36	t_{CKIN}	X1 Period[(a)]	50	60	40	60	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[(a)]	15		15		ns
38	t_{CHCK}	X1 High Time (1.5 V)[(a)]	15		15		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[(a)]		5		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[(a)]		5		5	ns
CLKOUT Timing							
42	t_{CLCL}	CLKOUTA Period	50		40		ns
43	t_{CLCH}	CLKOUTA Low Time (C_L=50 pF)	$0.5t_{CLCL}-2$ =23		$0.5t_{CLCL}-2$ =18		ns
44	t_{CHCL}	CLKOUTA High Time (C_L=50 pF)	$0.5t_{CLCL}-2$ =23		$0.5t_{CLCL}-2$ =18		ns
45	t_{CH1CH2}	CLKOUTA Rise Time (1.0 to 3.5 V)		3		3	ns
46	t_{CL2CL1}	CLKOUTA Fall Time (3.5 to 1.0 V)		3		3	ns
61	t_{LOCK}	Maximum PLL Lock Time		1		1	ms
69	t_{CICOA}	X1 to CLKOUTA Skew		15		15	ns
70	t_{CICOB}	X1 to CLKOUTB Skew		21		21	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} - 0.5$ V.

a The specifications for CLKIN are applicable to the normal PLL and CLKDIV2 modes.

The PLL should be used for operations from 16.667 MHz to 40 MHz. For operations below 16.667 MHz, the CLKDIV2 mode should be used.

Because the CLKDIV2 input frequency is two times the system frequency, the specifications for twice the frequency should be used for CLKDIV2 mode. For example, use the 20 MHz CLKIN specifications for 10 MHz operation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Clock (33 MHZ and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
CLKIN Requirements							
36	t_{CKIN}	X1 Period[a]	30	60	25	60	ns
37	t_{CLCK}	X1 Low Time (1.5 V)[a]	10		7.5		ns
38	t_{CHCK}	X1 High Time (1.5 V)[a]	10		7.5		ns
39	t_{CKHL}	X1 Fall Time (3.5 to 1.0 V)[a]		5		5	ns
40	t_{CKLH}	X1 Rise Time (1.0 to 3.5 V)[a]		5		5	ns
CLKOUT Timing							
42	t_{CLCL}	CLKOUTA Period	30		25		ns
43	t_{CLCH}	CLKOUTA Low Time (C_L=50 pF)	$0.5t_{CLCL}-1.5$ =13.5		$0.5t_{CLCL}-1.25$ =11.25		ns
44	t_{CHCL}	CLKOUTA High Time (C_L=50 pF)	$0.5t_{CLCL}-1.5$ =13.5		$0.5t_{CLCL}-1.25$ =11.25		ns
45	t_{CH1CH2}	CLKOUTA Rise Time (1.0 to 3.5 V)		3		3	ns
46	t_{CL2CL1}	CLKOUTA Fall Time (3.5 to 1.0 V)		3		3	ns
61	t_{LOCK}	Maximum PLL Lock Time		1		1	ms
69	t_{CICOA}	X1 to CLKOUTA Skew		15		15	ns
70	t_{CICOB}	X1 to CLKOUTB Skew		21		21	ns

Notes:

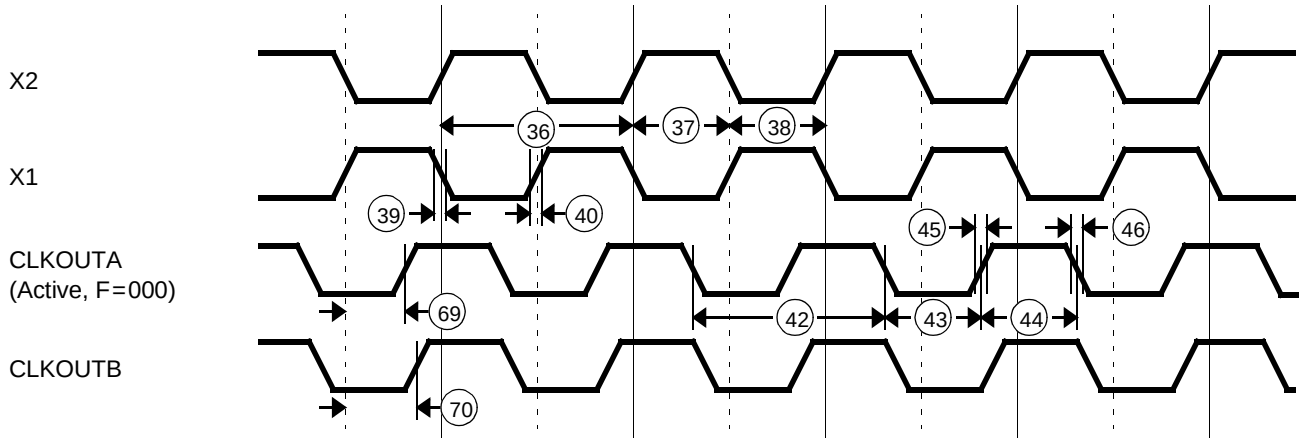
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where V_{IH} = V_{CC} – 0.5 V.

a The specifications for CLKIN are applicable to the normal PLL and CLKDIV2 modes.

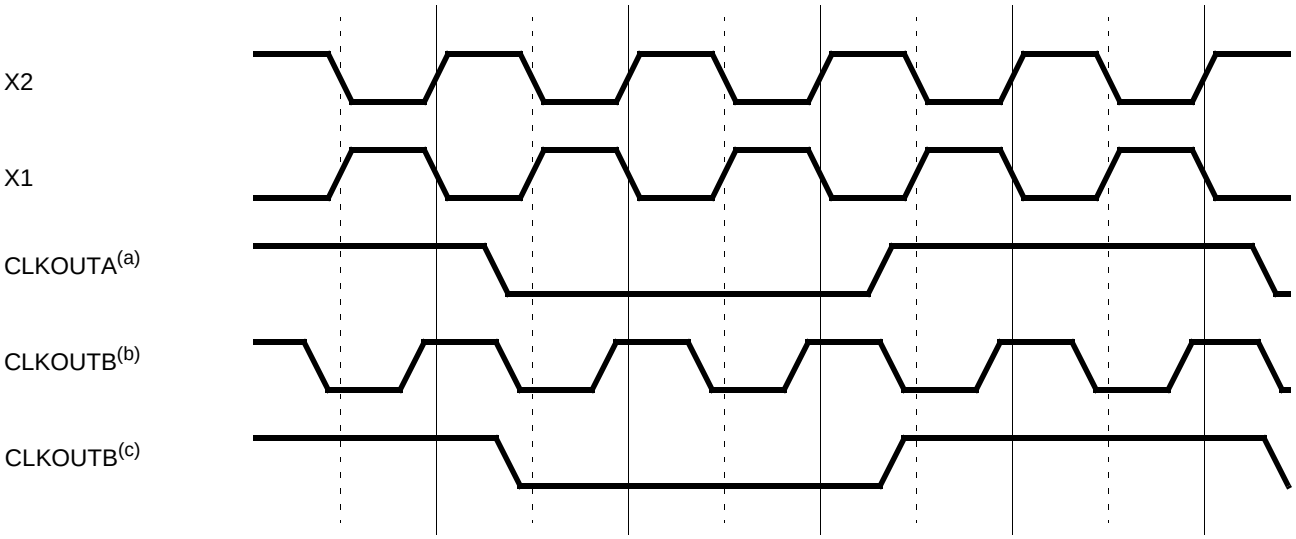
The PLL should be used for operations from 16.667 MHz to 40 MHz. For operations below 16.667 MHz, the CLKDIV2 mode should be used.

Because the CLKDIV2 input frequency is two times the system frequency, the specifications for twice the frequency should be used for CLKDIV2 mode. For example, use the 20 MHz CLKIN specifications for 10 MHz operation.

Clock Waveforms—Active Mode



Clock Waveforms—Power-Save Mode



Notes:

a The Clock Divisor Select (F2–F0) bits in the Power Save Control Register (PDCON) are set to 010 (divide by 4).

b The CLKOUTB Output Frequency (CBF) bit in the Power Save Control Register (PDCON) is set to 1.

c The CLKOUTB Output Frequency (CBF) bit in the Power Save Control Register (PDCON) is set to 0.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Ready and Peripheral Timing (20 MHz and 25 MHz)

Parameter			Preliminary 20 MHz		Preliminary 25 MHz		Unit
No.	Symbol	Description	Min	Max	Min	Max	
Ready and Peripheral Timing Requirements							
47	t_{SRYCL}	SRDY Transition Setup Time[a]	10		10		ns
48	t_{CLSRY}	SRDY Transition Hold Time[a]	3		3		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time[b]	10		10		ns
50	t_{CLARX}	ARDY Active Hold Time[a]	4		4		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	6		6		ns
52	t_{ARYLCL}	ARDY Setup Time[a]	15		15		ns
53	t_{INVCH}	Peripheral Setup Time[b]	10		10		ns
54	t_{INVCL}	DRQ Setup Time[b]	10		10		ns
Peripheral Timing Responses							
55	t_{CLTMV}	Timer Output Delay		25		20	ns

Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

a This timing must be met to guarantee proper operation.

b This timing must be met to guarantee recognition at the clock edge.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Ready and Peripheral Timing (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Ready and Peripheral Timing Requirements							
47	t_{SRYCL}	SRDY Transition Setup Time[a]	8		5		ns
48	t_{CLSRY}	SRDY Transition Hold Time[a]	3		2		ns
49	t_{ARYCH}	ARDY Resolution Transition Setup Time[b]	8		5		ns
50	t_{CLARX}	ARDY Active Hold Time[a]	4		3		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	6		5		ns
52	t_{ARYLCL}	ARDY Setup Time[a]	10		5		ns
53	t_{INVCH}	Peripheral Setup Time[b]	8		5		ns
54	t_{INVCL}	DRQ Setup Time[b]	8		5		ns
Peripheral Timing Responses							
55	t_{CLTMV}	Timer Output Delay		15		12	ns

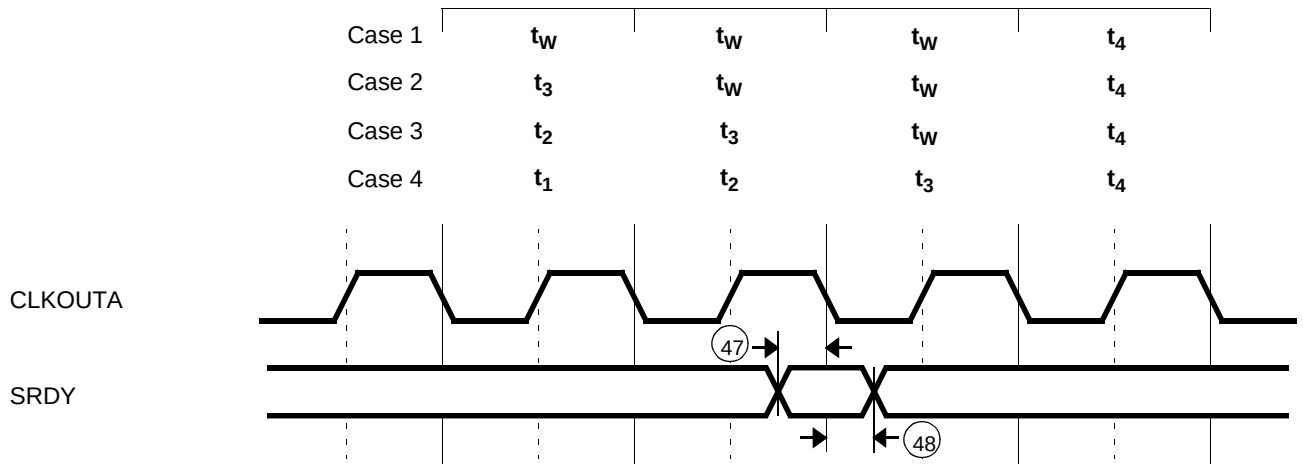
Notes:

All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

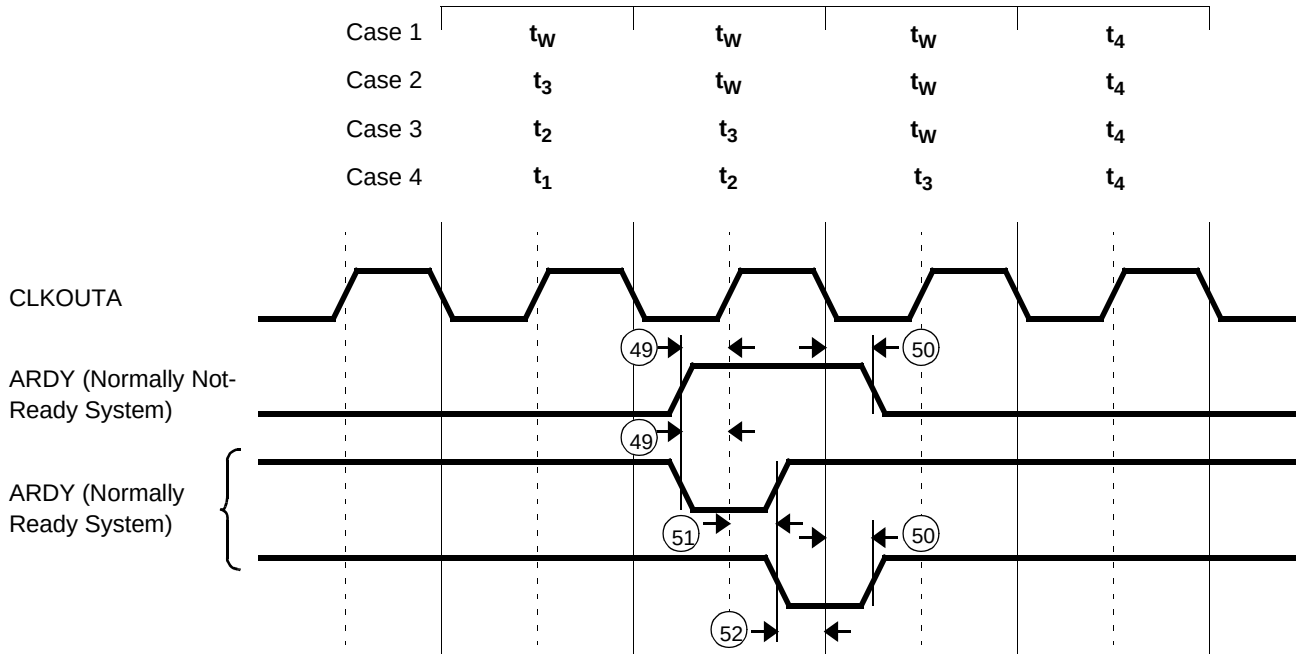
a This timing must be met to guarantee proper operation.

b This timing must be met to guarantee recognition at the clock edge.

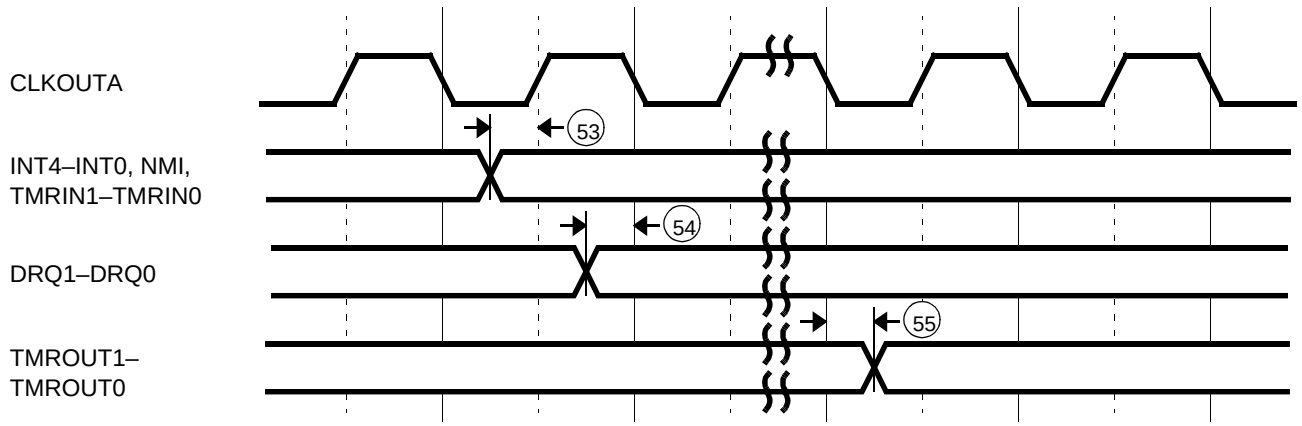
Synchronous Ready Waveforms



Asynchronous Ready Waveforms



Peripheral Waveforms



SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Reset and Bus Hold (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Reset and Bus Hold Timing Requirements							
5	t_{CLAV}	AD Address Valid Delay and BHE	0	25	0	20	ns
15	t_{CLAZ}	AD Address Float Delay	0	25	0	20	ns
57	t_{RESIN}	$\overline{RES}$ Setup Time	10		10		ns
58	t_{HVCL}	HOLD Setup[a]	10		10		ns
Reset and Bus Hold Timing Responses							
62	t_{CLHAV}	HLDA Valid Delay	0	25	0	20	ns
63	t_{CHCZ}	Command Lines Float Delay		25		20	ns
64	t_{CHCV}	Command Lines Valid Delay (after Float)		25		20	ns

Note:
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

a This timing must be met to guarantee recognition at the next clock.

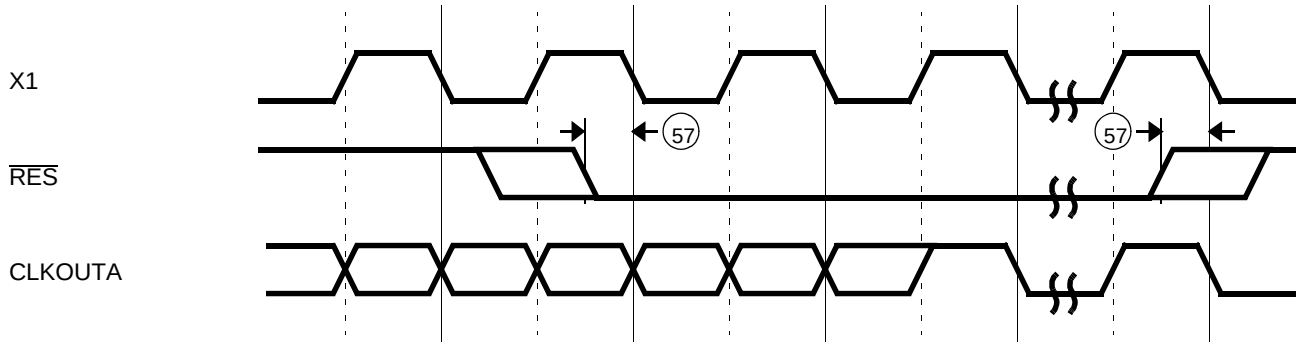
Reset and Bus Hold (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Reset and Bus Hold Timing Requirements							
5	t_{CLAV}	AD Address Valid Delay and BHE	0	15	0	12	ns
15	t_{CLAZ}	AD Address Float Delay	0	15	0	12	ns
57	t_{RESIN}	$\overline{RES}$ Setup Time	8		5		ns
58	t_{HVCL}	HOLD Setup[a]	8		5		ns
Reset and Bus Hold Timing Responses							
62	t_{CLHAV}	HLDA Valid Delay	0	15	0	12	ns
63	t_{CHCZ}	Command Lines Float Delay		15		12	ns
64	t_{CHCV}	Command Lines Valid Delay (after Float)		15		12	ns

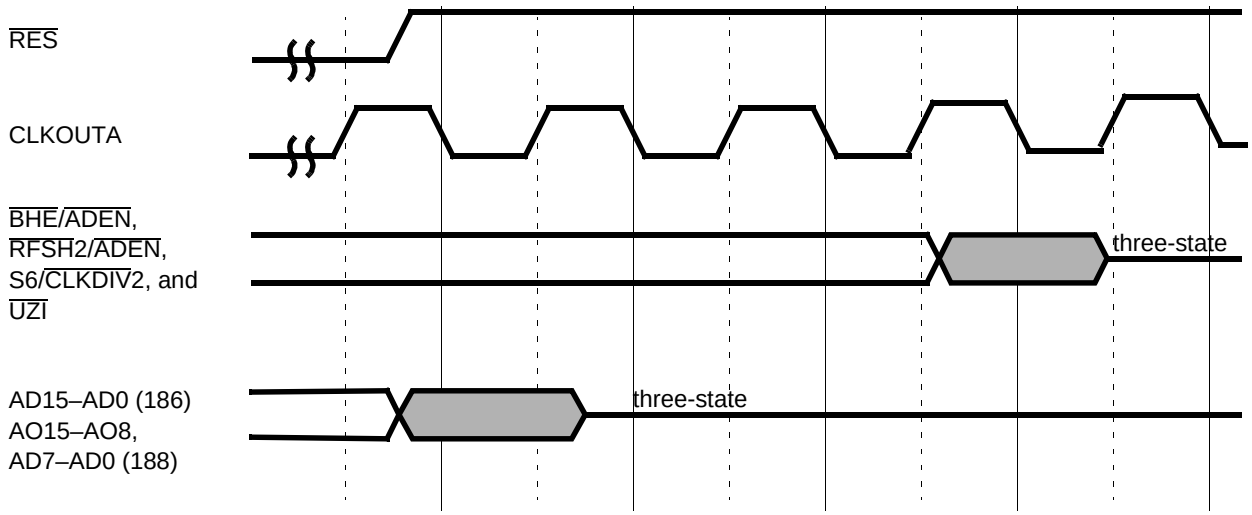
Note:
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

a This timing must be met to guarantee recognition at the next clock.

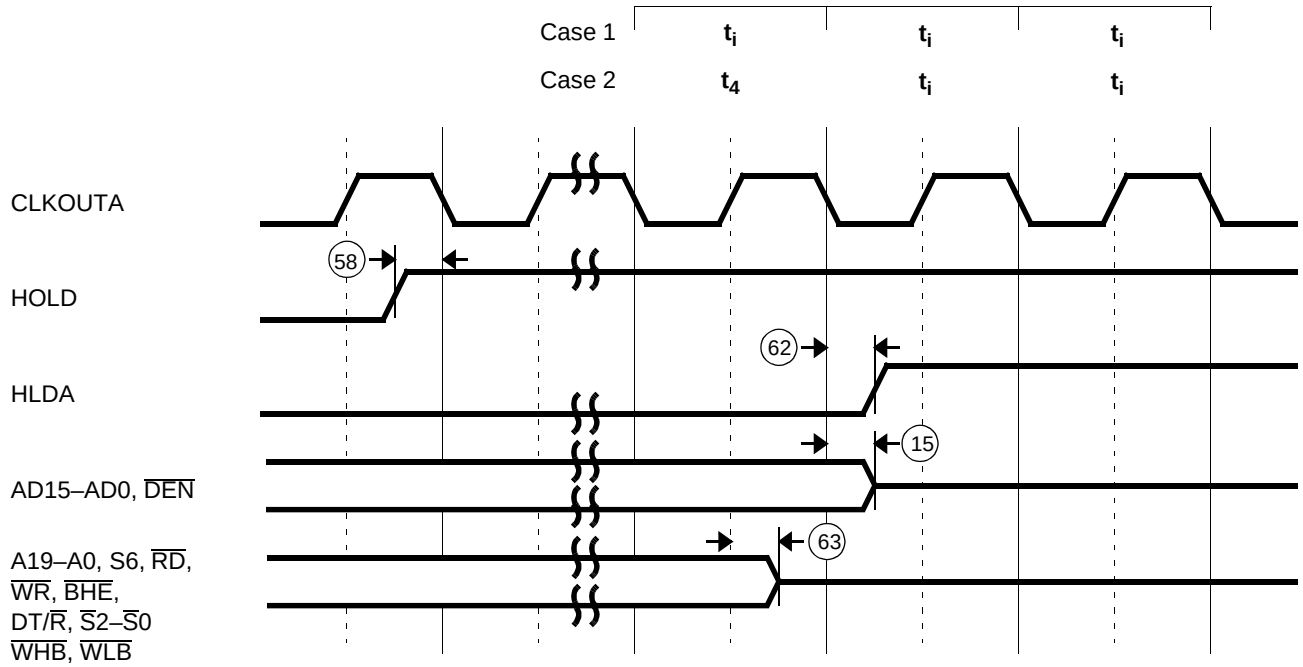
Reset Waveforms



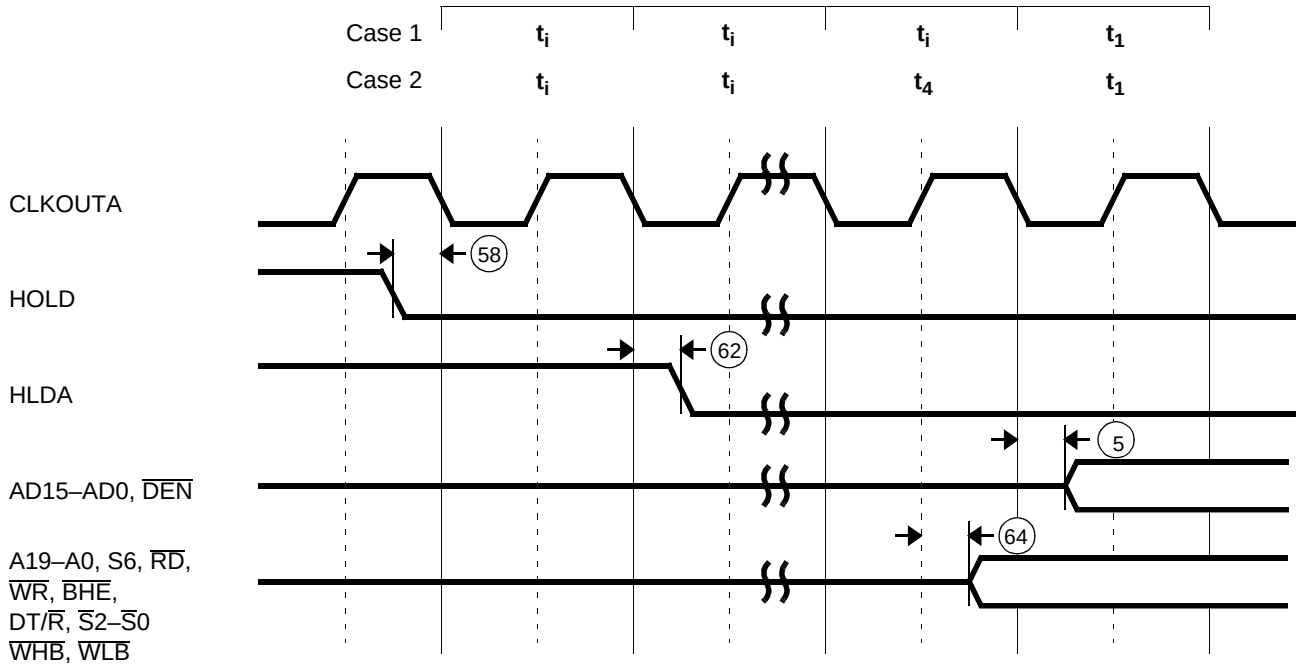
Signals Related to Reset Waveforms



Bus Hold Waveforms—Entering



Bus Hold Waveforms—Leaving



SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Synchronous Serial Interface (SSI) (20 MHz and 25 MHz)

Parameter			Preliminary				Unit
			20 MHz		25 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Synchronous Serial Port Timing Requirements							
75	t_{DVSH}	Data Valid to SCLK High	10		10		ns
77	t_{SHDX}	SCLK High to SPI Data Hold	3		3		ns
Synchronous Serial Port Timing Responses							
71	t_{CLEV}	CLKOUTA Low to SDEN Valid		25		20	ns
72	t_{CLSL}	CLKOUTA Low to SCLK Low		25		20	ns
78	t_{SLDV}	SCLK Low to Data Valid		25		20	ns

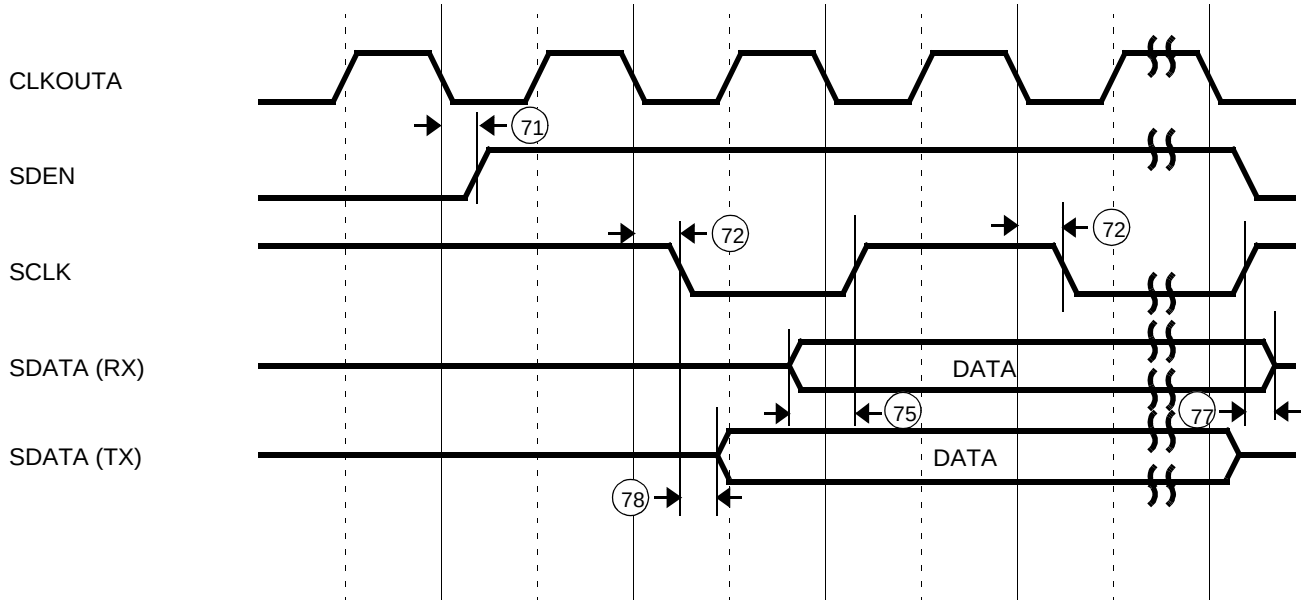
Note:
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

Synchronous Serial Interface (SSI) (33 MHz and 40 MHz)

Parameter			Preliminary				Unit
			33 MHz		40 MHz		
No.	Symbol	Description	Min	Max	Min	Max	
Synchronous Serial Port Timing Requirements							
75	t_{DVSH}	Data Valid to SCLK High	8		5		ns
77	t_{SHDX}	SCLK High to SPI Data Hold	2		2		ns
Synchronous Serial Port Timing Responses							
71	t_{CLEV}	CLKOUTA Low to SDEN Valid	0	15	0	12	ns
72	t_{CLSL}	CLKOUTA Low to SCLK Low	0	15	0	12	ns
78	t_{SLDV}	SCLK Low to Data Valid	0	15	0	12	ns

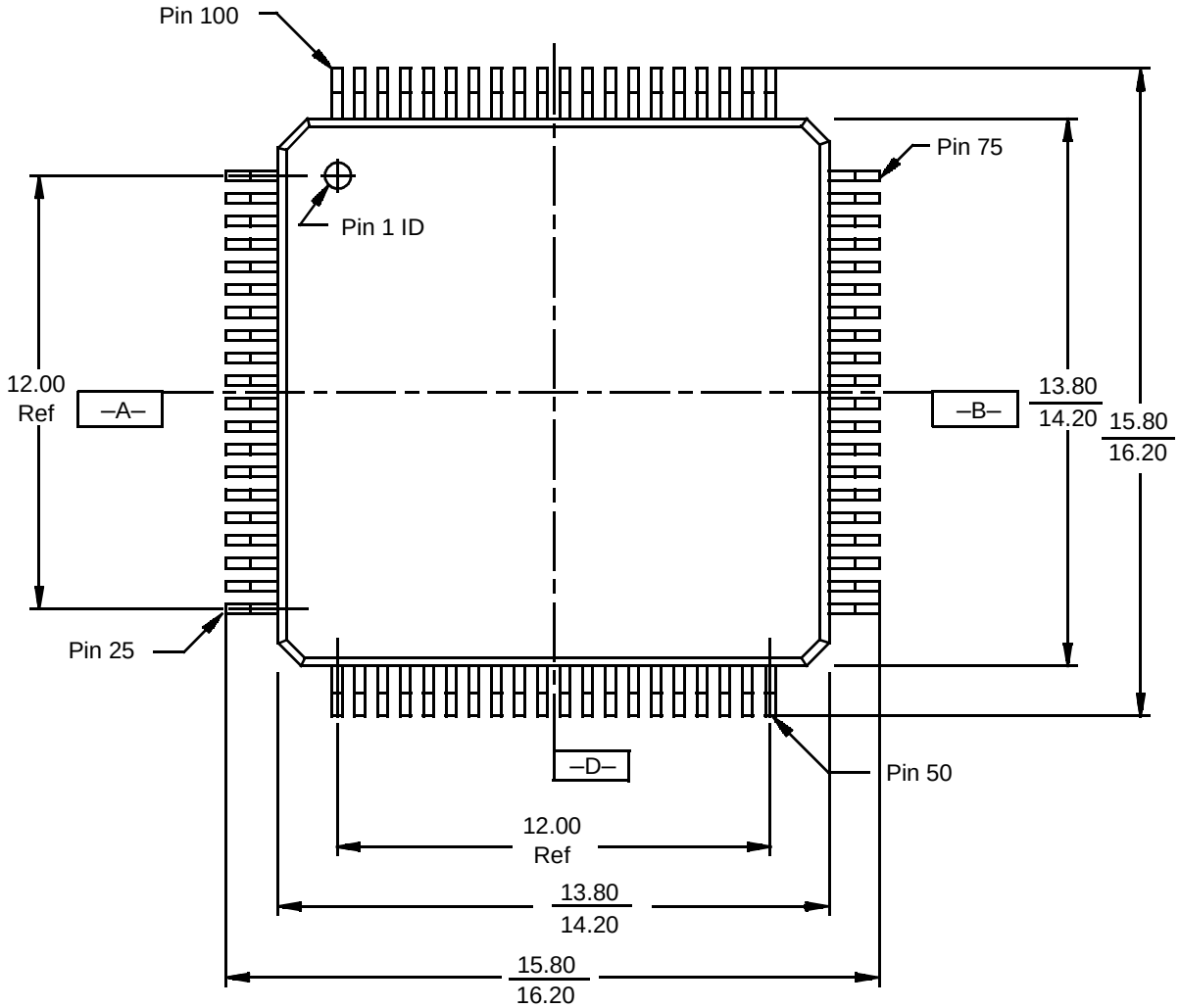
Note:
All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA unless otherwise noted. All output test conditions are with C_L = 50 pF. For switching tests, V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

Synchronous Serial Interface (SSI) Waveforms

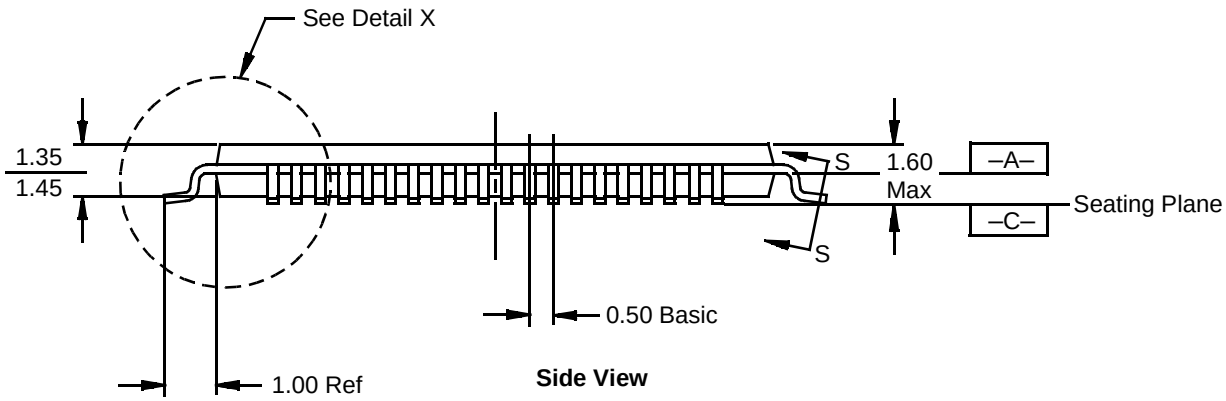


Note:
SDATA is bidirectional and used for either transmit (TX) or receive (RX). Timing is shown separately for each case.

TQFP PHYSICAL DIMENSIONS
PQL 100, Trimmed and Formed
Thin Quad Flat Pack



Top View



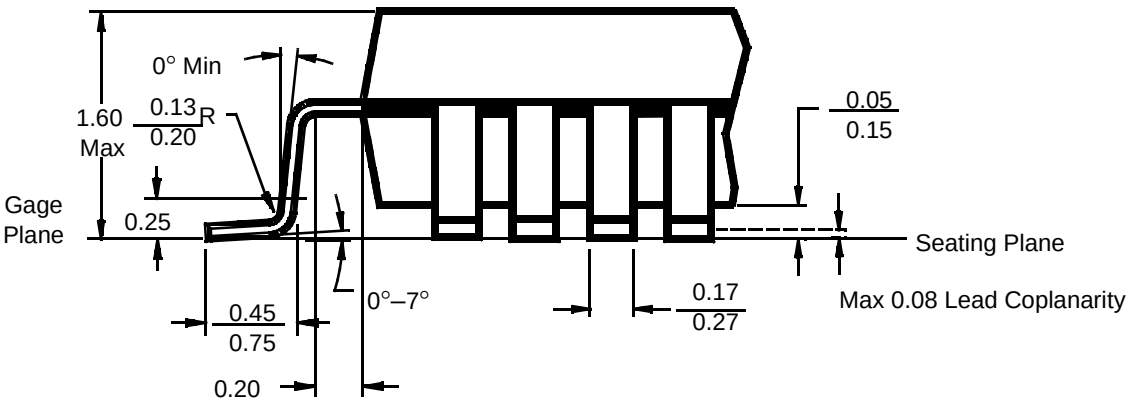
Side View

Notes:

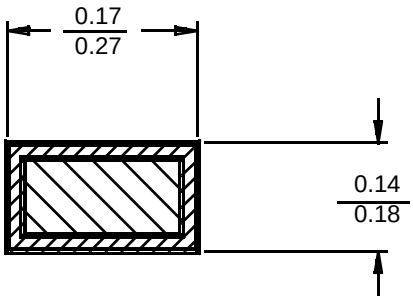
1. *All measurements are in millimeters unless otherwise noted.*
2. *Not to scale; for reference only.*

pql100
4-15-94

PQL 100 (continued)



Detail X



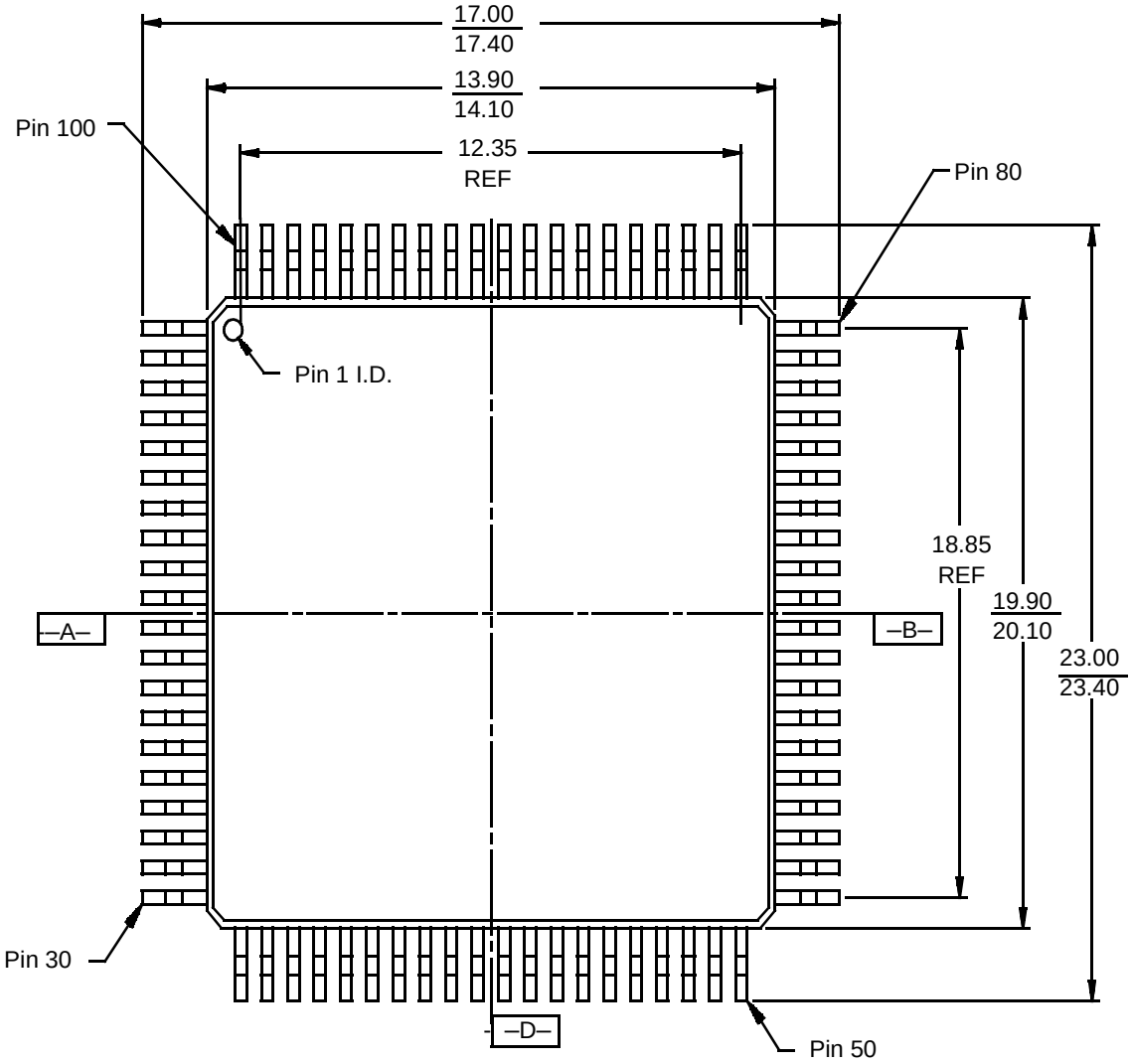
Section S-S

Notes:

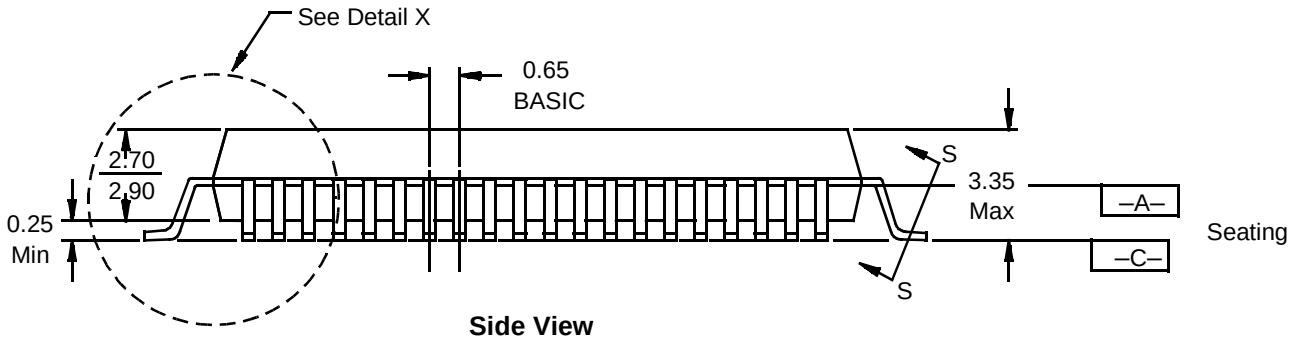
1. *All measurements are in millimeters unless otherwise noted.*
2. *Not to scale; for reference only.*

pql100
4-15-94

PQFP PHYSICAL DIMENSIONS
PQR 100, Trimmed and Formed
Plastic Quad Flat Pack



Top View



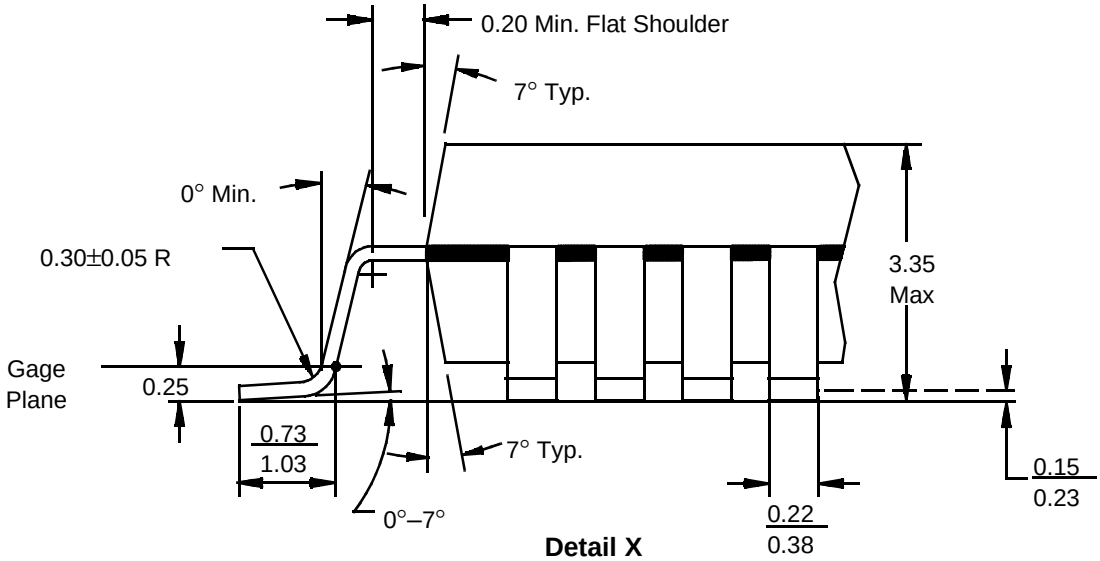
Side View

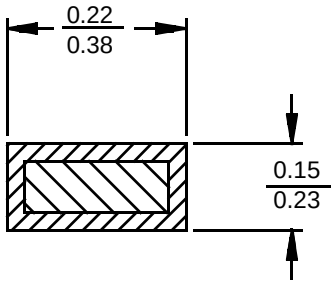
Notes:

1. *All measurements are in millimeters unless otherwise noted.*
2. *Not to scale; for reference only.*

pqr100
4-15-94

PQFP PQR 100 (continued)





Note:

Not to scale; for reference only.

pqr100
4-15-94

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