HARRIS

HI-548/883
HI-549/883

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **No Channel Interaction During Overvoltage**
- **Guaranteed R_{ON} Matching**
- **44V Maximum Power Supply**
- **Break-Before-Make Switch**
- **Analog Signal Range ..... ±15V**
- **Access Time (Max.) 1.0μs**
- **Power Dissipation (Max.) 45mW**

Applications

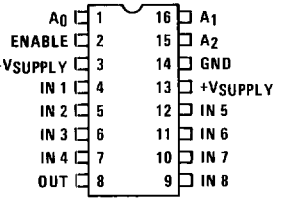
- **Data Acquisition Systems**
- **Control Systems**
- **Telemetry**

Description

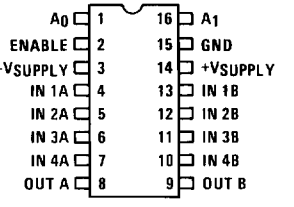
The HI-548/883 and HI-549/883 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels with ±15V supplies and digital inputs will sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-548/883 and HI-549/883 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-548/883 is a 8 channel device and the HI-549/883 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508/883 and HI-509/883 multiplexers are recommended. For further information see Application Notes 520 and 521.

Pinouts

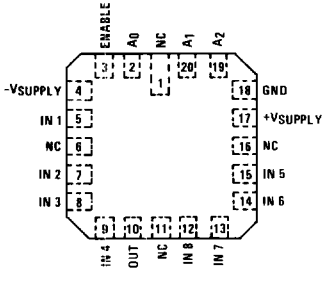
HI1-548/883 (CERAMIC DIP)
TOP VIEW



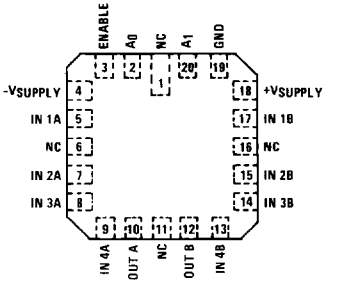
HI1-549/883 (CERAMIC DIP)
TOP VIEW



HI4-548/883 (CERAMIC LCC)
TOP VIEW

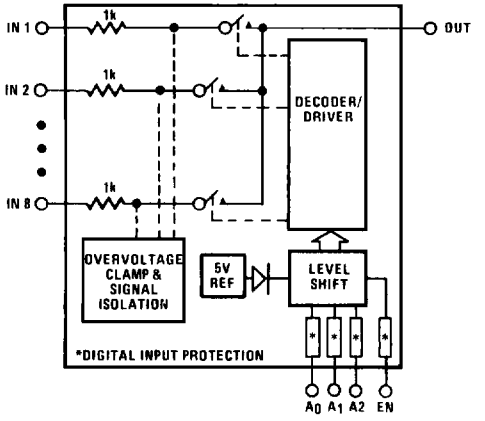


HI4-549/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

HI-548/883

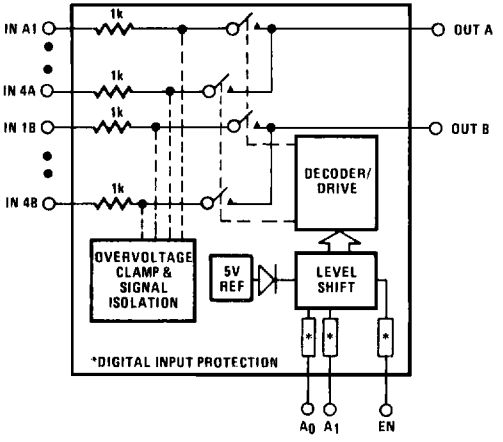


TRUTH TABLES

HI-548/883

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549/883



HI-549/883

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Absolute Maximum Ratings

Voltage Between Supply Pins 44V
$+V_{SUPPLY}$ to Ground 22V
$-V_{SUPPLY}$ to Ground 25V
Analog Input Voltage
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Digital Input Voltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first.
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% Duty Cycle Max.) 40mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... 275°C
Junction Temperature ..... +175°C
Thermal Resistance, Junction-to-Case (θjc)
Ceramic DIP Package ..... 26°C/W
Ceramic LCC Package ..... 19°C/W
Thermal Resistance, Junction-to-Ambient (θja)
Ceramic DIP Package ..... 80°C/W
Ceramic LCC Package ..... 76°C/W
Power Dissipation (at 75°C)
Ceramic DIP Package 1.25W
Ceramic LCC Package 1.32W
Power Dissipation Derating Factor (Above +75°C)
Ceramic DIP Package ..... 12.5mW/°C
Ceramic LCC Package ..... 13.2mW/°C
ESD Classification ..... ≤2000V

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Analog Input Voltage (V_S) ..... $\pm V_{SUPPLY}$
Logic Low Level (V_{AL}) ..... 0V to 0.8V
Logic High Level (V_{AH}) ..... +4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially,	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
	I_{IL}	Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V	2, 3	+125°C, -55°C	-50	+50	nA
	$-I_{S(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V	2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$+I_{D(OFF)}$	V_D = +10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-548/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-549/883	2, 3	+125°C, -55°C	-100	+100	nA
	$-I_{D(OFF)}$	V_D = -10V, V_{EN} = 0.8V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-548/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-549/883	2, 3	+125°C, -55°C	-100	+100	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$+I_{D(ON)}$	V_S = V_D = +10V	1	+25°C	-10	+10	nA
		All Unused Inputs = -10V HI-548/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-549/883	2, 3	+125°C, -55°C	-100	+100	nA
	$-I_{D(ON)}$	V_S = V_D = -10V	1	+25°C	-10	+10	nA
		All Unused Inputs = +10V HI-548/883	2, 3	+125°C, -55°C	-200	+200	nA
		HI-549/883	2, 3	+125°C, -55°C	-100	+100	nA
Overvoltage Protected, Leakage Current Into the Drain Terminal of an "OFF" Switch	$I_{D(OFF)}$ Overvoltage	V_S = 33V, V_D = 0V, V_{EN} = 0.8V V_S applied at ≤25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	µA
		V_S = -33V, V_D = 0V, V_{EN} = 0.8V V_S applied at ≤25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	µA
Positive Supply Current	I(+)	V_A = 0V, V_{EN} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Negative Supply Current	I(-)	V_A = 0V, V_{EN} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Standby Positive Supply Current	$+I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Standby Negative Supply Current	$-I_{SBY}$	V_A = 0V, V_{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Switch "ON" Resistance	$+R_{DS1}$	V_S = 10V	1	+25°C		1500	Ω
		I_D = 100µA	2, 3	+125°C, -55°C		1800	Ω
	$-R_{DS1}$	V_S = -10V	1	+25°C		1500	Ω
		I_D = -100µA	2, 3	+125°C, -55°C		1800	Ω
Logic Level Voltage	V_{AL}	Note 1, 2	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	V_{AH}	Note 1, 2	1, 2, 3	+25°C, +125°C, -55°C	4.0		V
Difference in switch "ON" Resistance Between Channels	$+\Delta R_{DS1}$	$\frac{(+R_{DS1}MAX) - (+R_{DS1}MIN) \times 100}{+R_{DS1}AVE}$	1	+25°C		7	%
	$-\Delta R_{DS1}$	$\frac{(-R_{DS1}MAX) - (-R_{DS1}MIN) \times 100}{-R_{DS1}AVE}$	1	+25°C		7	%

NOTES: 1. Used for forcing conditions for all DC tests unless otherwise specified.
2. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 1kΩ, C_L = 12.5pF	9	+25°C	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 14pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 1kΩ, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
	$t_{OFF(EN)}$	R_L = 1kΩ, C_L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	C_A	V+ = V- = 0V, f = 1MHz	3	+25°C		10	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V, f = 1MHz HI-548/883	3	+25°C		45	pF
		HI-549/883	3	+25°C		25	pF
Capacitance Input Switch	C_{IS}	V+ = V- = 0V, f = 1MHz	3	+25°C		15	pF
Charge Transfer Error	V_{CTE}	V_S = GND, V_{GEN} = 0V to 5V, f = 200kHz	3	+25°C		10	mV
Off Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz	3, 4	+25°C	-50		dB

NOTES: 3. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

4. Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

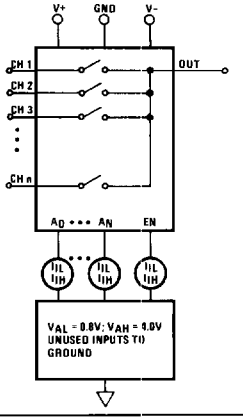
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

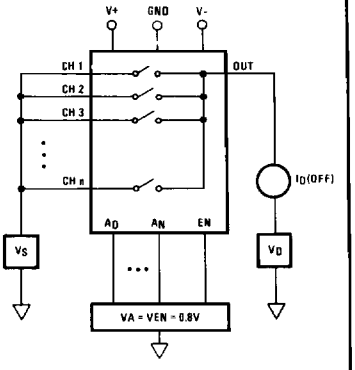
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

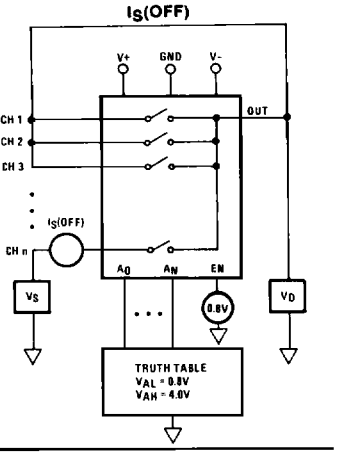
INPUT LEAKAGE CURRENT



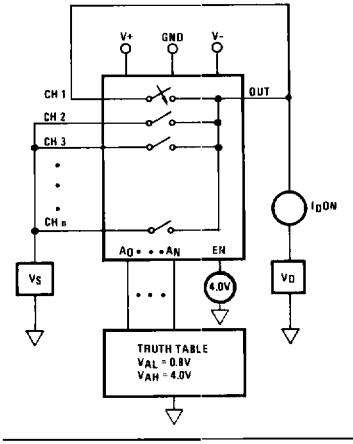
ID(OFF)



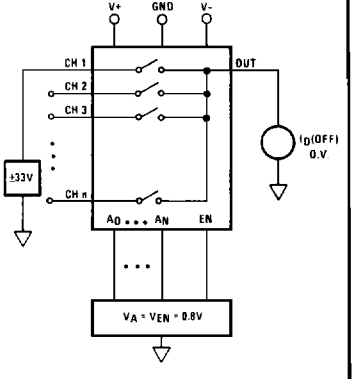
IS(OFF)



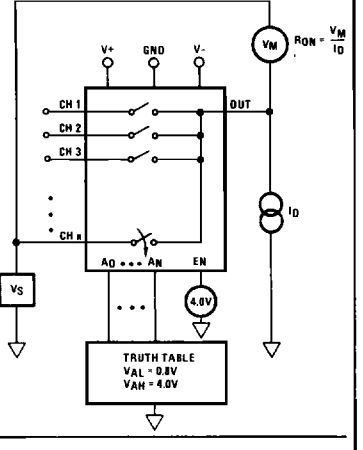
ID(ON)



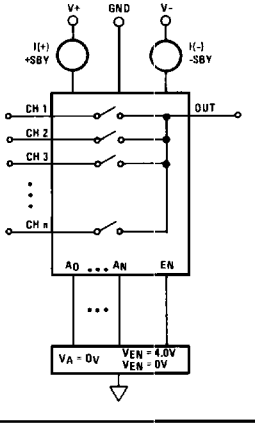
ID(OFF) OVERVOLTAGE



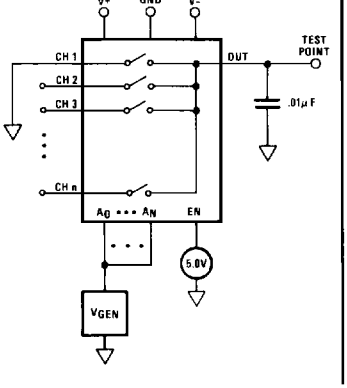
RDS



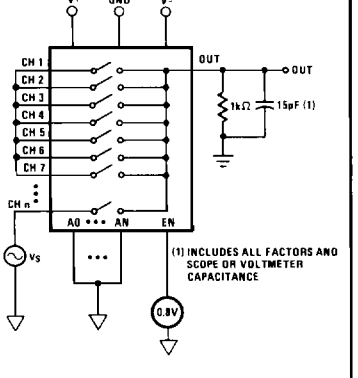
SUPPLY CURRENTS



CHARGE TRANSFER ERROR

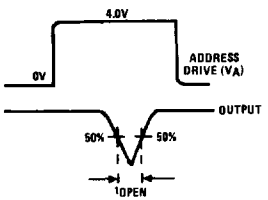


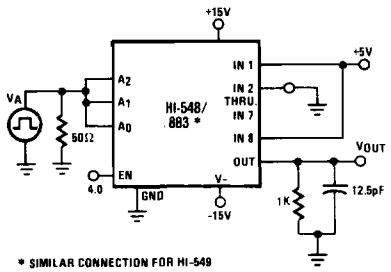
OFF CHANNEL ISOLATION



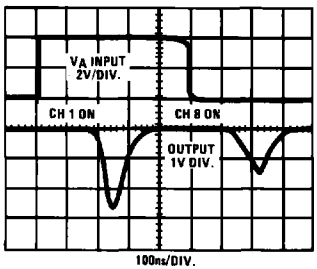
Switching Waveforms

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

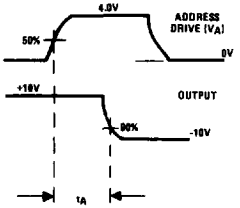


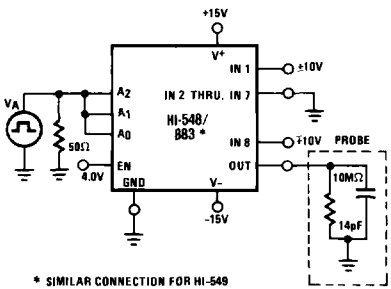


BREAK-BEFORE-MAKE DELAY (t_{OPEN})

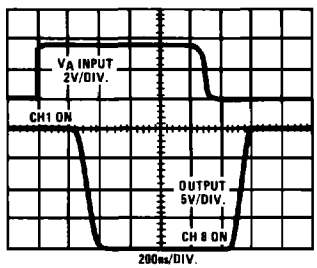


ACCESS TIME

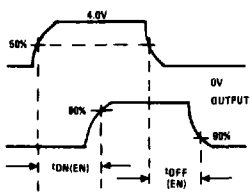




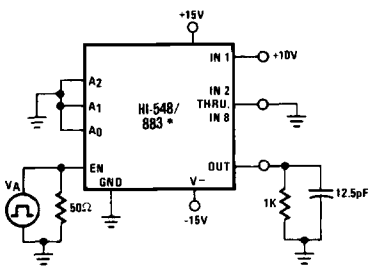
ACCESS TIME



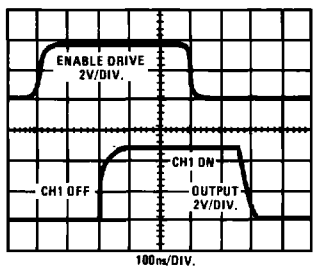
ENABLE DRIVE



ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

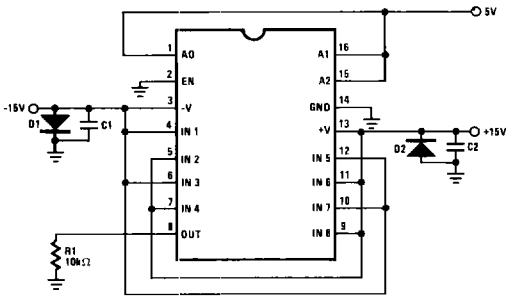


ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



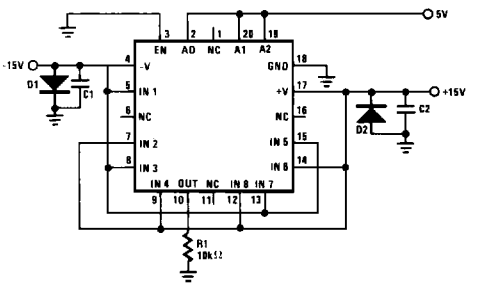
Burn-In Circuits

HI-548/883 CERAMIC DIP



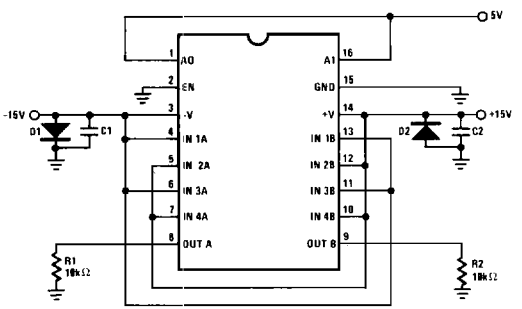
NOTES:
R1 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = 0.01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-548/883 CERAMIC LCC



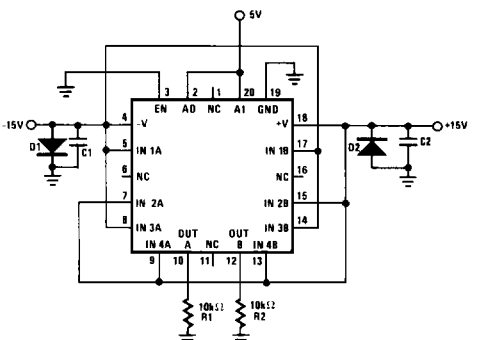
NOTES:
R1 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = .01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

HI-549/883 CERAMIC DIP



NOTES:
R1, R2 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = 0.01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

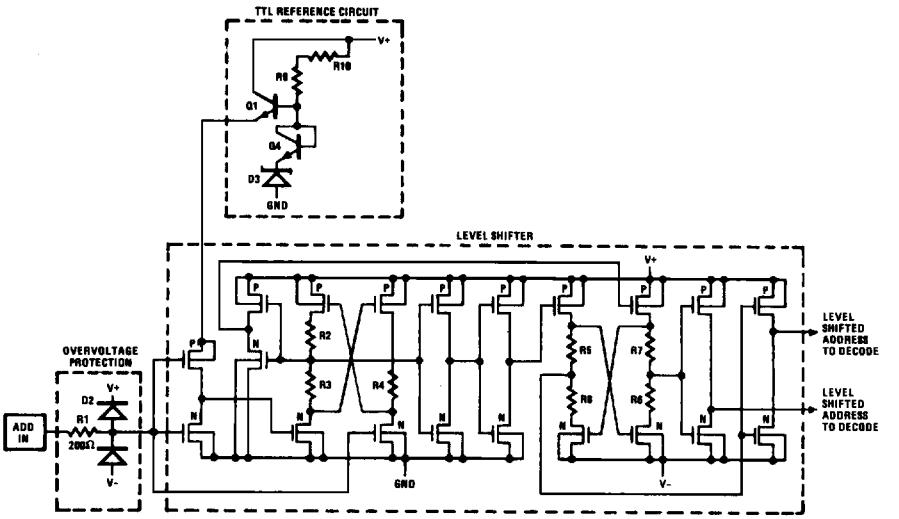
HI-549/883 CERAMIC LCC



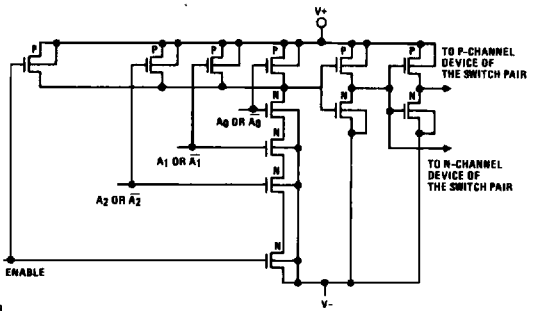
NOTES:
R1, R2 = 10kΩ ± 5% 1/2 or 1/4W (per socket)
C1, C2 = 0.01μF (per socket) or 0.1μF (per row)
D1, D2 = IN4002 (or equivalent) (per board)

Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVER SHIFTER

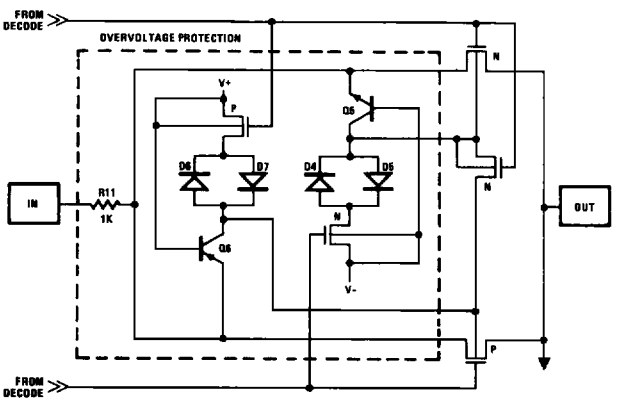


ADDRESS DECODER



Delete A_2 or $\overline{A}_2$ input for HI-549/883

MULTIPLEX SWITCH



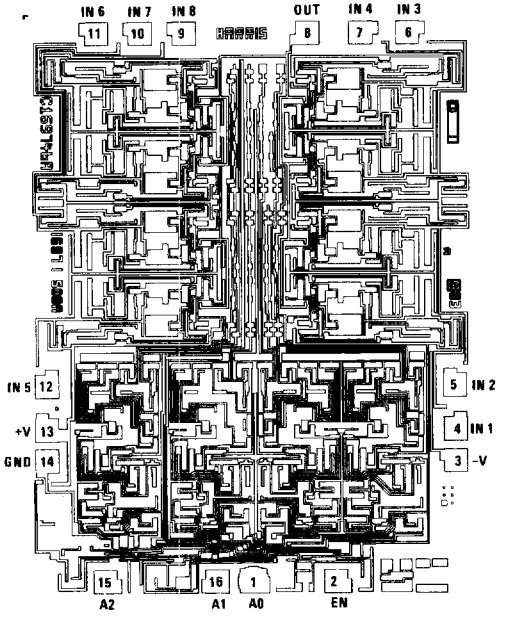
Die Characteristics

DIE DIMENSIONS: 83 x 108 x 19 mils
METALLIZATION
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ
WORST CASE CURRENT DENSITY: 1.4×10^5 A/cm^2

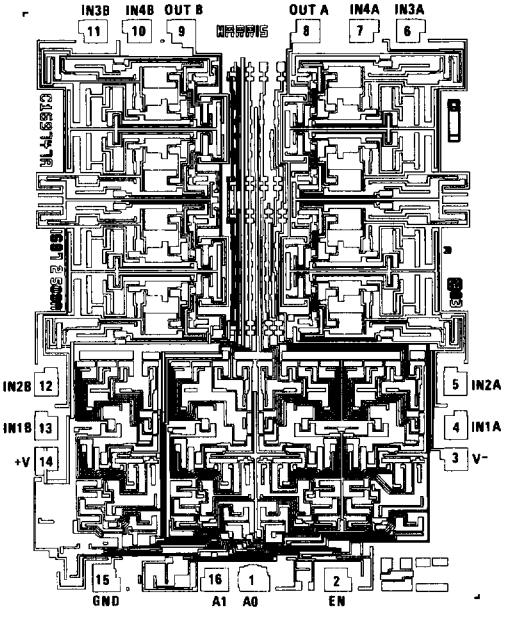
TRANSISTOR COUNT:
HI-548/883 253
HI-549/883 253
PROCESS: CMOS-DI
DIE ATTACH
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-548/883



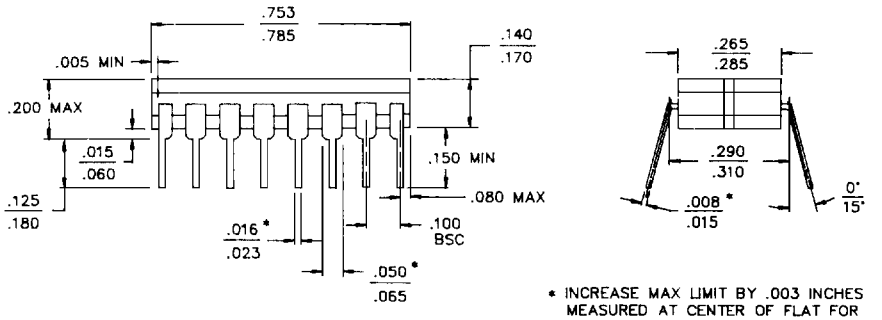
HI-549/883



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only

Packaging†

16 PIN CERAMIC DIP

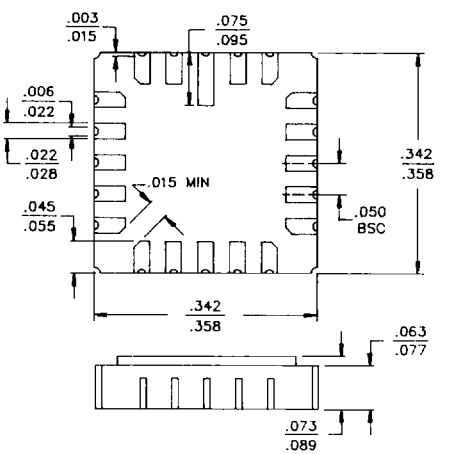


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are Min/Max. Dimensions are in inches.

† MIL-M-38510 Compliant Materials, Finishes & Dimensions.

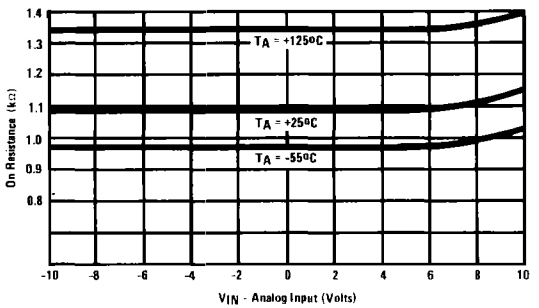
HI-548
HI-549

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

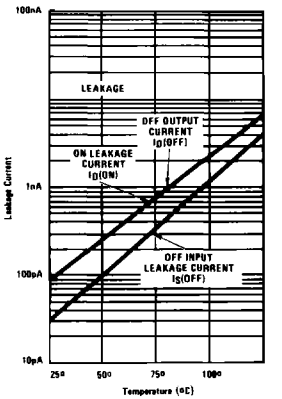
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V

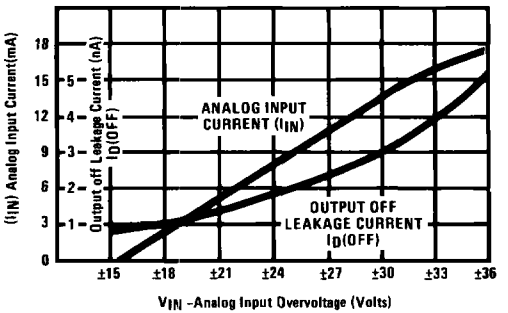
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



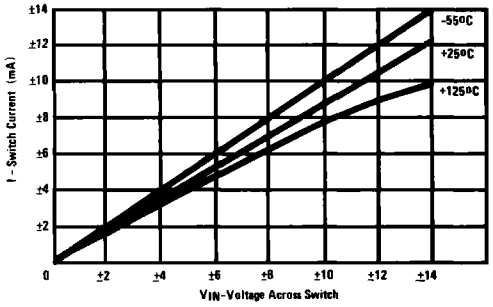
LEAKAGE CURRENT vs. TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



ON CHANNEL CURRENT vs. VOLTAGE



SUPPLY CURRENT vs. TOGGLE FREQUENCY