AK134/135

2B+D TCM Integrated Quad Transceiver

Features

- Completely integrated quadruple baseband transceiver for 2-wire twisted pair applications
- 2B+1D+1M channels of PCM-BUS framed data, using time compression multiplexing
- Data rate: 160kbps (2B+1D+1M)
- Loop Coverage, AK134: 1 km (3300 feet) / AK135: 2 km (6500 feet)
- Pin compatible between AK134 and AK135
- Low amplitude pulse-shaped Alternate Mark Inversion (AMI) coding for reduced spectral radiation
- Differential receiver architecture for highly reliable data recovery
- Bit error rate less than 10^{-7}
- PCM and Microprocessor ports for combined port operation
- Operates on a single +5 V power supply and draws only 360 mW active power (typ)
- Pakage: 44 pin QFP

Block Diagram

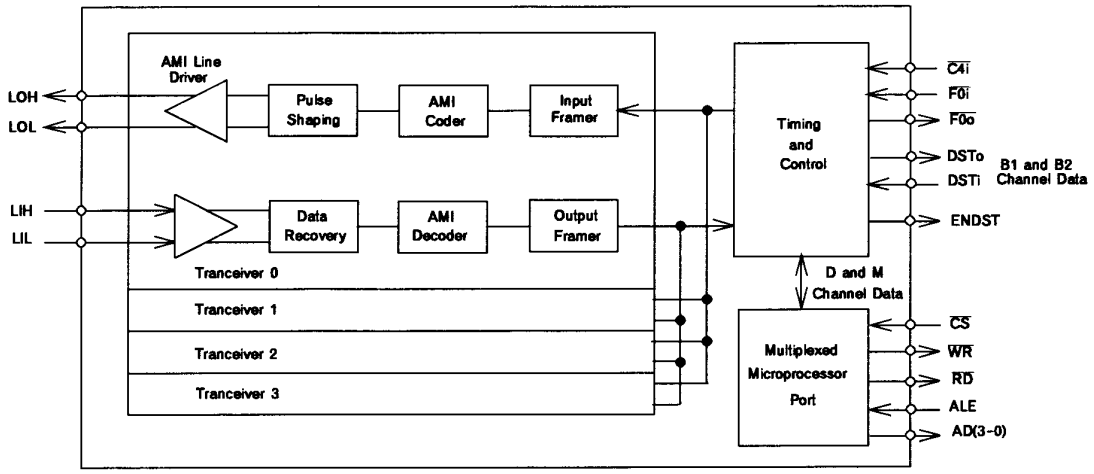


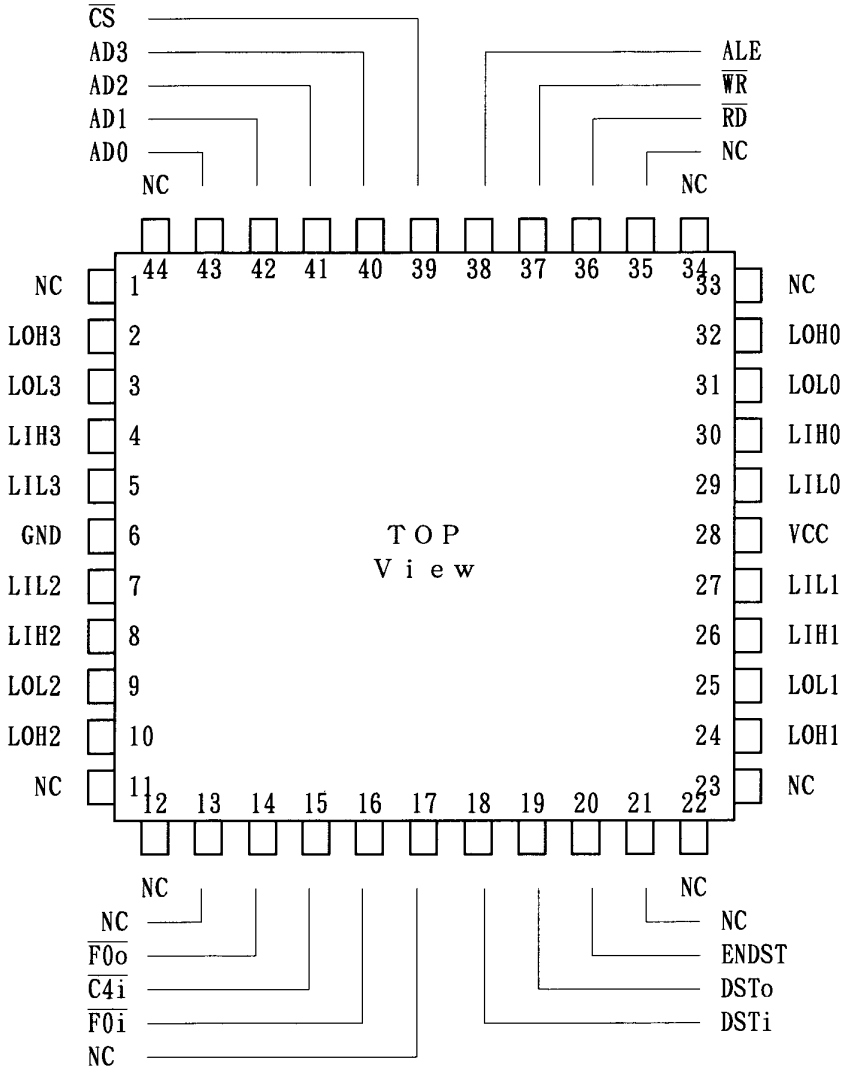
Fig-1 Block Diagram

General Description

The AK134/135 is a fully integrated quad transceiver for high-speed data transmission over unshielded twisted-pair subscriber loops. The device transmits at 160 kbps (line rate 512 kbps) over a single twisted pair wire, using a Time Compression Multiplex (TCM) transmission scheme.

The AK134/135 provides transparent, burst mode transmission of 2B+1D+1M channels in subscriber loop applications, typically KTS or PBX systems. It operates up to 1 km (AK130) / 2 km (AK131) on 0.5mm (24AWG) LOCAP station cable. The AK134/135 is designed for use in Line Termination (LT) (Master-only) applications. It uses a 2048 kbps synchronous serial PCM-BUS.

■ Pin assignment



■ Ordering information

AK134-VQ	0 ~ 70 ℃	44 pin QFP
AK135-VQ	0 ~ 70 ℃	44 pin QFP

Pin / Function

Pin #	Symbol	I/O	Function
1	NC	-	No connection.
2 3	LOH3 LOL3	O O	Differential output #3. Idle level at these outputs is VCC/2. A positive mark results in a voltage of VCC/2 + 1.25 V at LOH and VCC/2 - 1.25 V at LOL.
4 5	LIH3 LIL3	I I	Differential input #3. These inputs are insensitive to the polarity of the receive signal.
6	GND	-	Ground.
7 8	LIL2 LIH2	I I	Differential input #2.
9 10	LOL2 LOH2	O O	Differential output #2.
11 12 13	NC NC NC	- - -	No connection.
14	$\overline{FO}$o	O	Frame Pulse Out. An 8 kHz, 244-ns wide active low pulse indicating the end of the device's active channel time on the PCM-BUS. Used to daisy-chain up to 4 AK134/135 on the same PCM-BUS
15	$\overline{C4}$i	I	4.096 MHz master clock input. PCM-BUS clock used to established bit-cell boundaries for the serial bus.
16	$\overline{FO}$i	I	Frame Pulse In. An 8 kHz, 244-ns wide active low pulse indicating the beginning of the device's active time on the PCM-BUS.
17	NC	-	No connection.
18	DSTi	I	A 2.048 Mbps serial PCM-BUS input.
19	DSTo	O	A 2.048 Mbps serial PCM-BUS output.
20	ENDST	O	External Driver Enable. An active high enable signal output for external line drivers.
21 22 23	NC NC NC	- - -	No connection.
24 25	LOH1 LOL1	O O	Differential output #1.
26 27	LIH1 LIL1	I I	Differential input #1.
28	VCC	-	+5 V power supply input.
29 30	LIL0 LIH0	I I	Differential input #0.
31 32	LOL0 LOH0	O O	Differential output #0.
33 34 35	NC NC NC	- - -	No connection.
36	$\overline{RD}$	I	Active low Read signal.
37	$\overline{WR}$	I	Active low Write signal.
38	ALE	I	Address Latch Enable. The address is latched by the falling edge of ALE.

Pin #	Symbol	I/O	Function
39	$\overline{CS}$	I	Chip Select. Active low Chip Select signal for the microprocessor port.
40	AD3	I/O	Address/Data Bus lines. Bidirectional multiplexed Address/ Data Bus.
41	AD2	I/O	
42	AD1	I/O	
43	AD0	I/O	
44	NC	-	No connection.

Absolute Maximum Ratings

Parameter	Symbol	min	max	units
Supply Voltage	Vcc	-0.3	7.0	V
Voltage on any I/O pin	$V_{I/O}$	GND - 0.3	V_{CC} + 0.3	V
Current on any I/O pin	$I_{I/O}$	-50	50	mA
Package power dissipation	P_D		600	mW
Storage Temperature	Tstg	-65	150	℃

Warning: **Exceeding absolute maximum ratings may cause permanent damage. Normal operation is not guaranteed at these extremes.**

Operating Conditions

Voltages are with respect to ground (GND) unless otherwise stated.
Typical figures are at 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Parameter	Symbol	min	typ	max	unit	Condition
Supply Voltage	Vcc	4.75	5	5.25	V	
Operating Temperature	T_{OP}	0		70	℃	

■ DC Electrical Characteristics

– Clocked operation over recommended temperature ranges and power supply voltages.

Parameter	Symbol	min	typ	max	unit	Condition
Supply current(Transmitting a space)	I_{CC}	-	-	58	mA	15pF load
Supply current(Transmitting a mark)	I_{CC}	-	-	72	mA	15pF load
Input high voltage	V_{IH}	2.0	-	-	V	Note-2
Input low voltage	V_{IL}	-	-	0.8	V	Note-2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH}=40μA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL}=1.6mA
Output high voltage	V_{OH}	4.6	-	-	V	I_{OH}=10μA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL}=10μA
Output high current	I_{OH}	-	-	40	μA	V_{OH}=2.4V
Output low current	I_{OL}	-	-	1.6	mA	V_{OL}=0.4V
Input leakage current (Note-1)	I_{LL}	-	±1	±10	μA	Note-3

Note-1: And output buffer leakage, when tristated.
Note-2: Digital input
Note-3: Input between VCC and GND

■ AC Electrical Characteristics – Clock timing

Parameter	Symbol	min	typ	max	unit	Condition
Operating frequency	f_C	-	4.096	-	MHz	
Frequency tolerance	T_C	-	-	±1000	ppm	
Clock duty cycle		40	50	60	%	

■ Analog Characteristics

Parameter	Symbol	min	typ	max	unit	Condition
Transmit differential amplitude	V_{AO}	2.2	2.5	2.8	Vp	RL=800Ω
Transmit common mode offset	XCMR	0	-	±75	mV	Note-1
Transmit pulse output rise/fall time	T_{DRF}	-	-	400	ns	
Receive differential input amplitude	V_{AI}	0.35	-	1.5	V	

Note-1: Relative to VCC/2

■ AC Electrical Characteristics: PCM-BUS Timing (See Fig-2)

Timing figures are over recommended temperature and power supply voltages.

Parameter	Symbol	min	typ	max	unit	Condition
$\overline{F0i}$ input pulse width	t_{FPW}	-	244	-	ns	
Frame pulse ($\overline{F0i}$) setup time	t_{FPS}	50	-	-	ns	
Frame pulse ($\overline{F0i}$) hold time	t_{FPH}	50	-	-	ns	
$\overline{C4i}$ input clock period	t_{P4o}	-	244	-	ns	
$\overline{C4i}$ pulse width high or low	t_{C4W}	-	122	-	ns	
$\overline{C4i}$ transition time	t_{C4T}	-	-	11	ns	
$\overline{F0o}$ delay	t_{DFD}	-	20	-	ns	15pF Load
$\overline{F0o}$ pulse width	t_{DFW}	-	244	-	ns	15pF Load
Serial input setup time	t_{SIS}	30	-	-	ns	
Serial input hold time	t_{SIH}	50	-	-	ns	
Serial output delay	t_{SOD}	-	-	125	ns	15pF Load
$\overline{C4i}$ to ENDST delay	t_{CE}	-	-	125	ns	15pF Load

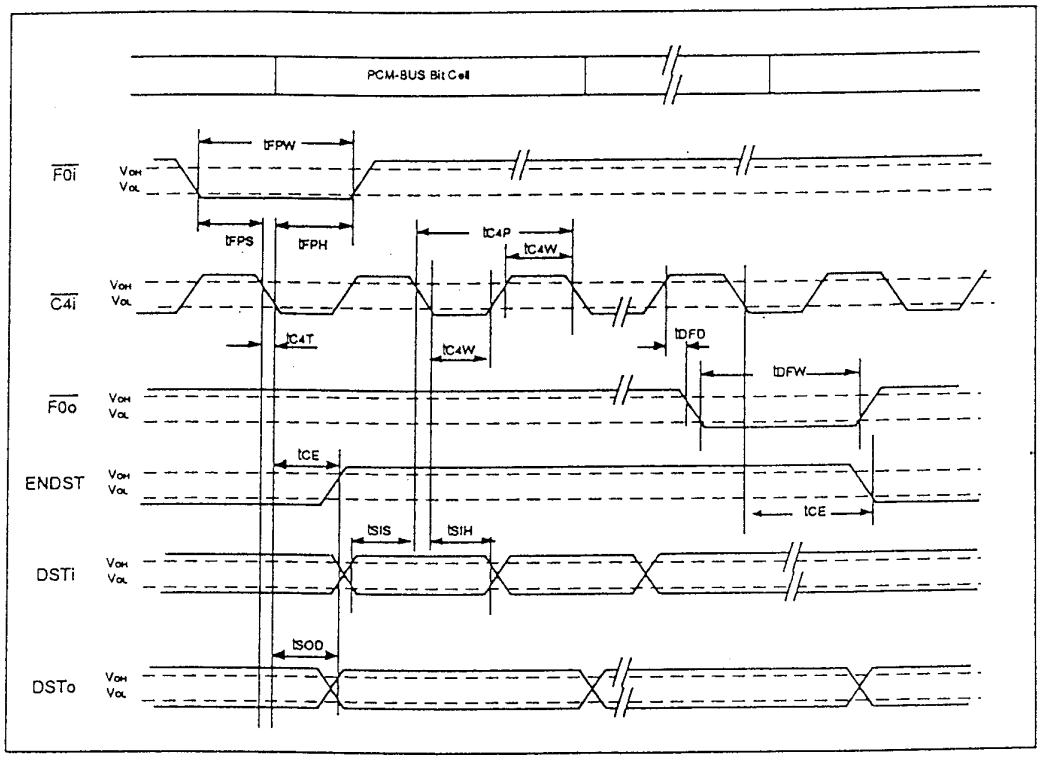


Fig-2 PCM-BUS Timing

■ AC Electrical Characteristics: Microprocessor Port Timing (See Fig-3 and Fig-4)

Timing figures are over recommended temperature and power supply voltages.

Parameter	Symbol	Min	Max	Unit	Condition
ALE Cycle time	Tlhlh	287	-	ns	
ALE pulse width	Tlhll	25	-	ns	
Address setup / valid before ALE	Tavll	25	-	ns	
Address hold after ALE	Tllax	10	-	ns	
$\overline{CS}$ Setup before $\overline{RD}$	Tclrl	25	-	ns	
ALE to $\overline{RD}$	Tllrl	40	-	ns	
Data hold after read	Trhdx	0	-	ns	
$\overline{CS}$ hold after read	Trhch	0	-	ns	
Data float after read	Trhdz	-	97	ns	
$\overline{RD}$ to ALE	Trhlh	0	-	ns	
$\overline{RD}$ to valid data	Trldv	-	125	ns	
$\overline{CS}$ setup before $\overline{WR}$	Tclwl	25	-	ns	
Data setup	Tdvwh	40	-	ns	
ALE to $\overline{WR}$	Tllwl	40	-	ns	
$\overline{CS}$ hold after write	Twhch	0	-	ns	
Data hold after write	Twhdx	25	-	ns	
$\overline{WR}$ to ALE	Twhlh	0	-	ns	
$\overline{WR}$ pulse width	Twlwh	55	-	ns	

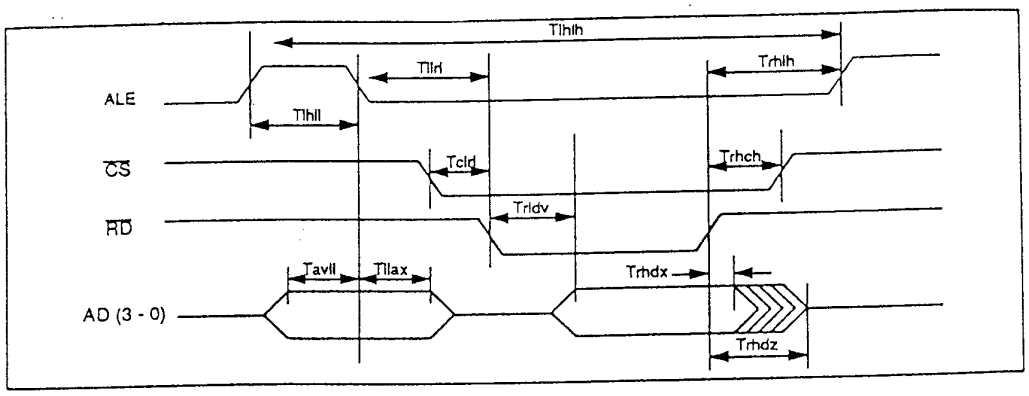


Fig-3 Microprocessor Port Read Cycle Timing

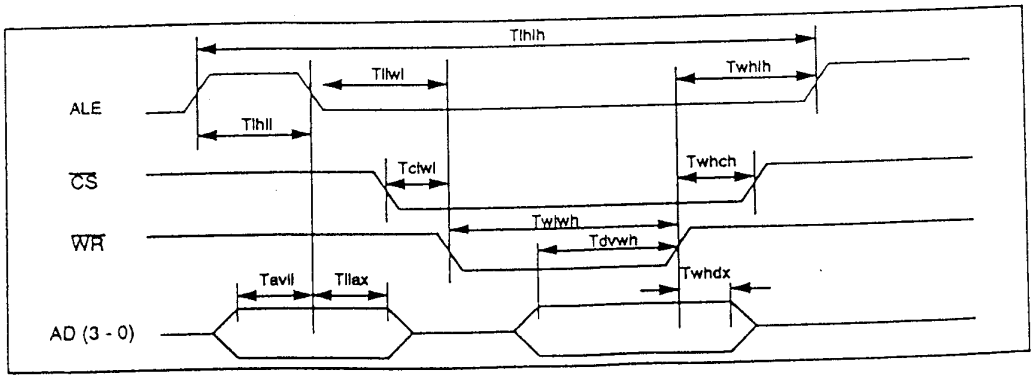


Fig-4 Microprocessor Port Write Cycle Timing

Functional Description

The AK134/135 is a high-speed 2-wire quadrupe TCM transceiver for PBX and KTS systems. It provides 160 kbps for transparent transmission of 2B+D+M channels. It is clocked to produce self-contained AMI pulses at a line rate of 512 kbps. Designed for Line Termination (LT) master applications only, the AK134/135 allows effective full-duplex transmission of high-speed digital data over existing twisted-pair installations. The AK134/135 operates over most customer premises wiring from 19 to 26 AWG. In typical systems (24 AWG), the AK134 is effective in subscriber loops of up to 1 km (3300 feet), and the AK135 is effective in subscriber loops of up to 2 km (6500 feet).

Each transmitter incorporates an 800 Ω fully differential line driver that, when coupled through two 200 Ω series termination resistors and a 2:1 step-down transformer, produces a peak line signal of 625 mV on a 100 Ω line from a single +5 V power supply. It uses AMI line coding for minimum spectral radiation and reduce RFI.

Each receiver uses a fully differential architecture to reduce the effect of impulsive noise. The adaptive data slicers and peak detectors (AK134), or the adaptive equalizer (AK135), ensure optimum signal-to-noise ratio regardless of received signal strength. These design allow data recovery with a Bit Error Rate of less than 10^{-7} over the specific operating conditions.

The system interface includes a simple PCM port and a microprocessor port. The PCM port is compatible with a variety of industry standard crosspoint switches. The microprocessor port is compatible with a multiplexed microprocessor bus.

Fig-1 is a simplified block diagram of the AK134/135. The signal received from the twisted-pair line is applied to the AK134/135 at LIH and LIL. This differential signal is processed, through the adaptive data slicer and peak detectors (AK134), or the adaptive equalizer (AK135), and then routed to the data recovery section. The recovered data signal is passed to the AMI decoder. Decoded data is then processed through the output framer to the PCM-BUS and microprocessor port registers.

■ Internal Timing

The AK134/135 requires an external input clock source $\overline{C4i}$ running at 4.096 MHz ($\pm$ 1000 ppm) which is used to generate all internal clocks. The AK134/135 also requires an 8 kHz input frame pulse F0i to indicate the data frame boundaries. It provides a delayed output frame pulse F0o which can be used as an input frame pulse for other devices, allowing them to be daisy-chained on the PCM-BUS.

■ Line Code

The AK134/135 transmits data encoded in self-contained AMI pulses at an effective line rate of 512 kbps. A mark is defined as a voltage differential between LOH and LOL, rather than a specific ground-referenced voltage. LOH and LOL are both held at VCC/2 for a space. See Fig-5.

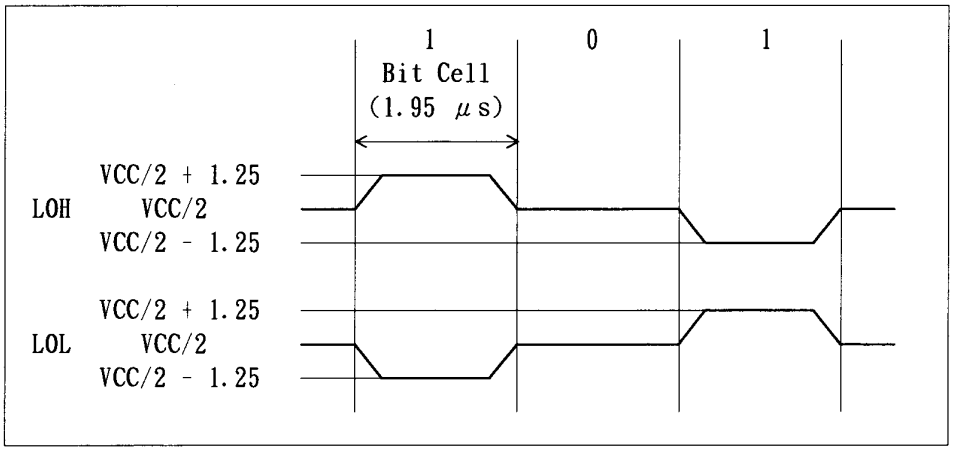


Fig-5 Self-Contained Rectangular AMI Bits

■ TCM Frame Format

The AK134/135 transmits and receives high speed digital data over twisted-pair loops using the 23-bit frame format shown in Fig-6. The 20 data bits are framed by the Start Bit (SB) on one end and two Space Bits (SP) on the other end. The 8 kHz line provides 160 kbps for transparent transmission of two 64 kbps B channels, one 16 kbps D channel and one 16 kbps control and maintenance channel (M channel). The D and M channel data are available through the microprocessor port. B channel data is available on the PCM-BUS.

■ PCM-BUS System Interface

One system interface to the AK134/135 is the flexible PCM-BUS. The PCM-BUS is a synchronous time-division multiplexed serial bus with data streams operating at 2048 kbps. The serial streams are divided into 125 μsec frames made up of 32 8-bit channels. See Fig-7. Synchronization is achieved with an 8 kHz frame pulse (F0i) which identifies the framing boundaries. See Fig-8. Data is clocked into the device on the falling edge of the master clock, C4i, halfway into the bit cell. Data is clocked out on the falling edges of the master clock at the start of the bit cell.

■ PCM-BUS Frame Format

Each of the four AK134/135 transceivers uses two of the 32 channels available in each PCM-BUS frame. The B1 channel data is transported in the first time slot and B2 channel data is transported in the second time slot. The first section of the quad uses time slots 0 and 1. Subsequent sections use time slots 2 through 7 as shown in Fig-9. The DSTo output is tri-stated for all remaining time slot, allowing the PCM-BUS to be shared by other devices. Up to four AK134/135 can use the same PCM-BUS. For PCM streams that must drive heavy loads, such as the system backplane, an external line buffer may be required. An active high enable (ENDST) is provided for this purpose.

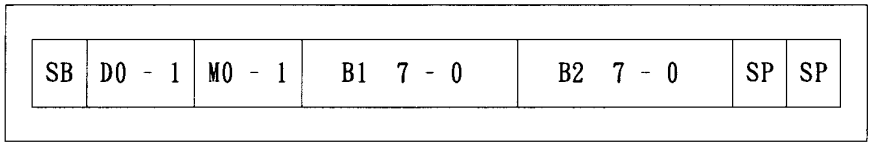


Fig-6 TCM Frame Format

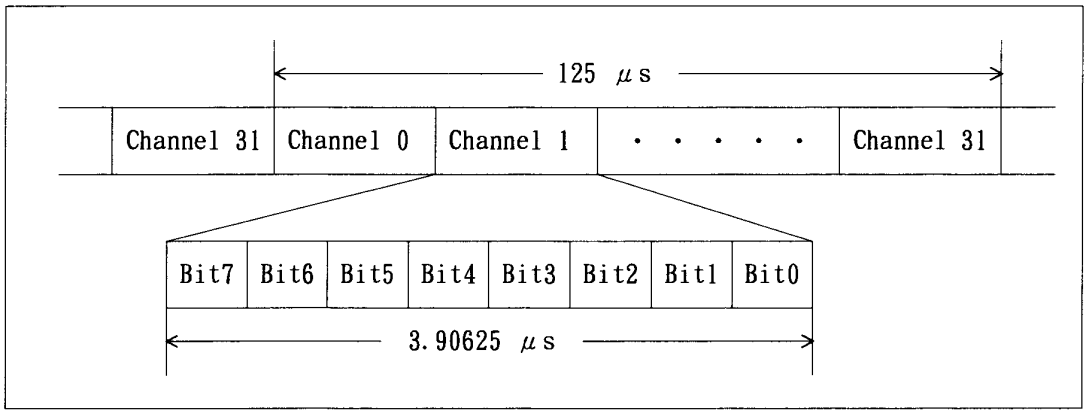


Fig-7 PCM-BUS Stream Format Diagram

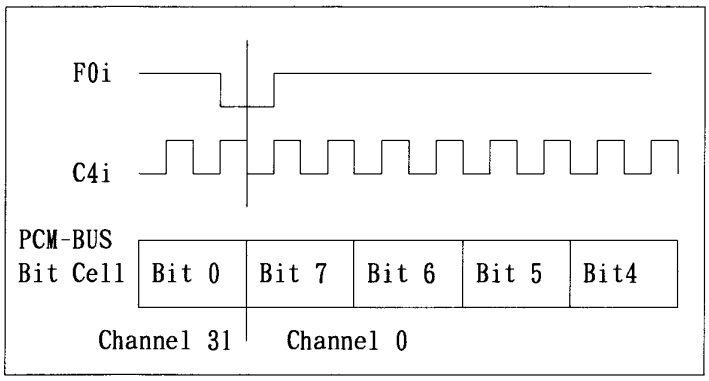


Fig-8 PCM-BUS Bit Cell Framing Diagram

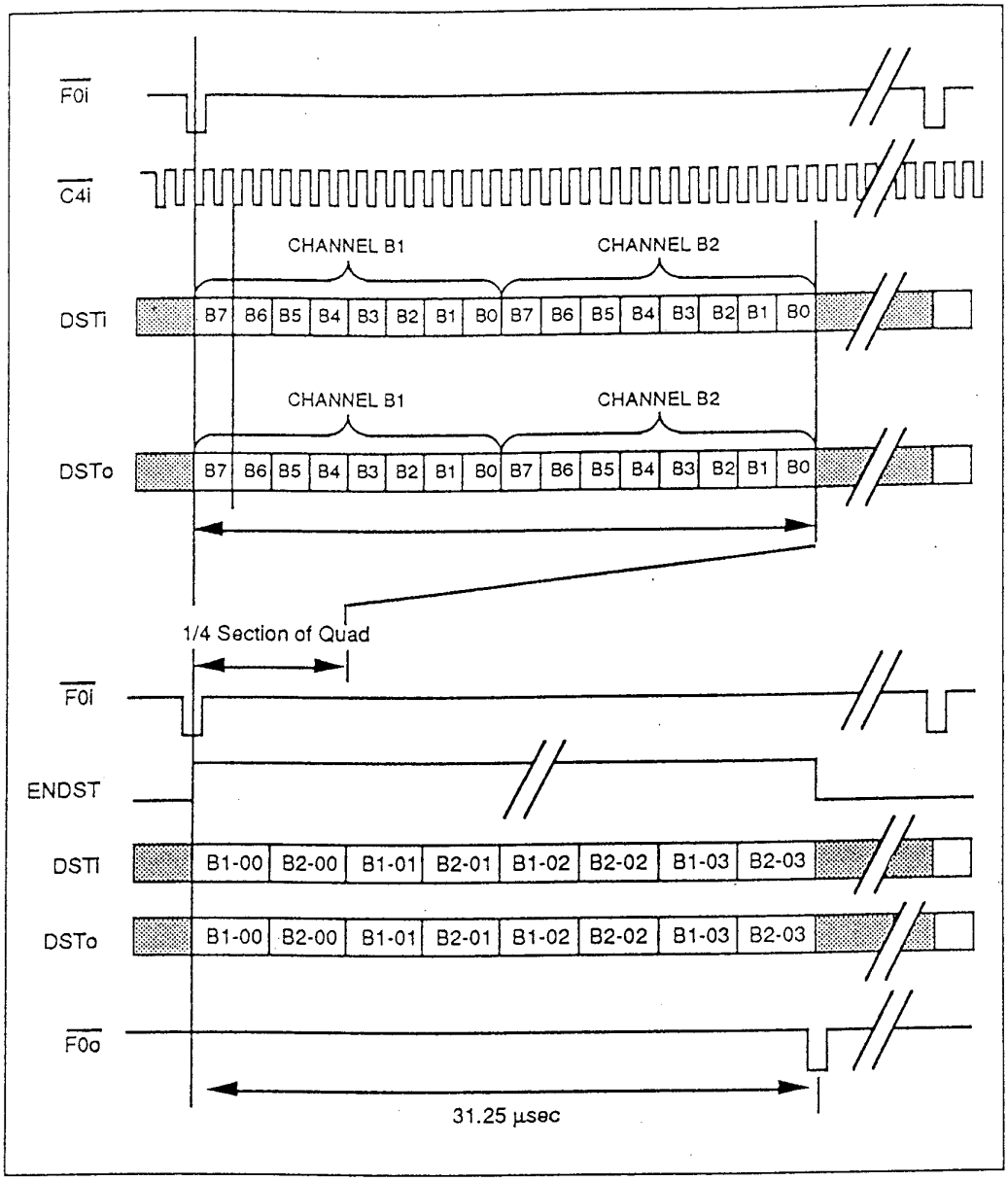


Fig-9 PCM-BUS Allocation

■ Microprocessor Port Operation

D and M channel data is accessed directly through the multiplexed microprocessor port. Each transceiver has its own read and write registers. Each group of read and write registers is addressed separately. The first group has address 0 and subsequent groups have incremental addresses. The address is latched on the falling edge of the ALE signal. Only the two least significant bits of the address are decoded. When selected by the active low CS pin, read or write operations are enabled. It is necessary to select the appropriate AK134/135 with the CS pin if more than one is serviced by the same microprocessor. The microprocessor can access the contents of these registers during the 115 μ s period following the F0i pulse as shown in Fig-10. (Microprocessor port timing is shown in Fig-3 and Fig-4.)

The two bits from the D channel and the two bits from the M channel are accessed in a common 4-bit nibble. The band-width of the two channels can be combined to form an uncommitted 32 kbps channel, or divided into sub-rate channels to meet specific applications. The bit order in the microprocessor port is as follows:

AD(3)	AD(2)	AD(1)	AD(0)
D1	D0	M1	M0

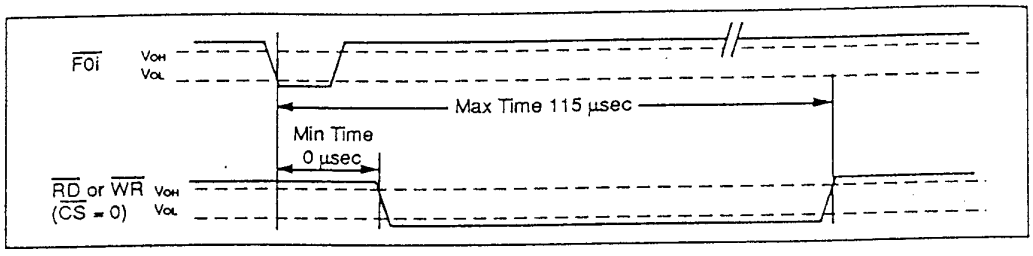


Fig-10 Microprocessor Port Read/Write Access

Applications

A typical AK134/135 application is shown in Fig-11.

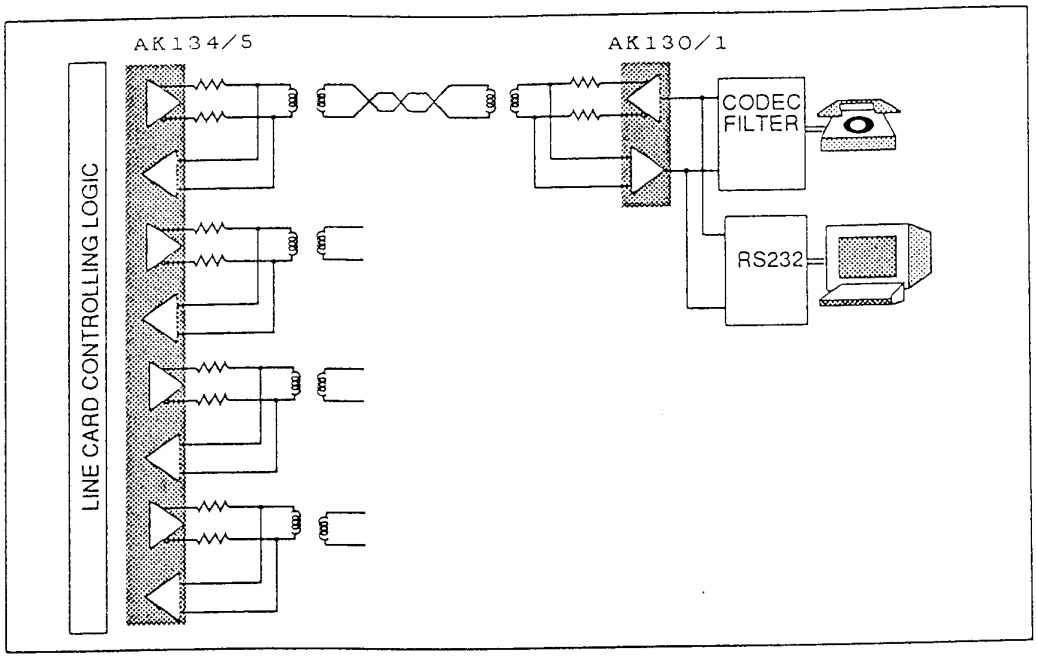
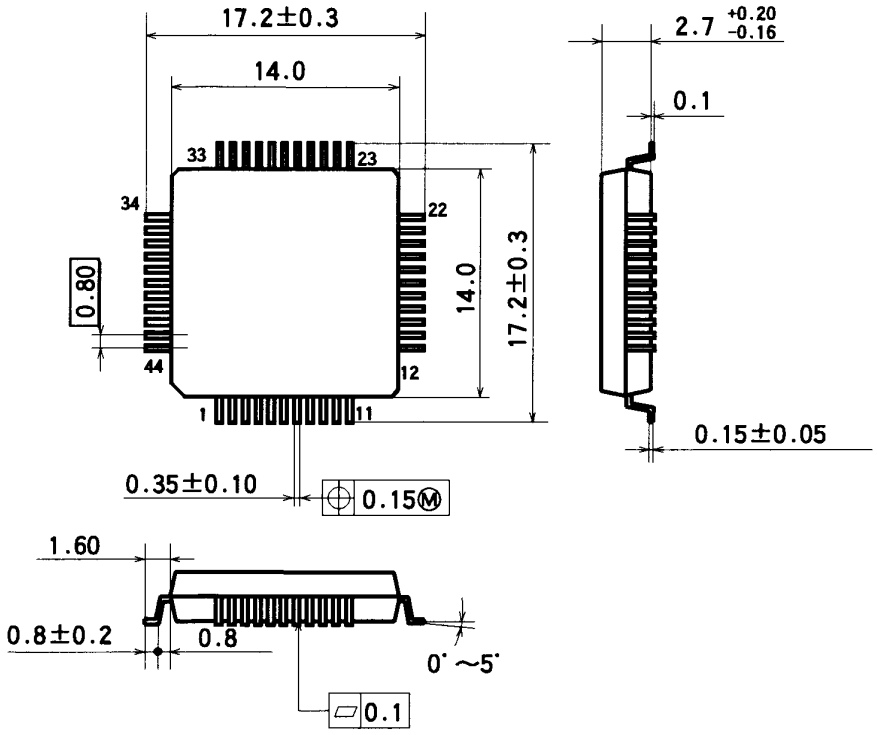


Fig-11 Typical AK134/135 Line Card Application

Packaging Information

■ 44 pin QFP



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