Standard Products

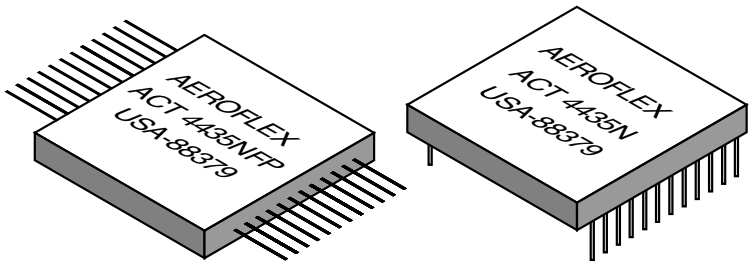
ACT4435N Transceiver

for H009 Specification

June 18, 2004

FEATURES

- ACT4435N Transceiver meets H009 data bus specifications
- Transmitter can be used to drive clock signal line
- Operates with ±15 Volts to ±12 Volts power supplies
- Direct replacement for CT1641 and CT1816 devices
- Voltage source output for higher bus drive power
- Plug-in and flat package available
- Monolithic construction using linear ASICs
- Processed and screened to MIL-STD-883 specs
- MIL-PRF-38534 compliant devices available
- Aeroflex is a Class H & K MIL-PRF-38534 Manufacturer



ACT4435NFP / 4435N

GENERAL DESCRIPTION

The Aeroflex Laboratories transceiver model ACT4435N is a new generation monolithic transceiver which provide full compliance with Macair and MIL-STD-1553 data bus requirements

The model ACT4435N performs the front-end analog function of inputting and outputting data through a transformer to a H009 data bus.

The Design of these transceivers reflects particular attention to active filter performance. This results in low bit and word error rate with superior waveform purity and minimal zero crossover distortion. The ACT4435N active filter design has additional high frequency roll-off to provide the required low harmonic distortion waveform without increasing the pulse delay characteristics significantly.

Efficient transmitter electrical and thermal design provides low internal power dissipation and heat rise at high and well as low duty cycles.

An optional receiver input threshold adjustment can be accomplished by the use of the "External Threshold" terminals.

TRANSMITTER

The Transmitter section accepts bi-phase TTL data at the input and when coupled to the data bus with a 1:1 transformer, isolated on the transceiver side with two 35 Ohm bus terminating resistors, with the bus terminated by a 170 Ohm resistor the data bus signal produced is 20.0 Volts typical P-P at A-A' (See Figure 5). When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitter output becomes a low impedance and signal is "removed" from the line. In addition, an overriding "INHIBIT" input returns the output to a high impedance state. A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the transmitter (See Transmitter Logic Waveforms - Figure 1).

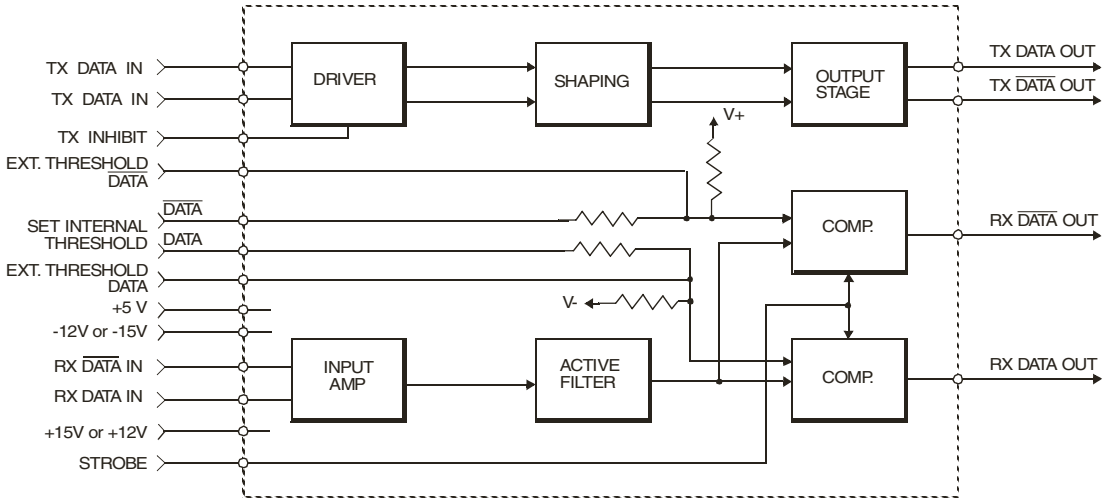
The transmitter utilizes an active filter to suppress harmonics above 1 MHz to meet H009 specifications. The transmitter may be safely operated for an indefinite period at 100% duty cycle into a data bus short circuit.

RECEIVER

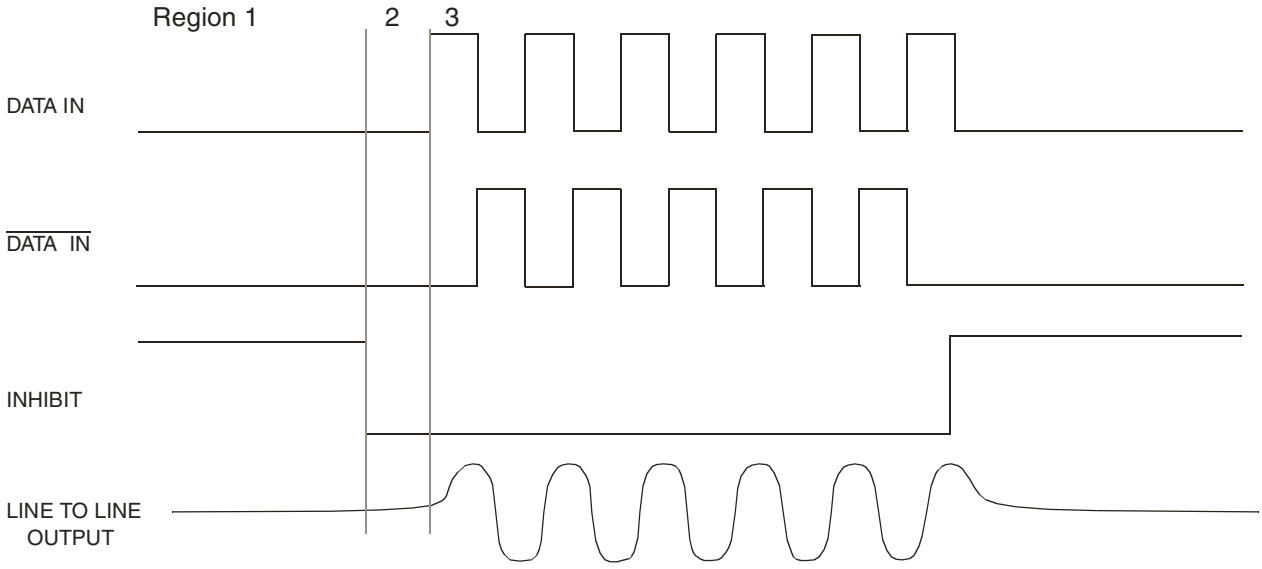
The Receiver section accepts bi-phase differential data at the input and produces two TTL signals at the output. The outputs are DATA and $\overline{\text{DATA}}$, and represent positive and negative excursions of the input beyond a pre-determined threshold (See Receiver Logic Waveforms - Figure 2).

The internal threshold is nominally set to detect data bus signals exceeding 1.05 Volts P-P and reject signals less than 0.6 Volts P-P when used with a 1:1 turns ratio transformer (See Figure 5 for transformer data and typical connection). This threshold setting can be held by grounding the appropriate pins or modified with the use of external resistors.

A low level at the Strobe input inhibits the DATA and $\overline{\text{DATA}}$ outputs. If unused, a 2K Ohm pull-up to +5 Volts is recommended.

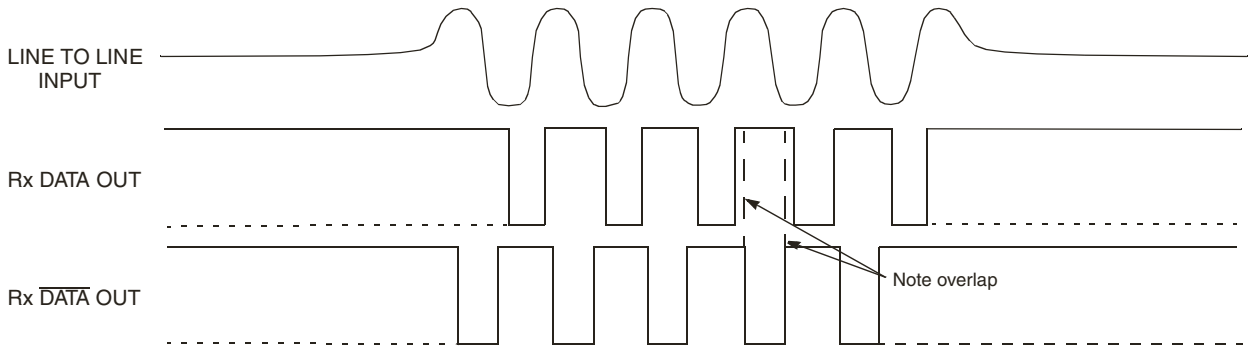


BLOCK DIAGRAM (WITHOUT TRANSFORMER)



Notes: 1. Data and DATA inputs must be complementry waveforms or 50% duty cycle average, with no delays between them, and in the same state during the off time (both high and low).
2. Region 1 ; no output signal, High Z state, (Receive Mode), Region 2; No Output signal, Low Z state, (Terminate Mode), Region 3, Transmitter signal on, low Z.

FIGURE 1 – TRANSMITTER LOGIC WAVEFORMS



Note: Waveforms shown are for normally low devices. For normally high receiver output level devices, the receiver outputs are swapped as shown by the dashed lines

FIGURE 2 – RECEIVER LOGIC WAVEFORMS

ABSOLUTE MAXIMUM RATINGS

Operating Case Temperature	-55°C to +125°C	
Storage Case Temperature	-65°C to +150°C	
Power Supply Voltages	±15VDC P.S. to ±18VDC MAX	+5VDC P.S. to +7VDC
Logic Input Voltage	-0.3 V to +5.5 V	
Receiver Differential Input	±40 V	
Receiver Input Voltage (Common Mode)	±10V	
Driver Peak Output Current	150 mA	
Total Package Power Dissipation over the Full Operating Case Temperature Range	3.25 Watts	
Maximum Junction to Case Temperature (100% duty cycle)	16.25°C	
Junction-Case, Thermal Resistance	5°C/W	

ELECTRICAL CHARACTERISTICS – DRIVER SECTION
INPUT CHARACTERISTICS, TX DATA IN OR TX $\overline{\text{DATA}}$ IN

Parameter	Condition	Symbol	Min	Typ	Max	Unit
"0" Input Current	V_{IN} = 0.4V	I_{ILD}	-	-0.2	-0.4	mA
"1" Input Current	V_{IN} = 2.7V	I_{IHD}	-	1	40	µA
"0" Input Voltage		V_{ILD}	-	-	0.7	V
"1" Input Voltage		V_{IHD}	2.0	-	-	V

INHIBIT CHARACTERISTICS

"0" Input Current	V_{IN} = 0.4V	I_{ILI}	-	-0.2	-0.4	mA
"1" Input Current	V_{IN} = 2.7V	I_{IHI}	-	1.0	40	µA
"0" Input Voltage		V_{ILI}	-	-	0.7	V
"1" Input Voltage		V_{IHI}	2	-	-	V
Delay from TX inhibit, (0→1) to inhibited output	Note 1	t_{DXOFF}	-	200	500	nS
Delay from TX inhibit, (1→0) to active output	Note 1	t_{DXON}	-	250	700	nS
Differential Output Noise, inhibit mode		V_{NOI}	-	0.8	10	mV p-p
Differential Output Impedance (inhibited)	Note2	Z_{OI}	10K	-	-	Ω

OUTPUT CHARACTERISTICS

Differential output level at point A-A' on Figure 5	RL=170 Ω	V_O	17	21	24	V p-p
Rise and fall times (10% to 90% of p-p output)		t_r	200	-	300	nS
Output offset at point A-A' on Figure 5, 2.5 µS after midpoint crossing of the last bit	RL=170 Ω	V_{OS}	-	-	±265	mV peak
Delay from 50% point of TX DATA or $\overline{\text{TX DATA}}$ input to zero crossing of differential signal (Note 1)		t_{DTX}	-	270	400	nS

ELECTRICAL CHARACTERISTICS – RECEIVER SECTION

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Differential Input Impedance (Note 1)	f= 1MHz	Z_{IN}	20K	-	-	Ω
Differential Input Voltage Range		V_{IDR}	-	-	40	V p-p
Input Common Mode Voltage Range	Note 1	V_{ICR}	10	-	-	V p-p
Common Mode Rejection Ratio	Point A-A on Figure 5	CMRR	40	-	-	dB

STROBE CHARACTERISTICS (LOGIC "0" INHIBITS OUTPUT)

"0" Input Current	V_S = 0.4V	I_{IL}	-	-0.2	-0.4	mA
"1" Input Current	V_S = 2.7V	I_{IH}	-	1	+40	µA
"0" Input Voltage		V_{IL}	-	-	0.7	V
"1" Input Voltage		V_{IH}	2.0	-	-	V
Strobe Delay (turn-on or turn-off)		$t_{SD(ON)}$	-	-	150	nS

THRESHOLD CHARACTERISTICS (SINEWAVE INPUT)

Internal Threshold Voltage (Referred to the bus) Pins 6 and 11 to GND For 4435N-701 only – Pins 6 and 11 to GND	100KHz-1MHz	V_{TH}	0.60 1.2	0.80 1.8	1.15 2.3	V P-P V P-P
External Threshold Pins 6 & 11 open, threshold settings resistors from Pin 5 & 12 to ground; For R_{TH} = 3K mimumn to 10K maximum		R_{TH}/V_{TH1}	-	4000	-	Ω/V_{P-P}

OUTPUT CHARACTERISTICS, RX DATA AND RX $\overline{\text{DATA}}$

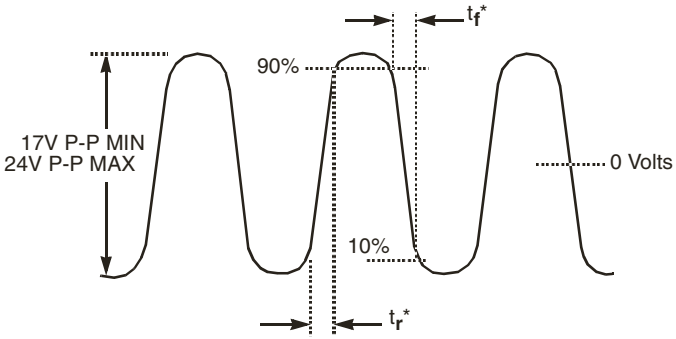
"1" State	I_{OH} = -0.4mA	V_{OH}	2.5	3.6	-	V
"0" State	I_{OL} = 4mA	V_{OL}	-	0.35	0.5	V
Delay, (average) from differential input zero crossings to RX DATA and RX $\overline{\text{DATA}}$ output	50% points	t_{DRX}	-	275	450	nS

POWER SUPPLY CURRENT

Duty Cycle	Condition	Symbol	Typ	Max	Unit
Transmitter Standby		I_{CC} I_{EE} I_L	5 15 18	10 35 30	mA
25%		I_{CC} I_{EE} I_L	25 35 18	40 60 30	
50%		I_{CC} I_{EE} I_L	45 55 18	60 80 30	
100%		I_{CC} I_{EE} I_L	85 95 18	120 140 30	

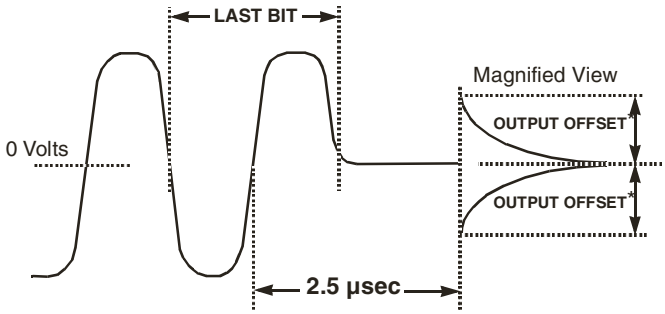
Notes:

1. Characteristics guaranteed by design, not production tested.
2. Measured at 1mHz at point A-A', power on or off.
3. Specifications apply over the temperature range of -55°C to +125°C (case temperature) unless otherwise noted.
4. All typical values are measured at +25°C.



* Rise and fall times measured at point A-A' in Fig 5

FIGURE 3 – TRANSMITTER (TX) OUTPUT WAVEFORM



*Offset measured at point A-A' in Fig 5

FIGURE 4 – TRANSMITTER (TX) OUTPUT OFFSET

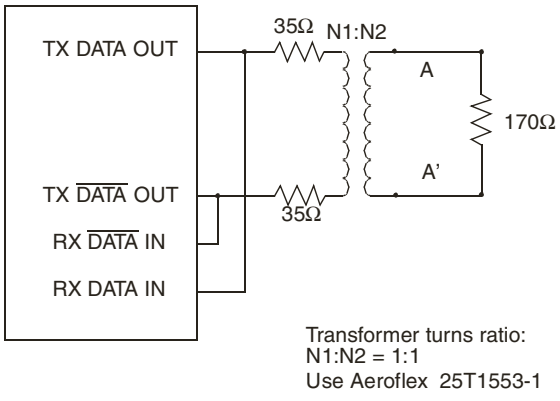


FIGURE 5 – TYPICAL TRANSFORMER CONNECTION

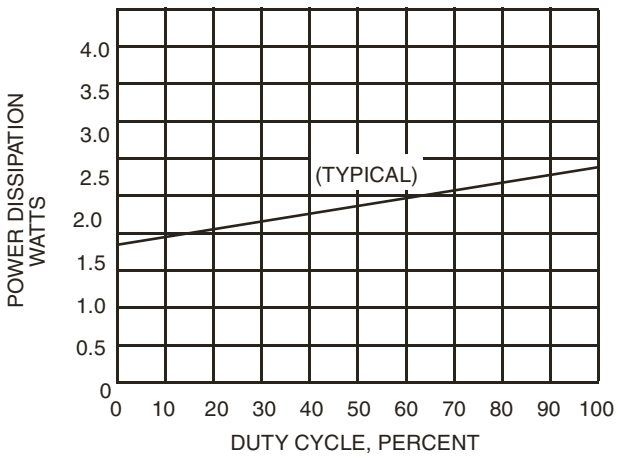


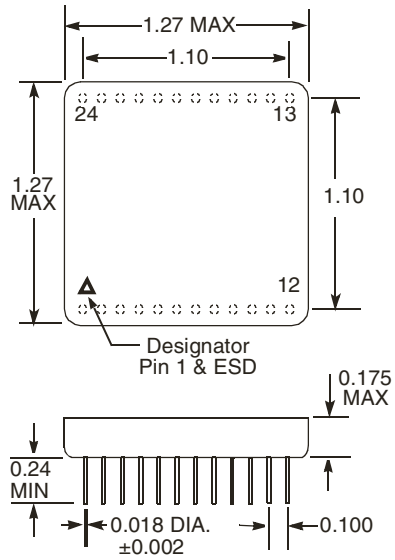
FIGURE 6 – POWER DISSIPATION VS. DUTY CYCLE

CONFIGURATIONS AND ORDERING INFORMATION

Model No.	DESC No.	Receiver Data level	Case	Specs.
ACT4435N	To Be Assigned	Normally High	Plug In	H009
ACT4435N-FP		Normally High	Flat Pack	
ACT4435N-701	-	Normally High	Plug In	H009 Commercial (0°C - 70°C)

PACKAGE CONFIGURATIONS AND PINOUTS

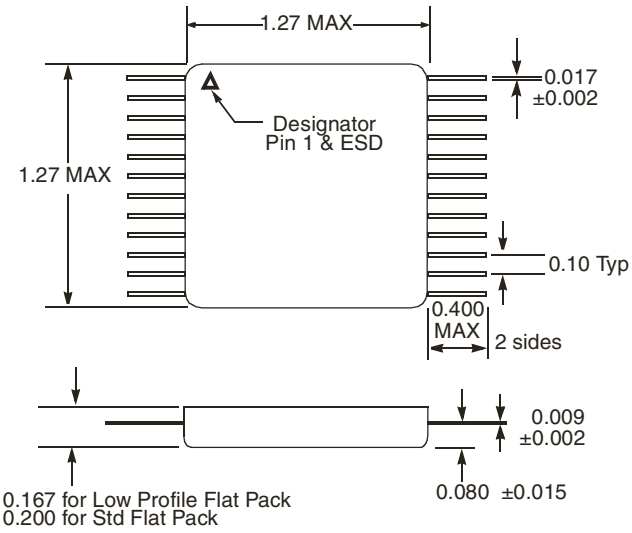
PLUG-IN PACKAGE



PIN CONNECTIONS

1. TX DATA OUT
2. TX DATA OUT
3. TX GND (+5V)
4. +15V (TX)
5. EXT. DATA THRES
6. INT. DATA THRES
7. RX DATA OUT
8. STROBE
9. RX GND (+5V)
10. RXDATA OUT
11. INT DATA THRES
12. EXT DATA THRES
13. +15V (RX)
14. N.C.
15. RX DATA IN
16. RX DATA IN
17. GND
18. CASE GND
19. -15V (RX)
20. +5V
21. TX INHIBIT
22. TX DATA IN
23. TX DATA IN
24. -15V (TX)

FLAT PACKAGE



Notes 1. Dimensions shown are in inches.
2. Pins are equally spaced at 0.100±0.002 tolerance non-cumulative each row.

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