# EClamp2388P ESD/EMI Protection for Color LCD Interfaces

#### PROTECTION PRODUCTS - EMIClamp™

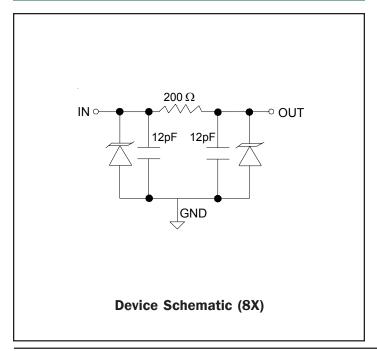
#### Description

The EClamp<sup>™</sup>2388P is a low pass filter array with integrated TVS diodes. It is designed to suppress unwanted EMI/RFI signals and provide electrostatic discharge (ESD) protection in portable electronic equipment. This state-of-the-art device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. They have been optimized for **protection of color LCD panels** in cellular phones and other portable electronics.

The device consists of eight identical circuits comprised of TVS diodes for ESD protection, and a resistor - capacitor network for EMI/RFI filtering. A series resistor value of  $200\Omega$  and a capacitance value of 12pF are used to achieve 30dB minimum attenuation from 800MHz to 2.7GHz. The TVS diodes provide effective suppression of ESD voltages in excess of  $\pm 15\text{kV}$  (air discharge) and  $\pm 8\text{kV}$  (contact discharge) per IEC 61000-4-2, level 4.

The EClamp2388P is in a 16-pin, RoHS/WEEE compliant, SLP4016P16 package. It measures  $4.0 \times 1.6 \times 0.58$ mm. The leads are spaced at a pitch of 0.5mm and are finished with lead-free NiPd. The small package makes it ideal for use in portable electronics such as cell phones, digital still cameras, and PDAs.

# Circuit Diagram (Each Line)



#### **Features**

- Bidirectional EMI/RFI filter with integrated TVS for ESD protection
- ◆ ESD protection to IEC 61000-4-2 (ESD) Level 4, ±15kV (air), ±8kV (contact)
- Filter performance: 30dB minimum attenuation 800MHz to 2.7GHz
- TVS working voltage: 5V
- Resistor:  $200\Omega + 15\%$
- ◆ Typical Capacitance: 12pF (VR = 2.5V)
- Protection and filtering for eight lines
- Solid-state technology

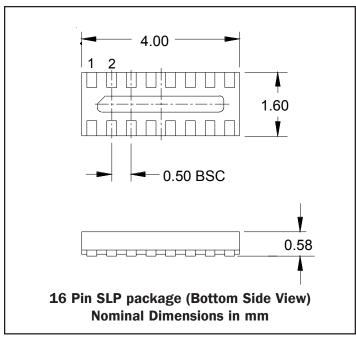
#### Mechanical Characteristics

- SLP4016P16 16-pin package
- ◆ RoHS/WEEE Compliant
- ◆ Nominal Dimensions: 4.0 x 1.6 x 0.58 mm
- Lead Pitch: 0.5mm
- Lead finish: NiPd
- Marking: Marking Code
- Packaging: Tape and Reel per EIA 481

#### **Applications**

- Color LCD Protection
- ◆ Cell Phone CCD Camera Lines
- ◆ CDMA/GSM Cell Phones

#### Package Configuration





# Maximum Ratings

Rating	Symbol	Value	Units
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V <sub>ESD</sub>	+/- 17 +/- 12	kV
Junction Temperature	T,	125	°C
Operating Temperature	T <sub>op</sub>	-40 to +85	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

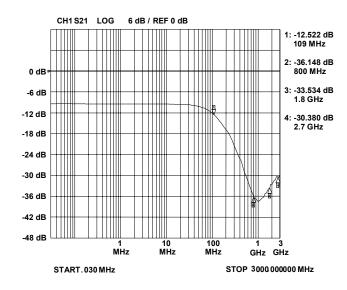
# Electrical Characteristics (T = 25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
TVS Reverse Stand-Off Voltage	$V_{_{\mathrm{RWM}}}$				5	V
TVS Reverse Breakdown Voltage	$V_{BR}$	I <sub>t</sub> = 1mA	6	8	10	V
TVS Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 3.0V			0.5	μΑ
Total Series Resistance	R	Each Line	170	200	230	Ohms
Capacitance	C <sub>in</sub>	Input to Gnd, Each Line V <sub>R</sub> = 2.5V, f = 1MHz	10	12	15	pF
Capacitance	C <sub>in</sub>	Input to Gnd, Each Line V <sub>R</sub> = OV, f = 1MHz	18	22	27	pF

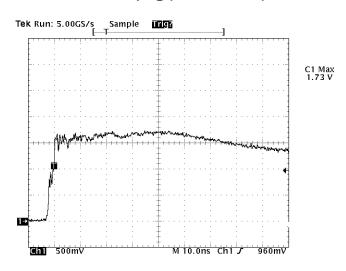


# Typical Characteristics

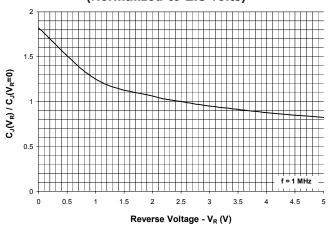
#### **Typical Insertion Loss S21 (Each Line)**



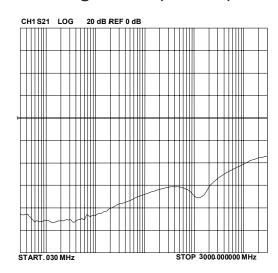
#### **ESD Clamping (+8kV Contact)**



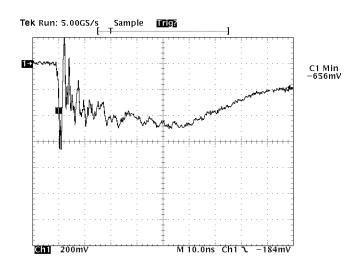
# Capacitance vs. Reverse Voltage (Normalized to 2.5 volts)



#### **Analog Crosstalk (Each Line)**



#### **ESD Clamping (-8kV Contact)**





#### **Applications Information**

#### **Device Connection**

The EClamp2388P is comprised of eight identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in a 16-pin SLP package. Electrical connection is made to the 16 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

#### **Ground Connection Recommendation**

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.

Equation 1: The Impedance of an Inductor at Frequency XLF

 $XLF(L, f) = 2 * \pi * f * L$ 

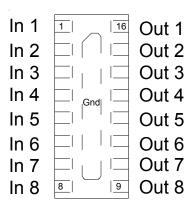
Where:

L= Inductance (H)

f = Frequency (Hz)

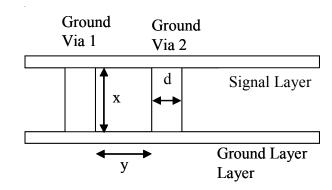
Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x. The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.

Figure 1 - Pin Identification and Configuration (Top Side View)



Pin	Identification
1 - 8	Input Lines
9 - 16	Output Lines
Center Tab	Ground

Figure 2 - Inductance of Rectangular Wire Loops



**Equation 2: Inductance of Rectangular Wire Loop** 

LRECT(d, x, y) = 
$$10.16 * 10^{-9} * \left[ x * ln \left[ \frac{2*y}{d} \right] + y * ln \left[ \frac{2*x}{d} \right] \right]$$

Where:

d = Diameter of the wire (in)

x = Length of wire loop (in)

y = Breath of wire loop (in)



#### **Applications Information**

Figure 3 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20 mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance (i.e. the log function in Equation 2 in highly insensitive to parameter d) . Figure 4 shows a typical insertion loss (S21) plot for the device using Semtech's filter evaluation board with 50 Ohm traces and the recommended via configuration.

Figure 3 - Recommended Layout Using Ground Vias

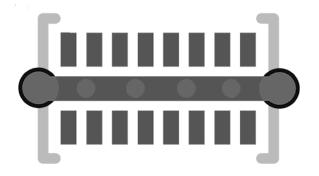
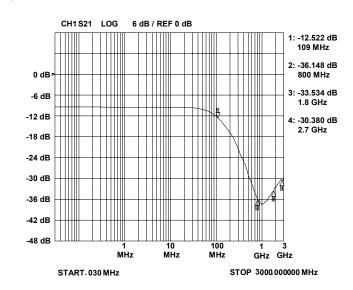


Figure 4 - Filter Characteristics Using Recommended Layout with Internal Vias





# Applications Information - Spice Model

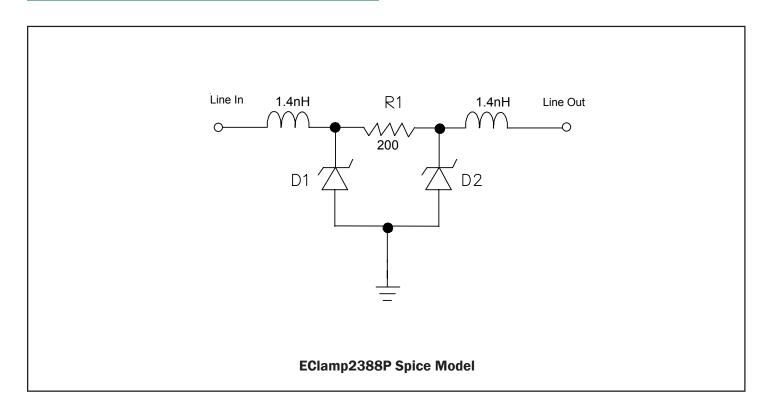
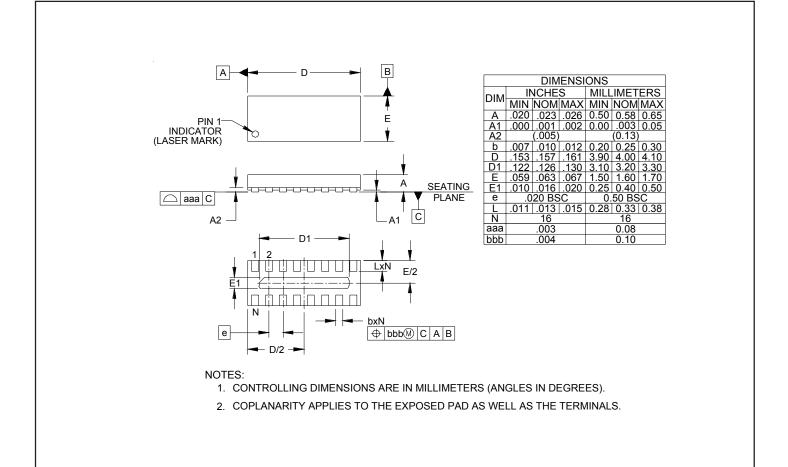


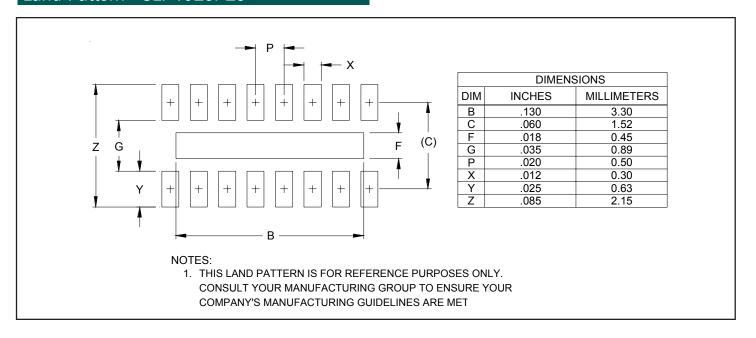
Table 1 - EClamp2388P Spice Parameters								
Parameter	Unit	D1 (TVS)	D2 (TVS)					
IS	Amp	5.15E-15	5.15E-15					
BV	Volt	7.53	7.53					
VJ	Volt	0.75	0.75					
RS	Ohm	0.426	0.426					
IBV	Amp	1E-3	1E-3					
C10	Farad	23E-12	23E-12					
TT	sec	2.541E-9	2.541E-9					
М		0.256	0.256					
N		1.1	1.1					
EG	eV	1.11	1.11					



#### Outline Drawing - SLP4016P16

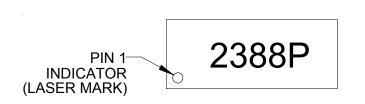


# Land Pattern - SLP4016P16





#### Marking

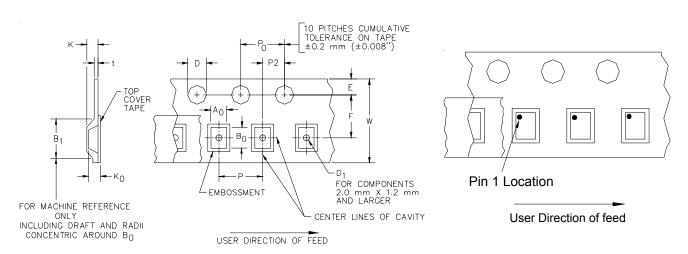


# Ordering Information

Part Number	Qty per Reel	Reel Size		
EClamp2388P.TCT	3000	7 Inch		

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# Tape and Reel Specification



#### **Device Orientation in Tape**

A0	В0	ко		
1.78 +/-0.10 mm	4.30 +/-0.10 mm	0.74 +/-0.10 mm		

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	Р	PO	P2	T(MAX)	W
12 mm	8.2 mm (.476)	1.5 + 0.1 mm - 0.0 mm (0.59 +.005 000)	1.0 mm ±0.05 (.039)	1.750±.10 mm (.069±.004)	5.5±0.05 mm (.217±.002)	4.5 mm (.177)	4.0±0.1 mm (.157±.00- 4)	4.0±0.1 mm (.157±.00- 4)	2.0±0.05m- m (.079±.002)	0.4 mm (.016)	12.0 mm + 0.3 mm - 0.1 mm (.472±.012)

# **Contact Information**

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