

General Description

The HMC767LP6CE is a fully functioned Fractional-N Phase-Locked-Loop (PLL) Frequency Synthesizer with an integrated Voltage Controlled Oscillator (VCO). The input reference frequency range is DC to 350 MHz while the advanced delta-sigma modulator design in the fractional synthesizer allows both ultra-fine step sizes and very low spurious products. The highly integrated structure provides excellent phase noise performance over temperature, shock and process. In addition, the HMC767LP6CE offers frequency sweep and modulation features, external triggering, double-buffering, exact frequency control, phase modulation and more. The HMC767LP6CE is packaged in a leadless QFN 6 x 6 mm surface mount package.

For theory of operation and register map refer to the "PLLs w/ Integrated VCO - Microwave VCOs" Operating Guide. To view the [Operating Guide](#), please visit www.hittite.com and choose HMC767LP6CE from the "Search by Part Number" pull down menu.

**Electrical Specifications, $T_A = +25^\circ\text{C}$; V_{CCVCO} , V_{DDL5} , $V_{PPCPA} = +5V$;
 R_{VDD} , A_{VDD} , V_{CCPS} , V_{CCHF} , V_{DDPD} , D_{VDD} , $V_{DDIO} = +3.3V$**

| Parameter | Condition | Min. | Typ. | Max. | Units |
|--|---|------|-------------|---------|---------|
| RF Output Characteristics | | | | | |
| VCO Output Frequency Range | | 8.45 | 9.0 | 9.55 | GHz |
| VCO Output Power ^[1] | | | 12 | | dBm |
| VCO Tuning Voltage | | 2 | | 13 | V |
| VCO Tuning Sensitivity | $V_{TUNE} = 6V$ | | 150 | | MHz/V |
| Frequency Pulling | into a 2:1 VSWR | | 6 | | MHz pp |
| Frequency Pushing | $V_{TUNE} = 5V$ | | 20 | | MHz/V |
| Frequency Drift Rate | | | 0.8 | | MHz/ °C |
| Sub Harmonic (1/2) | | | 40 | | dBc |
| Harmonic (2 nd) | | | 15 | | dBc |
| Harmonic (3 rd) | | | 40 | | dBc |
| VCO SSB Phase Noise @ 100 kHz Offset (Open Loop) | $V_{TUNE} = +5V$ $F_{VCO} = 9.0\text{ GHz}$ | | -115 | | dBc/Hz |
| Synthesizer In-Band SSB Phase Noise @ 10 kHz Offset (Integer / Fractional) | $F_{ref} = 50\text{ MHz}$ $F_{VCO} = 9.0\text{ GHz}$ Loop BW = 100 kHz | | -107/-102 | | dBc/Hz |
| Synthesizer Noise Floor, Figure Of Merit (Integer / Fractional) | | | -230 / -227 | | dBc/Hz |
| Synthesizer Fractional Spurs ^[2] | | | -65 | -38 | dBc |
| Synthesizer Frequency Settling Time (100 MHz Step) | 9.0 GHz to 9.1 GHz Loop BW = 100 kHz, 10° | | 433 | | μs |
| RF/2 Divider Range | | | | | |
| > 4GHz Integer Mode | 16 bit, even values only | 32 | | 131,070 | |
| < 4GHz Integer Mode | 16 bit, all values | 16 | | 65,535 | |
| > 4GHz Fractional Mode | 16 bit | 40 | | 131,065 | |
| < 4GHz Fractional Mode | 16 bit | 20 | | 65,531 | |

[1] See power output vs. tuning voltage graph for power slope.

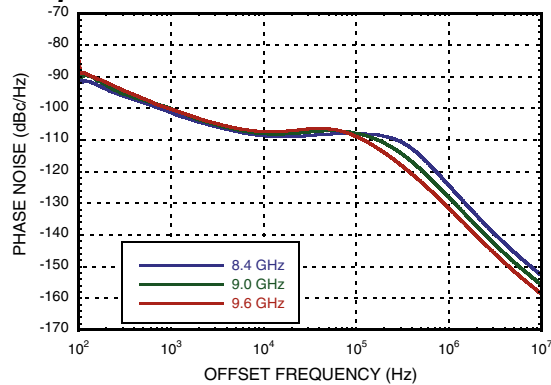
[2] Actual spur level is dependent on loop parameters and will increase at division ratios closest to integer boundaries.

Electrical Specifications (Continued)

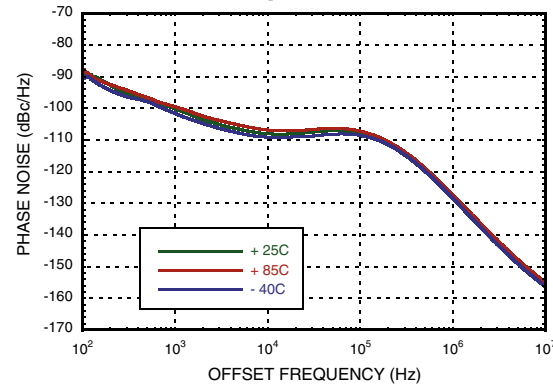
| Parameter | Condition | Min. | Typ. | Max. | Units |
|--|--|------|--------------------------------------|--------|--------|
| REF Input Characteristics | | | | | |
| Frequency Range (3.3V) | | DC | 50 | 350 | MHz |
| Power From 50Ω Source | With off chip 100Ω termination | | 6 | | dBm |
| Return Loss | | -16 | | -8 | dBm |
| Ref Divider Range (14-Bit) | | 1 | | 16,383 | |
| Phase Detector Rate | | | | | |
| Integer Mode | | DC | 50 | 115 | MHz |
| Fractional Mode A | | DC | 50 | 80 | MHz |
| Fractional Mode B | | DC | 50 | 100 | MHz |
| Charge Pump | | | | | |
| CP Output Current | 20μA steps CP_gain = CP_current ÷ 2π (amps/rad) | 0.02 | | 2.5 | mA |
| CP HIK | see "Charge Pump Gain" section of "Operation Guide" | | 3.5 | 6 | mA |
| Logic Inputs | | | | | |
| Switching Threshold (Vsw) | VIH/VIL within 50mV of Vsw | 38 | 47 | 54 | %VDDIO |
| Logic Outputs | | | | | |
| VOH Output High Voltage | | | VDDIO | | V |
| VOL Output Low Voltage | | | 0 | | V |
| Output Impedance: Pull Up | VDDIO = 3.3V | 115 | 150 | 180 | Ω |
| Output Impedance: Pull Dn | VDDIO = 3.3V | 130 | 135 | 210 | Ω |
| DC Load | | | | 1.5 | mA |
| Digital Output Driver Delay SCK to Digital Output Delay | 1.7 ns with a 3 pF load | | 0.5ns + 0.2ns/pF 8.2ns + 0.2ns/pF | | ns |
| Power Supply Voltages | | | | | |
| VCCVCO - VCO Supply | | 4.75 | 5.0 | 5.25 | V |
| RVDD, AVDD, VCCPS, VCCHF, VDDPD - Analog Supply | all must be equal | 2.7 | 3.3 | 3.5 | V |
| DVDD, VDDIO - Digital Supply | both must be equal | 2.7 | 3.3 | 3.5 | V |
| VDDL, VPPCPA - Charge pump | both must be equal | 4.7 | 5.0 | 5.2 | V |
| Power Supply Currents | | | | | |
| 5.0V - VCO Current Consumption | | 230 | 250 | 270 | mA |
| 3.3V - PLL Current Consumption | all modes | 34 | 54 | 95 | mA |
| 5.0V - Charge Pump Current Consumption | all modes | 3 | 7 | 16 | mA |
| Power Down Current | except VCO | | | 100 | μA |
| Bias Reference Voltage (Pin 20) | Measured with 10 GΩ meter | 1.88 | 1.92 | 1.96 | V |

FRACTIONAL-N PLL WITH INTEGRATED VCO, 8.45 - 9.55 GHz

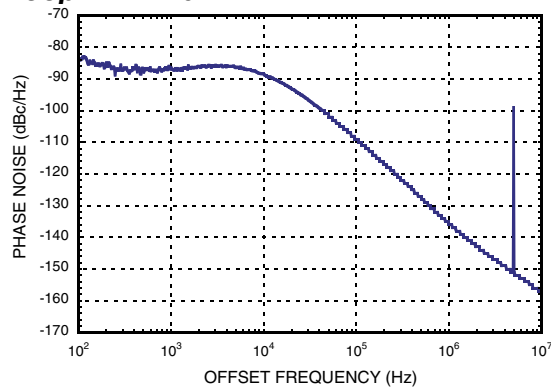
**SSB Phase Noise vs. Frequency,
Integer Mode, Fref = 50 MHz,
Loop BW = 100 kHz**



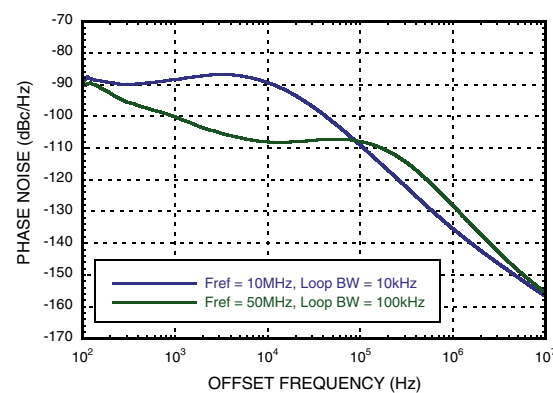
**SSB Phase Noise vs. Temperature
@ 9.0 GHz, Integer Mode,
Fref = 50 MHz, Loop BW = 100 kHz**



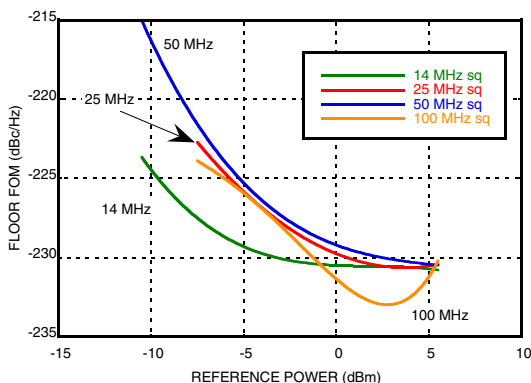
**SSB Phase Noise Fractional Spurs @
9.01 GHz, Fref = 10 MHz,
Loop BW = 10 kHz**



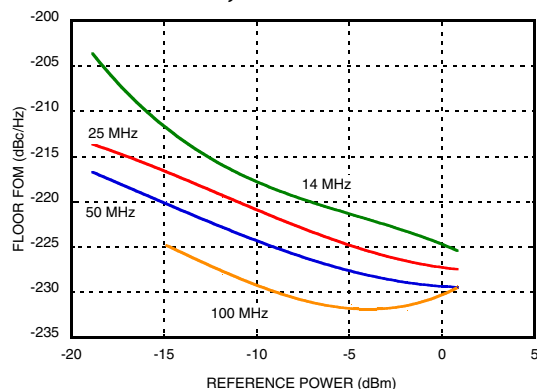
**SSB Phase Noise vs. Reference Freq. &
Loop BW @ 9.0 GHz, Integer Mode**



**Reference Input Sensitivity,
Square Wave, 50Ω**



**Reference Input Sensitivity,
Sinusoid Wave, 50Ω**





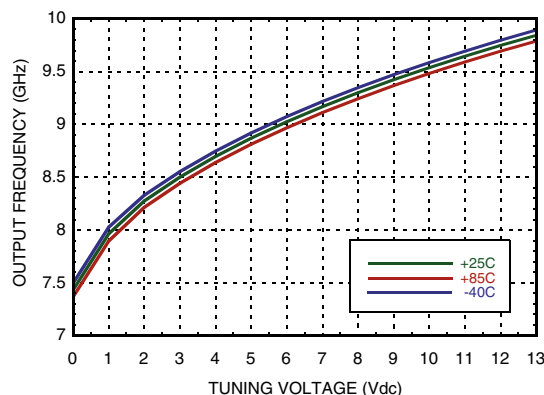
MICROWAVE CORPORATION v01.0112



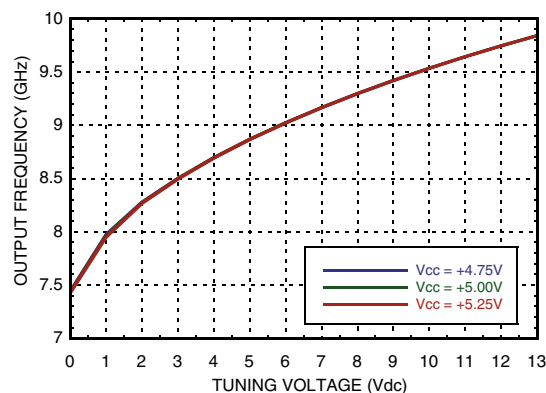
HMC767LP6CE

FRACTIONAL-N PLL WITH INTEGRATED VCO, 8.45 - 9.55 GHz

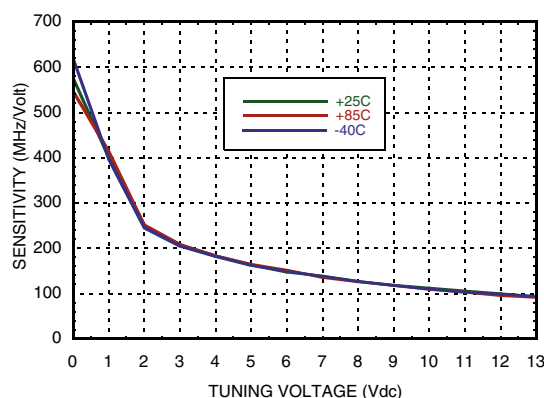
**Frequency vs. Tuning Voltage,
Vcc = +5V**



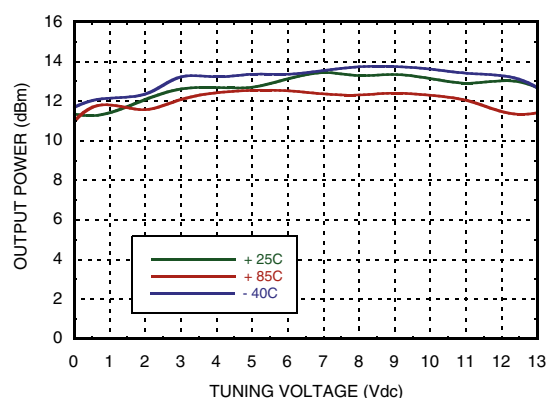
**Frequency vs. Tuning Voltage,
T = 25°C**



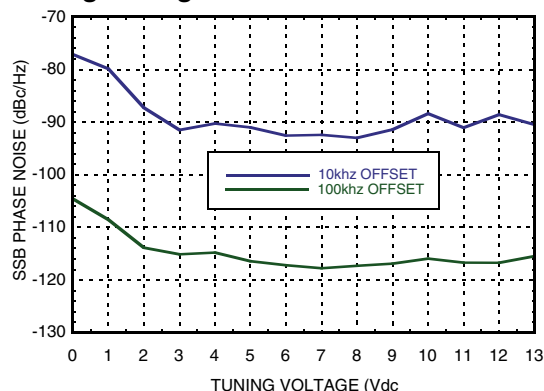
**Sensitivity vs. Tuning Voltage,
Vcc = +5V**



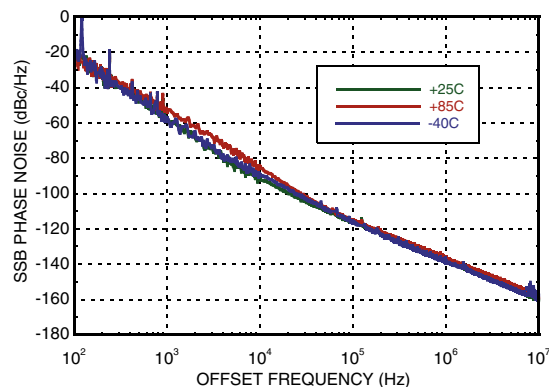
**Output Power vs. Tuning Voltage,
Vcc = +5V**



**Open Loop VCO SSB Phase Noise vs.
Tuning Voltage**



**Open Loop VCO SSB Phase Noise,
Vtune = +5V**

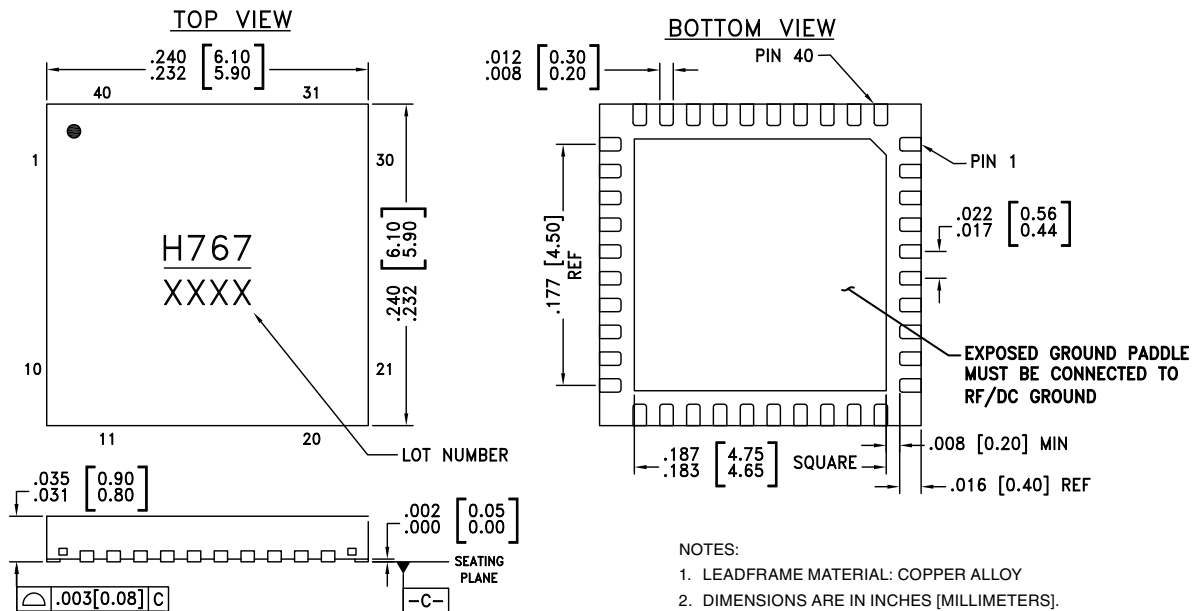


**FRACTIONAL-N PLL WITH
INTEGRATED VCO, 8.45 - 9.55 GHz**
Absolute Maximum Ratings

| | |
|---|------------------------|
| VCCVCO1, VCCVCO2 | +5.5V |
| Vtune | 0 to +15V |
| RVDD, AVDD, VCCPS, VCCHF, VDDPD | -0.3V to +3.6V |
| DVDD, VDDIO | -0.3V to +3.6V |
| VDDL5, VPPCPA | -0.3V to +5.5V |
| Digital Load | 1 K Ω min. |
| Digital Input 1.4V to 1.7V min. rise time | 20 ns |
| Digital Input Voltage Range | -0.25V to VDDIO + 0.5V |
| Storage Temperature Range | -65° C to +125° C |
| ESD Sensitivity (HBM) | Class 1A |

Reliability Information

| | |
|---|--------------|
| Junction Temperature To Maintain 1 Million Hours MTTF | 135 °C |
| Nominal Junction Temperature (T = +85°C) | 121.3 °C |
| Thermal Resistance (Junction to GND Paddle, 5V Supply) | 24.8 °C/W |
| Operating Temperature | -40 to +85°C |

Outline Drawing

Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[1] |
|-------------|--|---------------|------------|--------------------------------|
| HMC767LP6CE | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL3 | H767 XXXX |

[1] 4-Digit lot number XXXX

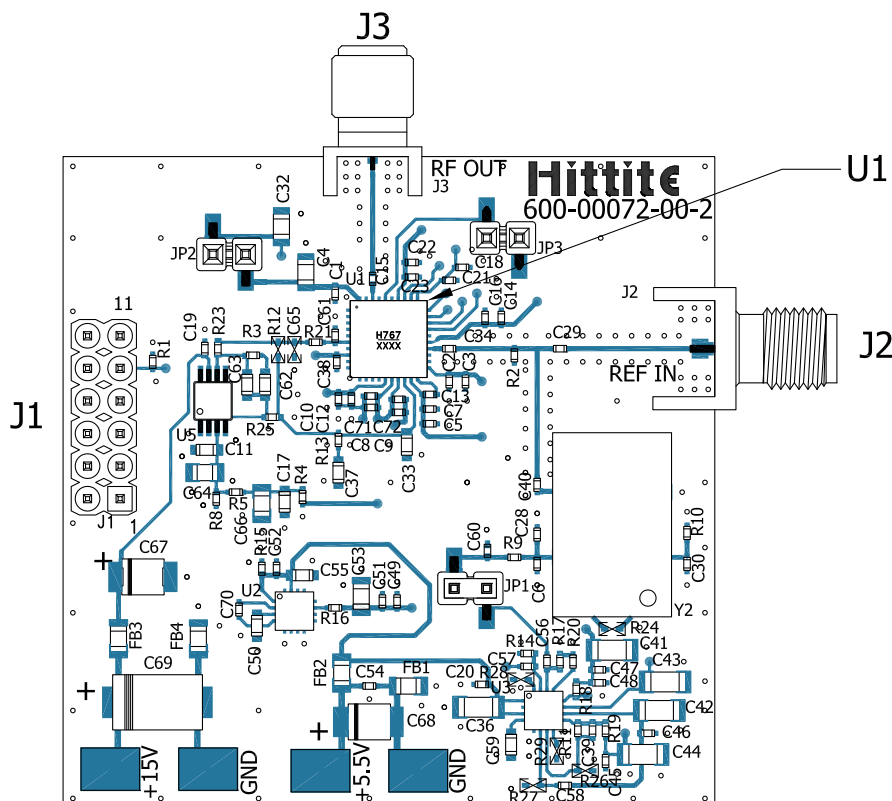
Pin Descriptions

| Pin Number | Function | Description |
|---------------------------|---------------------|--|
| 1, 9 - 14, 22, 23, 26, 35 | N/C | No connection. These pins may be connected to RF/DC ground. Performance will not be affected. |
| 2 - 5, 37, 39 | GND ^[1] | Pins must be connected to RF/DC ground |
| 7 | GND | This pin and package bottom must be connected to RF/DC ground |
| 6 | VTUNE | Control voltage input. Modulation port bandwidth dependent on drive source impedance. |
| 8 | VCCVCO2 | + 5V power supply for VCO. |
| 15 | VCCHF | Analog power supply for RF buffer. Nominal + 3.3V, 6 mA max. |
| 16 | VDDL5 | Power supply for PFD to CP level shifters. Nominal + 5V, 5 mA max., Fpd dependent. |
| 17 | VPPCPA | Power Supply for the charge pump. Nominal + 5V, 10 mA Max. |
| 18 | CP | Charge pump output |
| 19 | AVDD | Power Supply for analog bias generation. Nominal + 3.3V, 2 mA Max. |
| 20 | BIAS ^[2] | External bypass decoupling for precision bias circuits, 1.920V \pm 2 mV is generated internally |
| 21 | RVDD | Power Supply for Reference Path. Nominal + 3.3V, 15 mA Max., reference dependent |
| 24 | XREFP | Reference input. DC bias is generated internally. Normally AC coupled externally. |
| 25 | VDDPD | Power supply for phase detector. Nominal + 3.3V. Decoupling for this supply is critical. 5 mA max., Fpd dependent. |
| 27 | CEN | CMOS input, hardware chip enable. |
| 28 | SEN | CMOS input, serial port latch enable. |
| 29 | SCK | CMOS input, serial port clock. |
| 30 | SDI | CMOS input, serial port data. |
| 31 | DVDD | Power supply for digital. Nominal + 3.3V, 25 mA max., Fpd dependent. |
| 32 | VDDIO | Power supply for digital I/O. Nominal + 3.3V, 8 mA max. (only when driving LD_SDO) |
| 33 | LD_SDO | CMOS output. General purpose output; lock detect, serial data out, others, selectable |
| 34 | VCCPS | Power supply for RF divider. Nominal + 3.3V, 35 mA max. |
| 36 | TRIG | CMOS input. External trigger. |
| 38 | RFOUT | RF output (AC coupled). |
| 40 | VCCVCO1 | Power Supply for VCO. Nominal +5V, High Current, VCO dependent |

[1] Pin is not connected internally, however, pin must be connected to GND to maintain product family pin for pin compatibility.

[2] BIAS ref voltage (pin 20) cannot drive an external load, and must be measured with a 10 GOhm meter such as Agilent 34410A; a typical 10 Mohm DVM will read erroneously.

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC767LP6CE from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

| Item | Contents | Part Number |
|---------------------|---|--------------------|
| Evaluation PCB Only | HMC767LP6CE Evaluation PCB | 130369-HMC767LP6CE |
| Evaluation Kit | HMC767LP6CE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation Software, Hittite PLL Design Software) | EKIT01-HMC767LP6CE |