Preliminary QCA4004 Dual-Band 1x1 802.11abgn Wi-Fi USB BT SoC

Data Sheet

80-Y-xxxxx Rev. A

March 2013

Confidential and Proprietary - Qualcomm Atheros, Inc.

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Revision history

Revision	Date	Description
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Contents

1 Introduction

1.1 General Description

The QCA4004 is a highly integrated, system-on-a-chip solution for 2.4/5 GHz IEEE 802.11n 1x1 WLAN for CE applications, providing improved link robustness, extended range, and increased throughput and performance.

The QCA4004 supports single stream 802.11n and includes the Qualcomm Atheros internal Efficient Power Amplifier™ (EPA) technology. It includes a highly integrated, front-end module (power amplifier, low-noise amplifier and RF switch for 2.4 GHz), enabling low-cost designs. Advanced architecture and protocol techniques save power during sleep, stand-by and active states.

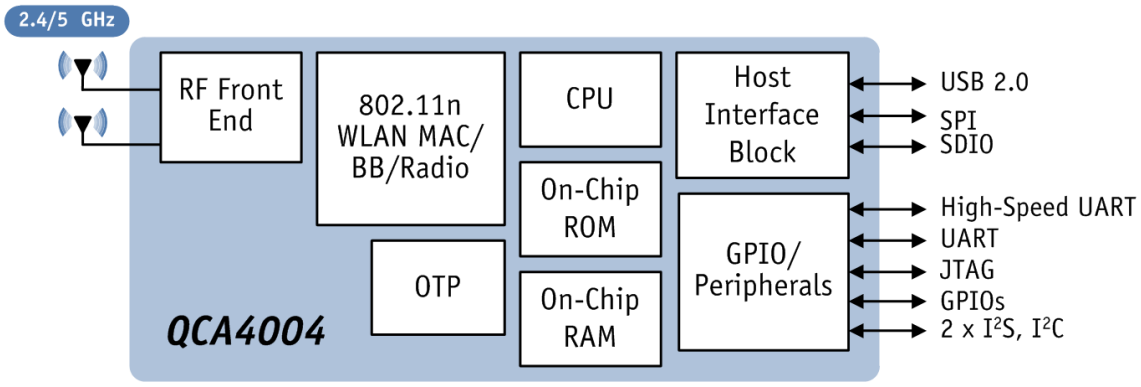
The QCA4004 supports USB, SDIO, and SPI host interfaces, and multiple peripheral interfaces including UART, SPI, I^2C and GPIO. All internal clocks generate from a single external crystal. The QCA4004 supports reference clocks ranging from 19.2 to 40 MHz, and is available in a 68-pin 8x8 mm LPCC package.

1.2 Features

- All-CMOS IEEE 802.11a/b/g/n 1x1 single-chip
- USB 2.0 at 480 Mbps using an integrated controller and PHY
- SDIO 2.0 interface with 200 Mbps throughput
- Extensive hardware support for WLAN coexistence through LPC message passing
- Power and clock management for extended battery life
- Green-Tx power saving
- Low-power listen mode and radio retention for reduced receive power consumption and sleep current
- Support for transmit beamformee (TxBFee)
- Internal OTP memory for calibration data
- Integrated PA, LNA minimizing external component count
- Integrated RF switch for 2.4 GHz
- Optional external PA, LNA support
- Data rates of up to 54 Mbps for 802.11a/g and 72.2 for 802.11n HT20, 150 Mbps for HT40
- Advanced power management to minimize standby, sleep and active power

- Security support for WPS, WPA2, WPA, WAP and protected management frames
- Full 802.11e QoS support including WMM and U-APSD
- 802.11e-compatible bursting
- Support for the IEEE 802.11e, h, i, and j
- WEP, TKIP, and AES hardware encryption
- Reduced (short) guard interval
- Frame aggregation with A-MPDU
- Block ACK
- UART for console support
- JTAG-based processor debugging supported
- 68-pin, 8 mm x 8 mm LPCC package

1.3 System Block Diagram



2 Functional Description

2.1 Overview

The QCA4004 is a single chip 1x1 802.11a/b/g/n MIMO solution optimized for low-power embedded applications with single-stream capability for both transmit and receive. Frame aggregation, reduced inter-frame spacing (RIFS), and half guard intervals provide improved throughput on the link. Additional 802.11n performance optimization, such as 802.11n frame aggregation (A-MPDU and A-MSDU), is provided by drivers that support SDIO bus transaction bundling (a form of bus aggregation) and low-overhead host assisted buffering (Rx A-MSDU and A-MPDU). These techniques can improve the performance and efficiency of applications involving large bulk data transfers (for example, file transfers or high-resolution video streaming). The typical data path consists of the host interface, mailbox DMA, AHB, memory controller, MAC, BB, and radio. The CPU drives the control path via register and memory access. External interfaces include USB LPM, SDIO or SPI slave, reference clock, and front-end components, as well as optional connections such as UART, SPI/I^2C, GPIO, JTAG. See the "System Block Diagram" on page 5.

2.2 XTENSA CPU

The QCA4004 uses an XTENSA CPU. The CPU is connected to a large 448 KB RAM block that precludes the need for external memory. The CPU has 768 KB internal ROM. The CPU connects to the main AHB bus through its peripheral interface (PIF). It also has a JTAG interface for debugging.

The CPU's internal logic and boot code detect the presence of and automatically begin communicating with an external host. The CPU communicates directly with the RAM and ROM modules within the device without any caching.

2.3 AHB and APB Blocks

The AHB block acts as an arbiter. It has AHB interfaces from the masters:

- MAC
- MBOX
- CPU
- USB

Depending upon the address, the AHB data request can go into one of the two slaves: APB block or the CPU PIF. Data requests to the CPU PIF are generally high-speed memory requests, while requests to the APB block are primarily meant for register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within the QCA4004's main blocks. Depending on the address, the APB request can go to:

- Radio
- SI/SPI
- MBOX
- GPIO
- UART
- Real Time Clock (RTC)
- MAC/BB

2.4 Master SI/SPI Control

The QCA4004 has a master serial interface (SI) that can operate in two or four-wire bus configurations to control EEPROMs or other I^2C/SPI devices. Multiple I^2C devices with different device addresses are supported by sharing the two-wire bus. Multiple SPI devices are supported by sharing the clock and data signals and using separate software-controlled GPIO pins as chip selects.

An SI transaction consists of two phases: a data transmit phase of 0-8 bytes followed by a data receive phase of 0-8 bytes. The flexible SI programming interface allows software to support various address and command configurations in I^2C/SPI devices. In addition, software may operate the SI in either polling or interrupt mode.

2.5 GPIO

The QCA4004 has GPIO pins with direct software access. Many are multiplexed with other functions such as the host interface, UART, SI, Bluetooth coexistence, etc. Each GPIO supports these configurations via software programming:

- Internal pull-up/pull-down options
- Input available for sampling by software registers
- Input triggering an edge or level CPU interrupt
- Input triggering a level chip wakeup interrupt
- Open-drain or push-pull output driver
- Output source from a software register or the Sigma Delta Pulse-width Modulation (PWM) DAC
- When the QCA4004 is in SLEEP mode, it can be woken up with a GPIO-level interrupt

The QCA4004 has one Sigma Delta PWM DAC shared by all its GPIO pins. It allows the GPIO pins to approximate intermediate output voltage levels. The DAC has a period of 256 samples with a software controllable duty cycle. In applications where the QCA4004 is driving LEDs using GPIO pins, the Sigma Delta PWM DAC can provide a continuous dimmer function.

2.6 MBOX

The MBOX is a service module to handle one of two possible external hosts: SDIO or SPI slave. The QCA4004 can handle only one of these hosts at any given time. The type of host the QCA4004 uses depends upon the polarity of some pins upon system power up. The MBOX has two interfaces: an APB interface for access to the MBOX registers and an AHB interface used by the external host to access MC memory or other registers within the QCA4004.

2.7 HCI UART Over SDIO–BT and GPS

The QCA4004 has a high-speed HCI UART that connects to an external Bluetooth chip though its HCI interface. This UART can directly transfer data between the host and Bluetooth or GPS device.

2.8 Debug UART

The QCA4004 includes a high-speed UART interface fully compatible with the 16550 UART industry standard. This UART is a general purpose UART although it is primarily used for debug.

2.9 Reset Control

The QCA4004 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal deasserts, the QCA4004 waits for host communication or boots from flash. Until then, the MAC, BB, and SoC blocks are powered off and all modules except the host interface are held in reset.

Once the host initiates communication, the QCA4004 turns on its crystal and later its PLLs. After all clocks are stable and running, resets to all blocks are automatically deasserted.

2.10 Reset Sequence

For USB boot, after the CHIP_PWD_L deasserts, the QCA4004 enters WAKEUP, then 2 mS later, it enters the ON state where the CPU starts running. For SDIO/SPI boot, upon deassertion of CHIP_PWD, the QCA4004 enters HOST_OFF and waits for communication from the host. A host transaction is required to put the QCA4004 into WAKEUP, then 2 mS later, it enters the ON state where the CPU begins execution.

2.11 Power Management Unit

The QCA4004 has an integrated power management unit (PMU) that generates all power supplies required by its internal circuitry from a 3.3 V supply.

The main components of the PMU are:

- A switching regulator (SWREG) produces a 1.2 V supply from a 3.3 V input supply.
- A linear regulator also produces a 1.2 V supply, originating from the SWREG 3.3 V input. There is a board option provided to select the switching regulator or linear regulator as a 1.2 V supply.
- A linear regulator (SREG) that converts the host I/O supply to a 1.2 V supply for some small control blocks, which turns on when CHIP_PWD_L is deasserted.

2.12 Power Transition Diagram

The QCA4004 provides integrated power management and control functions and extremely low power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unnecessary high speed clock sources
- Reducing voltage levels to specific blocks in some states to save power

2.12.1 Hardware Power States

QCA4004 hardware has five top level hardware power states managed by the RTC block. Table 2-1 describes the input from the MAC, CPU, host (which could be USB, SDIO), interrupt logic, and timers that affect the power states to save power.

2.12.2 Sleep State Management

Sleep state minimizes power consumption while saving system states. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. For the QCA4004 to enter SLEEP state, the MAC, MBOX, and CPU systems must not be active.

The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the reference clock source to stabilize, then ungate all enabled clock trees. The CPU wakes up only when an interrupt arrives, which may have also generated the system WAKEUP event. See Table 2-1.

Table 2-1 Power Management States

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.
SLEEP	Only the sleep clock is operating.
	The crystal or oscillator is disabled.
	Any wakeup events (MAC, host, LF timer, GPIO interrupt) force a transition to WAKEUP.
	All internal states are maintained.
WAKEUP	The system transitions from sleep/OFF states to ON.
	The high frequency clock is gated off as the oscillator is brought up and the PLL is enabled.
	WAKEUP duration is usually 2 ms.
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	Lower-level clock gating is implemented at the block level, including the CPU, which can be gated off using WAITI instructions while the system is on. No CPU, host, or WLAN activities go to sleep.

Figure 2-1 depicts the power state transition.

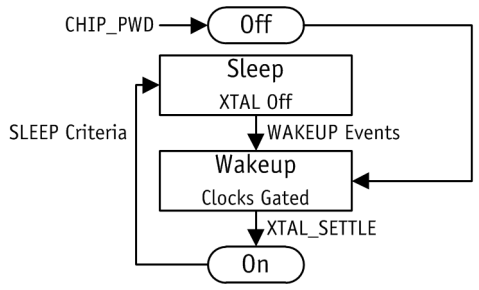


Figure 2-1 QCA4004 Power State

2.13 System Clocking (RTC Block)

The QCA4004 RTC block controls the clocks and power going to other internal modules. Its inputs are sleep requests from the modules, and its outputs are clock enable and power signals that gate clocks going to these modules. RTC also manages resets going to the modules with the device. QCA4004 has high-speed and low-speed clocking.

2.13.1 High Speed Clocking

The reference clock source drives the PLL and RF synthesizer within the QCA4004. It can be an external crystal or oscillator. For minimal power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, and OFF states. For an external crystal, the QCA4004 disables the on-chip oscillator driver. For an external oscillator, it deasserts CLK_REQ to indicate no reference clock is needed.

When exiting SLEEP state, the QCA4004 waits in WAKEUP state for a programmable duration. During this time, CLK_REQ is asserted to allow the reference clock source to settle. The CLK_ REQ signal remains asserted in ON state.

The QCA4004 supports reference clock sharing in all power states. For an external crystal, the on-chip oscillator driver drives a reference clock output when an external clock request signal is asserted. For an external oscillator, the external clock request signal is forwarded on the CLK_ REQ signal, and the input clock is passed along to the reference clock output.

2.13.2 Low-Speed Clocking

The QCA4004 eliminates the need for an external sleep clock source, reducing system cost. It uses an internal ring oscillator that generates a low frequency sleep clock and runs state machines and counters related to low power states.

The internal calibration module produces a 32.768 KHz output with minimal variation, for which it uses the reference clock source as the golden clock. The calibration module adjusts for process and temperature variations in the ring oscillator when the system is ON.

2.13.3 Interface Clock

The host interface clock comes from the SDIO or SPI slave host and is completely independent from the other internal clocks. It drives the host interface logic and certain registers accessed by the host in HOST_OFF and SLEEP states.

2.14 Front End Control

For applications that use external front-end components, the QCA4004 provides the ability to control them with four antenna switch control outputs named as follows:

- ANTA
- ANTB
- ANTC
- ANTD

A programmable switch table indexed by transceiver state offers flexibility for various front-end configurations. The QCA4004 supports antenna sharing with another wireless or Bluetooth chip in all power states by using ANTD to control the shared antenna switch.

2.15 MAC/BB/RF Block

The QCA4004 Wireless MAC consists of five major blocks:

- Host interface unit (HIU) for bridging to the AHB for bulk data accesses and APB for register accesses
- Ten queue control units (QCU) for transferring Tx data
- Ten DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring Rx data

The QCA4004 baseband module (BB) is the physical layer controller for the IEEE802.11a/b/g/n air interface. It is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

2.16 Design for Test

The QCA4004 has a built in JTAG boundary scan of its pins. It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2.17 Interface Selection

The QCA4004 supports multiple interfaces including SDIO, SPI, I^2S, I^2C, USB, UART and JTAG. It is possible to configure the QCA4004 to support any of these interfaces by connecting certain inputs externally. Table 2-2 illustrates the GPIO pins that select these interfaces.

Table 2-2 Interface Selection by GPIO

GPIO	SDIO WLAN	USB WLAN with 2 Audio streams	USB WLAN with BT Coexistence
GPIO0	SDIO_CMD	GPIO / I2C_WP	XLNA0
GPIO1	SDIO_D3	I2S_BCLK1	BT_ACTIVE
GPIO2	SDIO_D2	I2S_SDI1	BT_PRIORITY
GPIO3	SDIO_D1	I2S_SDO1	BT_FREQ
GPIO4	SDIO_D0	I2S_WS1	WLAN_ACTIVE
GPIO5	SDIO_CLK	I2S_MCLK	XLNA1
GPIO6	DEBUG_UART_RXD/TDI	DEBUG_UART_RXD/TDI	DEBUG_UART_RXD
GPIO7	DEBUG_UART_TXD	DEBUG_UART_TXD	DEBUG_UART_TXD
GPIO8	GPIO/XLNA0	UART_RTS	CLK_REQ_IN
GPIO9	GPIO/XLNA1	UART_CTS	CLK_REQ_OUT
GPIO10	GPIO/TMS	I2S_MCLK/TMS	UART_RXD/TMS
GPIO11	GPIO	I2S_BCLK	UART_TXD
GPIO12	I2C_SCK/TCK	I2C_SCK/TCK	I2C_SCK/TCK
GPIO13	I2C_SDA/TDO	I2C_SDA/TDO	I2C_SDA/TDO
GPIO15	SPIM_CLK	SPIM_CLK	SPIM_CLK
GPIO16	SPIM_CS	SPIM_CS	SPIM_CS
GPIO17	SPIM_MOSI	SPIM_MOSI	SPIM_MOSI
GPIO18	SPIM_MISO	SPIM_MISO	SPIM_MISO
GPIO19	GPIO	I2S_SDI	UART_RTS
GPIO20	GPIO/DEBUG_UART_TXD	I2S_SDO	UART_CTS
GPIO21	GPIO/DEBUG_UART_RXD	I2S_WS	UART_RXD

Table 2-3 IoT Interface Selection by GPIO

GPIO	Hosted	Hostless	SDIO
GPIO0	SPI_CS	SENSOR1_SPIM_CS	XLNA0
GPIO1	SPI_MOSI	SENSOR0_INT	BT_ACTIVE
GPIO2	GPIO/LED	GPIO	BT_PRIORITY
GPIO3	SPI_INT	SENSOR1_INT	BT_FREQ
GPIO4	SPI_MISO	SENSOR2_INT	WLAN_ACTIVE
GPIO5	SPI_CLK	SENSOR2_SPIM_CS	XLNA1
GPIO6	DEBUG_UART_RXD/TDI	DEBUG_UART_RXD/TDI	DEBUG_UART_RXD
GPIO7	DEBUG_UART_TXD	DEBUG_UART_TXD	DEBUG_UART_TXD
GPIO8	UART_RTS	UART_RTS	UART_RTS
GPIO9	UART_CTS	UART_CTS	UART_CTS
GPIO10	UART_RXD/TMS	UART_RXD/TMS	UART_RXD/TMS
GPIO11	UART_TXD	UART_TXD	UART_TXD
GPIO12	I2C_SCK/TCK	I2C_SCK/TCK	I2C_SCK/TCK
GPIO13	I2C_SDA/TDO	I2C_SDA/TDO	I2C_SDA/TDO
IOT_MODE_EN	IOT_MODE_EN	IOT_MODE_EN	IOT_MODE_EN
GPIO15	SPIM_CLK	SPIM_CLK	SPIM_CLK
GPIO16	SPIM_CS0	SPIM_CS0	SPIM_CS0
GPIO17	SPIM_DIO0	SPIM_DIO0	SPIM_DIO0
GPIO18	SPIM_DIO1	SPIM_DIO1	SPIM_DIO1
GPIO19	SPIM_DIO2	SPIM_DIO2	SPIM_DIO2
GPIO20	SPIM_DIO3	SPIM_DIO3	SPIM_DIO3
GPIO21	SPIM_CS1/LED	SENSOR0_SPIM_CS/LED	SPIM_CS1/LED

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the QCA4004. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

NOTE Maximum rating for signals follows the supply domain of the signals.

Table 3-1 Absolute Maximum Ratings

Symbol (Domain)	Description	Max Rating	Unit
VDDIO_GPIO	I/O supply for GPIO18-GPIO25 pins	–0.3 to 4.0	V
VDDIO_SDIO	I/O supply for GPIO0-GPIO13 pins	–0.3 to 4.0	V
DVDD12	Digital 1.2 V supply[1]	–0.3 to 1.32	V
SWREG_FB_VDD12			
VDD12_BB_PLL	1.2 V supply for analog BB PLL	–0.3 to 1.32	V
VDD12_RF	1.2 V supply for analog RF	–0.3 to 1.32	V
VDD12_SYNTH	1.2 V supply for analog SYNTH	–0.3 to 1.32	V
VDD33_ANT	Antenna control I/O supply	–0.3 to 4.0	V
VDD33_RF	3.3 V supply for analog RFs	–0.3 to 4.0	V
VDD33_SYNTH	3.3 V supply for analog SYNTH	–0.3 to 4.0	V
VDD33	3.3 V supply for switching regulator/PMU	–0.3 to 4.0	V
SWREG_IN			
VDD33_PLL_XTAL	3.3 V supply for XTAL/PLL	–0.3 to 4.0	V
VDD33_USB	3.3 V supply for USB	–0.3 to 4.0	V
V_{IH} MIN	Minimum Digital I/O Input Voltage for 1.8 V or 3.3 V I/O Supply	–0.3	V
3.3 V I/O $_{VIH}$ MAX	Maximum Digital I/O Input Voltage for 3.3 V I/O Supply	V_{dd} +0.3	V
RF_{in}	Maximum RF input (reference to 50-Ω input)	+10	dBm
T_{store}	Storage Temperature	–45 to 135	°C
T_j	Junction Temperature	TBD	°C
ESD	Electrostatic Discharge Tolerance	TBD	V

1. DVDD12 and SWREG_FB are connected through an external LC filter to the SWREG_OUT pin. See Figure 3-1.

3.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VDDIO_GPIO	I/O supply for GPIO18-GPIO25 pins	1.71	—	3.46	V
VDDIO_SDIO	I/O supply for GPIO0-GPIO13 pins	1.71	—	3.46	V
DVDD12	Digital 1.2 V supply[1]	1.14	1.2	1.26	V
SWREG_FB_VDD12					
VDD12_BB_PLL, VDD12_SYNTH, VDD12_RF	Analog 1.2 V supplies	1.14	1.2	1.26	V
VDD33	Internal switching regulator supply	3.14	3.3	3.46	V
SWREG_IN					
VDD33_ANT	Antenna control I/O supply	3.14	3.3	3.46	V
VDD33_RF, VDD33_SYNTH, VDD33_PLL_XTAL, VDD33_USB	Analog 3.3 V supplies	3.14	3.3	3.46	V
T_{case}	Case temperature	TBD	—	TBD	°C
Psi_{JT}	Thermal Parameter[2]	—	3	—	°C/W

1. DVDD12 and SWREG_FB_VDD12 are connected through an external LC filter to the SWREG_OUT pin. See Figure 3-1.
2. The thermal parameter is for the 7x7 LPCC package.

3.3 General DC Electrical Characteristics

These conditions apply to all DC characteristics unless otherwise specified:

T_{amb} = 25 °C, V_{dd33}= 3.3 V

Table 3-3 DC Electrical Characteristics for Digital I/Os

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	—	1.8	—	3.6	V
V_{IL}	Low Level Input Voltage	—	–0.3	—	0.3	V
V_{OH}	High Level Output Voltage	—	2.2	—	3.3	V
V_{OL}	Low Level Output Voltage	—	0	—	0.4	V
I_{IL}	Low Level Input Current	—	—	—	15	µA
I_{OH}	High Level Output Current	—	—	—	8	mA
C_{IN}	Input Capacitance	—	—	3	—	pF

3.4 Internal Voltage Regulator

Figure 3-1 depicts the 1.2 V power supply regulated by the QCA4004. Refer to the reference design schematics for details.

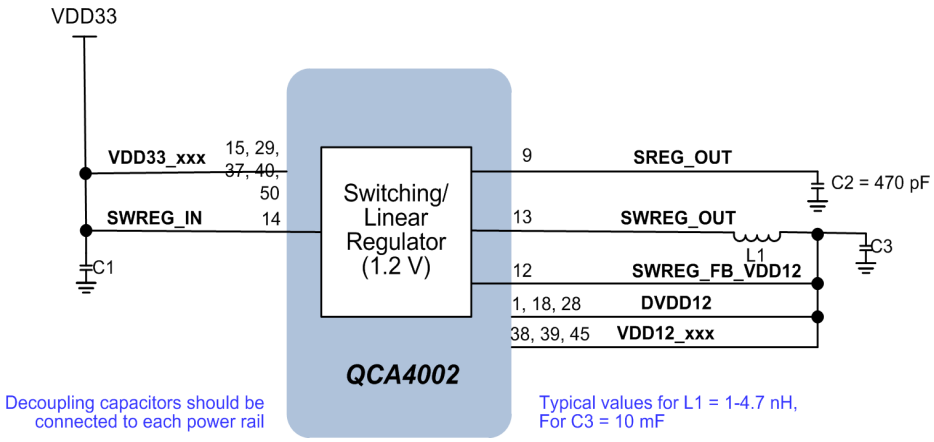


Figure 3-1 1.2 V Power Supply Regulated by the QCA4004

3.5 Radio Receiver Characteristics

Table 3-4, and Table 3-6 summarize the QCA4004 receiver characteristics.

Table 3-4 Receiver Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions[1]	Min	Typ[2]	Max	Unit
F_{rx}	Receive input frequency range	—	2.412	—	2.484	GHz
S_{rf}	Sensitivity					
	CCK, 1 Mbps		—	-95	—	dBm
	CCK, 2 Mbps		—	-93	—	
	CCK, 5.5 Mbps		—	-91	—	
	CCK, 11 Mbps		—	-88	—	
	OFDM, 6 Mbps		—	-92	—	
	OFDM, 9 Mbps		—	-91	—	
	OFDM, 12 Mbps		—	-91	—	
	OFDM, 18 Mbps		—	-89	—	
	OFDM, 24 Mbps		—	-85	—	
	OFDM, 36 Mbps		—	-82	—	
	OFDM, 48 Mbps		—	-78	—	
	OFDM, 54 Mbps		—	-76	—	
	HT20, MCS0		—	-92	—	
	HT20, MCS1		—	-89	—	
	HT20, MCS2		—	-87	—	
	HT20, MCS3		—	-85	—	
	HT20, MCS4		—	-83	—	
	HT20, MCS5		—	-78	—	
	HT20, MCS6		—	-77	—	
	HT20, MCS7		—	-72	—	
	HT40, MCS0		—	-90	—	
	HT40, MCS1		—	-87	—	
	HT40, MCS2		—	-85	—	
	HT40, MCS3		—	-83	—	
	HT40, MCS4		—	-81	—	
	HT40, MCS5		—	-76	—	
	HT40, MCS6		—	-75	—	
	HT40, MCS7		—	-70	—	

1. In LPL mode, sensitivity will be degraded by 1 - 2 dB.
2. Performance measured at the balun.

Table 3-5 Adjacent Channel Rejection for 2.4 GHz Operation

Symbol	Parameter	Conditions [1]	Min	Typ	Max	Unit
r_{adj}	Adjacent channel rejection					
	CCK, 1 Mbps	—	—	41	—	dB
	CCK, 11Mbps	—	—	38	—	
	OFDM, 6 Mbps	—	—	33	—	
	OFDM, 54 Mbps	—	—	20	—	
	HT20, MCS0	—	—	33	—	
	HT20, MCS7	—	—	23	—	

1. Performance measured at the balun.

Table 3-6 Receiver Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions [1 2]	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range	—	4.90	—	5.925	GHz
S_{rf}	Sensitivity					
	OFDM, 6 Mbps	—	—	-91	—	dBm
	OFDM, 9 Mbps	—	—	-90	—	
	OFDM, 12 Mbps	—	—	-90	—	
	OFDM, 18 Mbps	—	—	-88	—	
	OFDM, 24 Mbps	—	—	-84	—	
	OFDM, 36 Mbps	—	—	-81	—	
	OFDM, 48 Mbps	—	—	-77	—	
	OFDM, 54 Mbps	—	—	-74	—	
	HT20, MCS0	—	—	-90	—	
	HT20, MCS1	—	—	-87	—	
	HT20, MCS2	—	—	-85	—	
	HT20, MCS3	—	—	-82	—	
	HT20, MCS4	—	—	-80	—	
	HT20, MCS5	—	—	-75	—	
	HT20, MCS6	—	—	-73	—	
	HT20, MCS7	—	—	-71	—	

Table 3-6 Receiver Characteristics for 5 GHz Operation (cont.)

Symbol	Parameter	Conditions [1 2]	Min	Typ	Max	Unit
S_{rf} (cont.)	HT40, MCS0	—	—	-88	—	dBm
	HT40, MCS1	—	—	-85	—	
	HT40, MCS2	—	—	-83	—	
	HT40, MCS3	—	—	-80	—	
	HT40, MCS4	—	—	-77	—	
	HT40, MCS5	—	—	-72	—	
	HT40, MCS6	—	—	-71	—	
	HT40, MCS7	—	—	-68	—	

1. In LPL mode, sensitivity will be degrade by 1 - 2 dB.
2. Performance measured at the balun.

Table 3-7 Adjacent Channel Rejection for 5 GHz Operation

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
R_{adj}	Adjacent channel rejection					
	OFDM, 6 Mbps	—	—	23	—	dB
	OFDM, 54 Mbps	—	—	15	—	
	HT20, MCS0	—	—	23	—	
	HT20, MCS7	—	—	9	—	
	HT40, MCS0	—	—	22	—	
	HT40, MCS7	—	—	11	—	

1. Performance measured at the balun.

3.6 Radio Transmitter Characteristics

Table 3-8 and Table 3-9 summarize the transmitter characteristics for QCA4004.

Table 3-8 Transmitter Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range	—	2.412	—	2.484	GHz
P_{out}	Output power[1, 2]					
	11b mask compliant 1 Mbps	1 Mbps	—	20	—	dBm
	11g mask compliant 6 Mbps	6 Mbps	—	20	—	
	11g EVM compliant	54 Mbps	—	16	—	
	11n HT20 mask compliant	MCS0	—	20	—	
	11n HT40 mask compliant	MCS0	—	19	—	
	11n HT20 EVM compliant	MCS7	—	15	—	
	11n HT40 EVM compliant	MCS7	—	14	—	
A_{pc}	Accuracy of power control	—	—	±1.5	—	dB

1. Refer to IEEE 802.11 specification for transmit spectrum limits:
   - 802.11b mask (18.4.7.3)
   - 802.11g mask (19.5.4)
   - 802.11g EVM (17.3.9.6.3)
   - 802.11n HT20 mask (20.3.21.1)
   - 802.11n HT20 EVM (20.3.21.7.3)
2. Performance measured at the balun.

Table 3-9 Transmitter Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range		4.90	—	5.925	GHz
Pout	Output power[1]					
	11n HT20 mask compliant	MCS0	—	17.0	—	
	11n HT40 mask compliant	MCS0	—	16.0	—	dBm
	11a mask compliant	6 Mbps	—	17.0	—	
	11a EVM compliant	54 Mbps	—	10.0	—	
	11n HT20 EVM compliant	MCS7	—	9.0	—	
	11n HT40 EVM compliant	MCS7	—	8.0	—	
Apc	Accuracy of power control	—	—	±2.0	—	dB

1. Performance measured at the balun.

3.7 QCA4002 Synthesizer Characteristics

Table 3-10 and Table 3-11 summarize the synthesizer characteristics for the QCA4004.

Table 3-10 Synthesizer Composite Characteristics for 2.4 GHz Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_c	Center channel frequency	Center frequency at 5 MHz spacing	2.412	—	2.484	GHz
F_{ref}	Reference oscillator frequency	±20 ppm	—	40[1]	—	MHz
F_{step}	Frequency step size (at RF)		—	1	—	MHz

1. 26 MHzis the other supported frequency.

Table 3-11 Synthesizer Composite Characteristics for 5 GHz Operation

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_c	Center channel frequency	Center frequency at 5 MHz spacing	4.90	—	5.925	GHz
F_{ref}	Reference oscillator frequency	±20ppm	—	40[2]	—	MHz
F_{step}	Frequency step size (at RF)	[1]	—	5	—	MHz

1. 5 MHz channel spacing is for the 5.725 to 5.925 GHz band.
2. 26 MHzis the other supported frequency.

3.8 Typical Power Consumption Performance

3.8.1 Measurement Conditions for Low Power States

- T_ambient = 25°C
- All I/O pins except CHIP_PWD_L are maintained at their default polarities (I/Os without default internal pulls are pulled low). See Table 3-12.

Table 3-12 QCA4004 Typical Current Consumption – Low Power States at 3.3 V Operation

Mode	State	Typical Current Consumption for USB at 3.3 V	Typical Current Consumption for SDIO/SPI/UART at 3.3 V[4]
Standby	CHIP_PWD	5 uA	5 uA
	HOST_OFF	NA[1]	50 uA
	SLEEP/suspend	TBD[2]	TBD
PS (2.4 GHz) (without LPL enabled)	DTIM=1	2.6 mA[3]	2.6 mA[5]
	DTIM=3	1.4 mA[3]	1.4 mA[5]
	DTIM=10	0.9 mA[3]	0.9 mA[5]
PS (5 GHz) (without LPL enabled)	DTIM=1	1.8 mA[3]	1.8 mA[5]
	DTIM=3	1.1 mA[3]	1.1 mA[5]
	DTIM=10	0.8 mA[3]	0.8 mA[5]

1. Not applicable to USB
2. USB suspend
3. WoW standby
4. Measured using SDIO interface
5. Estimation Value

3.8.2 Measurement Conditions for Continuous Receive (2.4 GHz Operation)

Table 3-13 QCA4004 Typical Current Consumption (2.4 GHz operation) – Continuous Receive at 3.3 V Operation

Mode/Rate (Mbps)	Typical Current for USB [1] (mA)	Typical Current for SDIO/SPI/UART[2] (mA)
RX 11 Mbps	86	64
RX 54 Mbps	86	64
RX HT20 MCS0	86	64
RX HT20 MCS7	86	64
RX HT40 MCS0	98	74
RX HT40 MCS7	98	74

1. Using LPL
2. Measured using SDIO interface

T_ambient = 25°C

3.8.3 Measurement Conditions for Continuous Transmit (2.4 GHz Operation)

Table 3-14 QCA4004 Typical Current Consumption (2.4 GHz operation) – Continuous Transmit at 3.3V Operation

Rate	Target Output Power (dBm)	Typical Current Consumption for USB (mA)	Typical Current Consumption for SDIO/SPI/UART[1] (mA)
TX 1 Mbps	19.0	250	224
TX 11 Mbps	19.0	250	225
TX 54 Mbps	18.0	221	195
TX HT20 MCS0	20.0	265	241
TX HT20 MCS7	17.0	208	187

1. Measured using SDIO interface

- T_ambient = 25°C

3.8.4 Measurement Conditions for Continuous Receive (5 GHz Operation)

Table 3-15 QCA4004 Typical Current Consumption (5 GHz operation) – Continuous Receive at 3.3 V Operation

Mode/Rate (Mbps)	Typical Current for USB[1](mA)	Typical Current for SDIO/SPI/UART[2] (mA)
RX 54 Mbps	94	72
RX HT20 MCS0	93	71
RX HT20 MCS7	93	71
RX HT40 MCS0	99	78
RX HT40 MCS7	99	78

1. Using LPL
2. Measured using SDIO interface

- T_ambient = 25°C

3.8.5 Measurement Conditions for Continuous Transmit (5 GHz Operation)

Table 3-16 QCA4004 Typical Current Consumption (5 GHz operation) – Continuous Transmit at 3.3 V Operation

Mode/Rate (Mbps)	Target Output Power (dBm)	Typical Current Consumption for USB (mA)	Typical Current Consumption or SDIO/SPI/UART[1] (mA)
OFDM, 6 Mbps	17.0	265	242
OFDM 54 Mbps	15.0	221	201
HT20, MCS0	18.0	284	269
HT20, MCS7	10.5	189	165
HT40, MCS0	14.0	228	208
HT40, MCS7	10.5	189	165

1. Measured using SDIO interface

- T_ambient = 25°C

4 AC Specifications

4.1 External 19.2 / 25 / 26 / 40 MHz Reference Input Clock Timing

Figure 4-1 and Table 4-1 show the external 19.2/24/26/38.4/40/52 MHz reference input clock timing requirements.

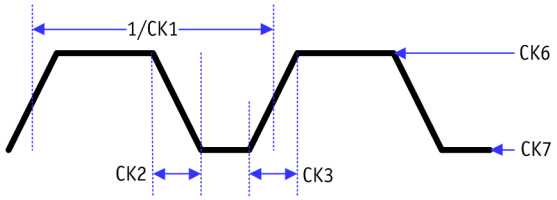


Figure 4-1 External 19.2/25/26/40MHz

Table 4-1 External 19.2/25/26/40 MHz Reference Input Clock Timing

Symbol	Description	Min	Typ	Max	Unit
CK2	Fall time	—	—	0.1 x period	ns
CK3	Rise time	—	—	0.1 x period	ns
CK4	Duty cycle (high-to-low ratio)	40	—	60	%
CK5	Frequency stability	–20	—	20	ppm
CK6	Input high voltage	0.75	—	1.26	V
CK7	Input low voltage	–0.55	—	0.3	V

4.2 SDIO/SPI Slave Interface Timing

Figure 4-2 shows the SDIO timing.

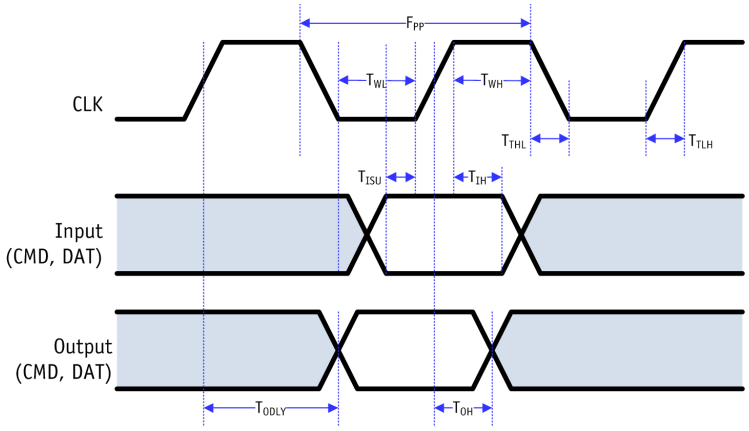


Figure 4-2 SDIO 2.0 Timing

Table 4-2 shows the values for timing constraints for SDIO.

Table 4-2 SDIO Timing Constraints

Parameter	Description	Min	Max	Unit	Note
f_{PP}	Clock frequency data transfer mode	0	50	MHz	40 pF C_L
t_{WL}	Clock low time	7	—	ns	40 pF C_L
t_{WH}	Clock high time	7	—	ns	40 pF C_L
t_{TLH}	Clock rise time	—	3	ns	40 pF C_L
t_{THL}	Clock fall time	—	3	ns	40 pF C_L
t_{ISU}	Input setup time	6	—	ns	40 pF C_L
t_{IH}	Input hold time	2	—	ns	40 pF C_L
t_{OH}	Output hold time	2.5	—	ns	40 pF C_L
$t_{O\_DLY\ (min)}$	Output delay time during data transfer mode	0	14	ns	40 pF C_L

Figure 4-3 shows the write timing for SPI slave style transactions.

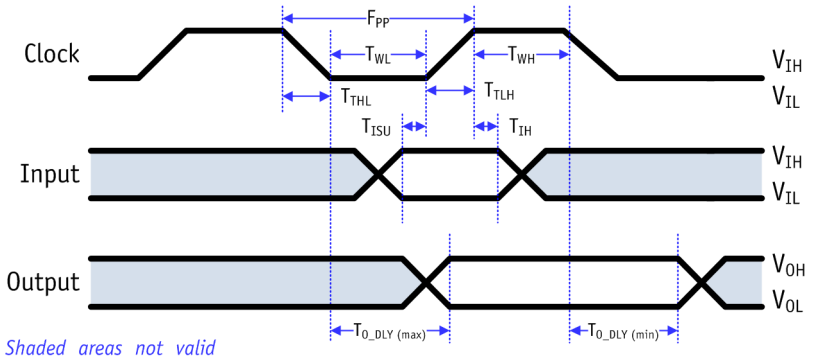


Figure 4-3 SPI Slave Timing

Table 4-3 shows the values for timing constraints for SPI slave.

Table 4-3 SPI Slave Timing Constraints

Parameter	Description	Min	Max	Unit
f_{PP}	Clock frequency	0	48	MHz
t_{WL}	Clock low time	8.3	—	ns
t_{WH}	Clock high time	8.3	—	ns
t_{TLH}	Clock rise time	—	2	ns
t_{THL}	Clock fall time	—	2	ns
t_{ISU}	Input setup time	5	—	ns
t_{IH}	Input hold time	5	—	ns
t_{O_DLY}	Output delay	0	5	ns

5 Pin Descriptions

This section contains both a package pinout (see Table 5-1) and tabular listings of the signal descriptions.

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types:

IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

Figure 5-1 shows the QCA4004 pinout. Refer also to the Package Dimensions in Table 6-1 on page 35.

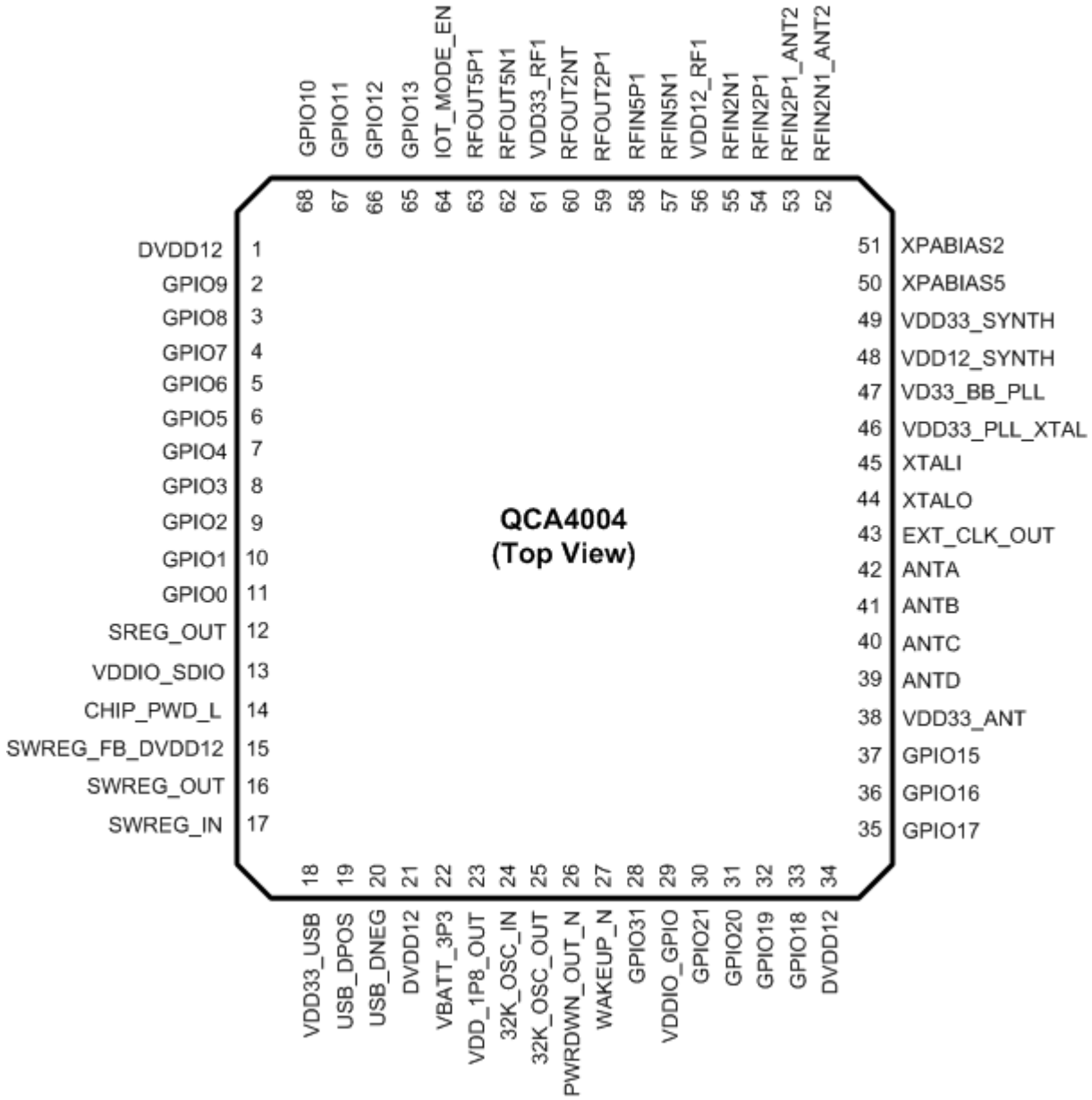


Figure 5-1 QCA4004 Package Pinout

Table 5-1 provides the signal-to-pin relationship information for the QCA4004.

Table 5-1 Signal to Pin Relationships and Descriptions

Signal Name	Pin	Type	Description
General			
EXT_CLK_OUT	43	O	External clock out: 40 or 26 MHz. Its corresponding half rate is available when configured.
XTALI	45	I/O	Supports 40 MHz or 26 MHz crystal.
XTALO	44	I	When an external reference clock is used, connect the clock signal to the XTALO pin and ground the XTALI pin.
Radio			
CHIP_PWD_L	14	I	Chip power-down control
RFIN2N1	55	IA	The first differential RF inputs
RFIN2P1	54	IA	
RFIN5N1	57	IA	
RFIN5P1	58	IA	
RFOUT2N1	60	OA	The first differential RF outputs
RFOUT2P1	59	OA	
RFOUT5N1	62	OA	
RFOUT5P1	63	OA	
RFIN2P1_ANT2	53	IA	The second differential RF inputs for 2.4GHz Rx/LNA diversity using two antennas
RFIN2N1_ANT2	52	IA	
Analog Interface			
XPABIAS2	51	OA	Bias for optional external power amplifier in 2.4 GHz
XPABIAS5	50	OA	Bias for optional external power amplifier in 5 GHz
External Switch Control			
ANTA	42	O	External RF switch control
ANTB	41	O	
ANTC	40	O	
ANTD	39	O	
USB			
USB_DPOS	19	IA/OA	USB D+ signal; carries USB data to and from the USB 2.0 PHY
USB_DNEG	20	IA/OA	USB D- signal; carries USB data to and from the USB 2.0 PHY

Table 5-1 Signal to Pin Relationships and Descriptions (cont.)

Signal Name	Pin	Type	Description
GPIO			
GPIO0	11	I/O	General purpose input/output. The QCA4004 supports a USB interface as well as an RGMII and an SDIO interface. It is possible to configure the QCA4004 to support any of these interfaces by tying certain inputs externally. See Interface Selection, page 2-14 for more information on GPIOs and interface options.
GPIO1	10	I/O	
GPIO2	9	I/O	
GPIO3	8	I/O	
GPIO4	7	I/O	
GPIO5	6	I/O	
GPIO6	5	I/O	
GPIO7	4	I/O	
GPIO8	3	I/O	
GPIO9	2	I/O	
GPIO10	68	I/O	
GPIO11	67	I/O	
GPIO12	66	I/O	
GPIO13	65	I/O	
GPIO15	37	I/O	
GPIO16	36	I/O	
GPIO17	35	I/O	
GPIO18	33	I/O	
GPIO19	32	I/O	
GPIO20	31	I/O	
GPIO21	30	I/O	
GPIO31	28	I/O	
I^2S			
Internal Switching Regulator			
SREG_OUT	12	P	1.2 V SDIO regulator output, connect to a 470pF bypass capacitor on the board
SWREG_OUT	16	P	Output of the switching regulator to an LC filter or the LDO
SWREG_IN	17	P	3.3 V input to the internal switching regulator or LDO

Signal Name	Pin	Description
Power		
DVDD12	1, 21, 34	Digital 1.2 V power supply, should be connected to the SWREG_FB pin.
SWREG_FB_DVDD12	15	Reference feedback voltage to the internal switching regulator or LDO
VBATT_3P3	22	Connect to 3.3 V host IO supply
VDD_1P8_OUT	23	1.8V LDO output, connect to a >1uF bypass capacitor on the board
VDD12_BB_PLL	47	Analog 1.2 V power supply, should be connected to the SWREG_FB pin.
VDD12_RF1	56	
VDD12_SYNTH	48	

Signal Name	Pin	Description
VDD33_ANT	38	Analog 3.3 V power supply
VDD33_RF1	61	
VDD33_PLL_XTAL	46	
VDD33_SYNTH	49	
VDD33_USB	18	Analog 3.3 V power supply, power regulator output
VDDIO_SDIO	13	Connect to 3.3 V host IO supply
VDDIO_GPIO	29	Connect to 3.3 V host IO supply or 1.8 V peripheral IO supply
VDD33_USB	18	I/O power supply
Ground		
GND	—	Exposed ground pad (See “Package Dimensions” on page 34.)

6 Package Dimensions

The QCA4004 is packaged in a LPCC package. The body size is 8 mm by 8 mm. The package drawings and dimensions are provided in Figure 6-1 and Table 6-1.

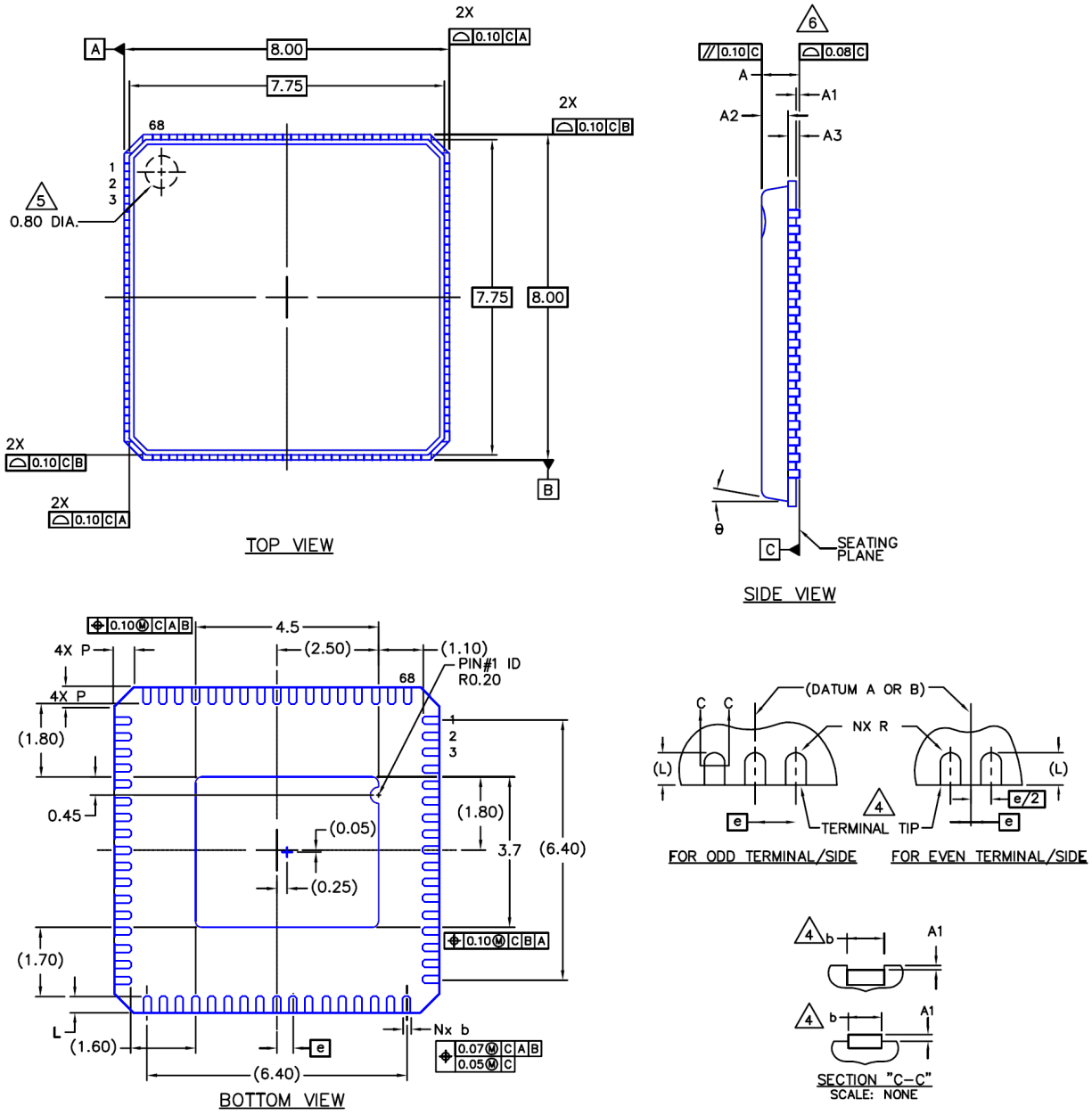


Figure 6-1 QCA4004 Package Drawing

Table 6-1 Package Dimensions

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	0.80	0.85	0.90	mm	0.315	0.335	0.354	inches
A1	0.00	0.01	0.05	mm	0.000	0.001	0.002	inches
A2	0.60	0.65	0.70	mm	0.236	0.256	0.276	inches
A3		0.20 REF		mm		0.008 REF		inches
θ	0	—	12	°	0	—	12	°
P	0.24	0.42	0.60	mm	0.094	0.165	0.236	inches
e		0.40 BSC		mm		0.157 BSC		inches
L	0.30	0.40	0.50	mm	0.118	0.157	0.197	inches
b	0.15	0.20	0.25	mm	0.059	0.079	0.098	inches

1. Controlling dimension: Millimeters
2. Reference document: 483287PO

7 Ordering Information

The order number QCA4004-AL3A specifies a lead-free standard-temperature version of the QCA4004.