HD74ACT161/HD74ACT163

Synchronous Presettable Binary Counter

HITACHI

Description

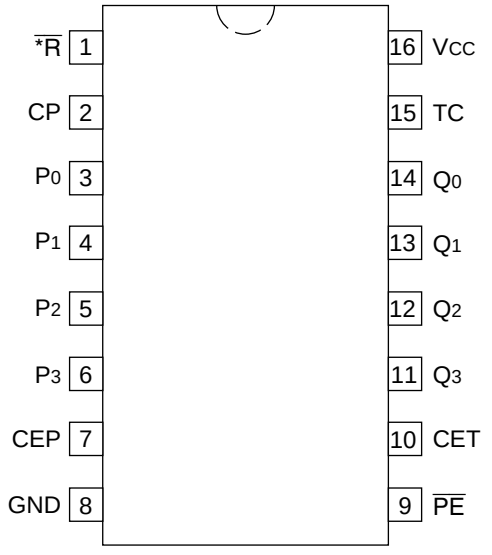
The HD74ACT161 and HD74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The HD74ACT161 have an asynchronous Master Reset input that overrides all other inputs and forces the outputs Low. The HD74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- HD74ACT161 and HD74ACT163 have TTL-Compatible Inputs

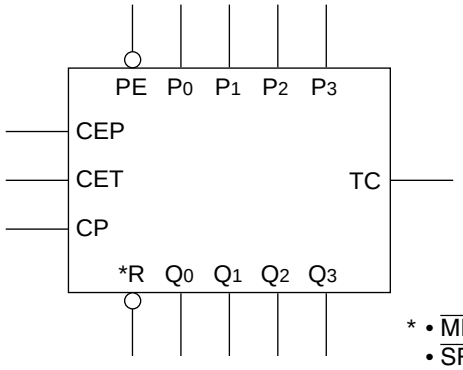
Hitachi semiconductor

Pin Arrangement



(Top view)

Logic Symbol



* • $\overline{MR}$ for HD74ACT161
  • $\overline{SR}$ for HD74AC163/HD74ACT163

Pin Names

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ (HD74ACT161)	Asynchronous Master Reset Input
$\overline{SR}$ (HD74ACT163/HD74ACT163)	Synchronous Reset Input
P_0 to P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0 to Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Functional Description

The HD74ACT161 and HD74ACT163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the HD74ACT161) occur as a reset of, and synchronous with, the Low-to-High transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (HD74ACT161), synchronous reset (HD74ACT163), parallel load, countup and hold. Five control inputs – Master Reste ($\overline{MR}$, HD74ACT161), Synchronous Reset ($\overline{SR}$, HD74ACT163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) – determine the mode of operation, as shown in the Mode Select Table. A Low signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs Low. A Low signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go Low on the next rising edge of CP. A Low signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (Pn) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (HD74ACT161) or $\overline{SR}$ (HD74ACT163) High, CEP and CET permit counting when both are High. Conversely, a Low signal on either CEP or CET inhibits counting.

The HD74ACT161 and HD74ACT163 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. The Terminal Count (TC) output is High when CET is High and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = $CEP \bullet CET \bullet \overline{PE}$

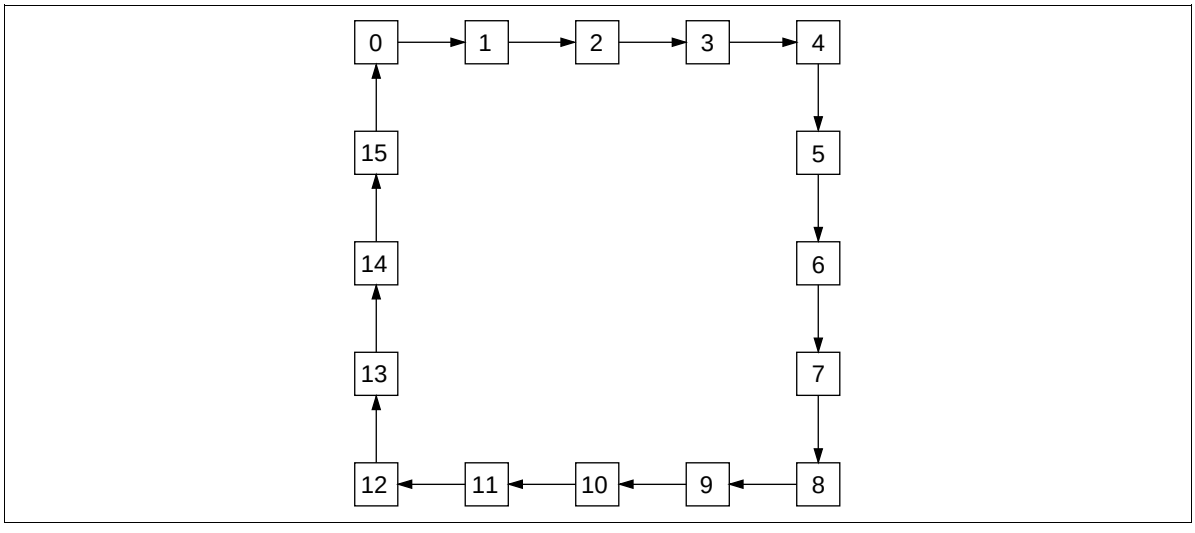
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

Mode Select Table

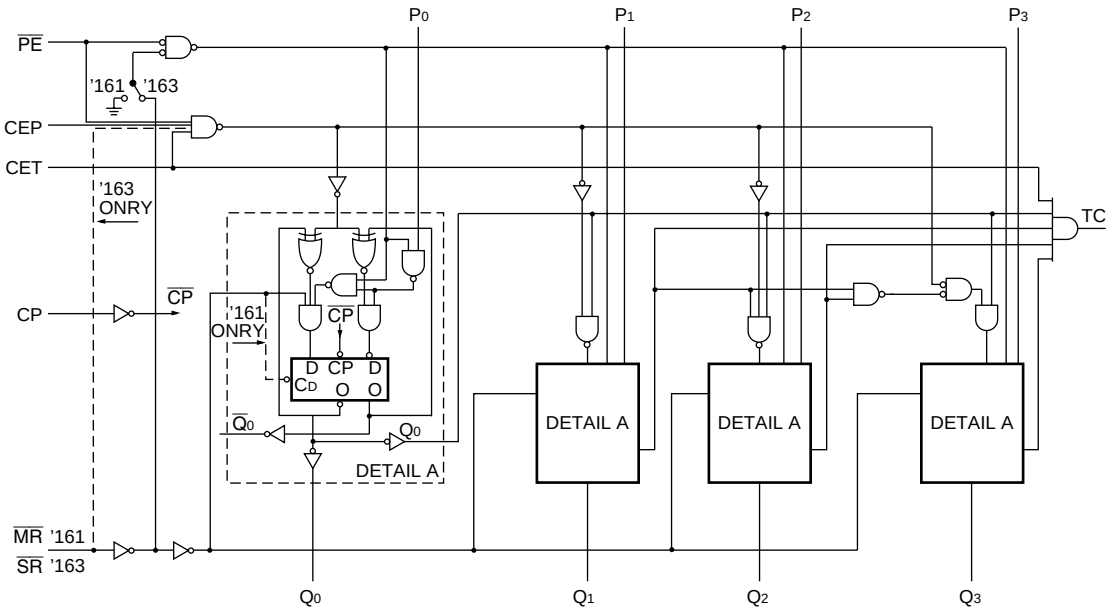
$\overline{SR}$*[1]	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐¬)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (Pn → Qn)
H	H	H	H	Count (Increment)
H	H	L	X	No change (Hold)
H	H	X	L	No change (Hold)

Note: 1. For HD74AC163/HD74ACT163
H : High Voltage Level
L : Low Voltage Level
X : Immaterial

State Diagram



Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	8.0	μA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = 25°C
Maximum additional I_{CC}/input (HD74ACT161/HD74ACT163)	I_{CCT}	1.5	mA	V_{IN} = V_{CC} – 2.1 V, V_{CC} = 5.5 V, Ta = Worst case

AC Characteristics: HD74ACT161

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum count frequency	f_{max}	5.0	115	125	—	100	—	MHz
Propagation delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	t_{PLH}	5.0	1.0	5.5	9.5	1.0	10.5	ns
Propagation delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	t_{PLH}	5.0	1.0	6.0	10.5	1.0	11.5	ns
Propagation delay CP to TC	t_{PLH}	5.0	1.0	7.0	11.0	1.0	12.5	ns
Propagation delay CP to TC	t_{PHL}	5.0	1.0	8.0	12.5	1.0	13.5	ns
Propagation delay CET to TC	t_{PLH}	5.0	1.0	5.5	8.5	1.0	10.0	ns
Propagation delay CET to TC	t_{PHL}	5.0	1.0	6.0	9.5	1.0	10.5	ns
Propagation delay $\overline{MR}$ to Q_n	t_{PHL}	5.0	1.0	6.0	10.0	1.0	11.0	ns
Propagation delay $\overline{MR}$ to TC	t_{PHL}	5.0	1.0	8.0	13.5	1.0	14.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT161

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF	Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Typ	Guaranteed Minimum		
Set-up time, HIGH or LOW P_n to CP	t_{su}	5.0	4.0	9.5	11.5	ns
Hold time, HIGH or LOW P_n to CP	t_h	5.0	–5.0	0	0	ns
Setup time, HIGH or LOW $\overline{MR}$ to CP	t_{su}	5.0	4.0	8.5	9.5	ns
Hold time, HIGH or LOW $\overline{MR}$ to CP	t_h	5.0	–5.5	–0.5	–0.5	ns
Setup time, HIGH or LOW $\overline{PE}$ to CP	t_{su}	5.0	4.0	8.5	9.5	ns
Hold time, HIGH or LOW $\overline{PE}$ to CP	t_h	5.0	–5.5	–0.5	–0.5	ns
Setup time, HIGH or LOW CEP or CET to CP	t_{su}	5.0	2.5	5.5	6.5	ns
Hold time, HIGH or LOW CEP or CET to CP	t_h	5.0	–3.0	0	0	ns
Clock pulse width (Load) HIGH or LOW	t_w	5.0	2.0	3.0	3.5	ns
Clock pulse width (Count) HIGH or LOW	t_w	5.0	2.0	3.0	3.5	ns
$\overline{MR}$ pulse width, LOW	t_w	5.0	3.0	3.0	7.5	ns
Recovery time $\overline{MR}$ to CP	t_{rec}	5.0	0	0	0.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	45.0	pF	V_{CC} = 5.0 V

AC Characteristics: HD74ACT163

			Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		
Item	**Symbol**	**V_{cc} (V)*[1]**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
Maximum count frequency	f_{max}	5.0	120	128	—	105	—	MHz
Propagation delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	t_{PLH}	5.0	1.0	5.5	10.0	1.0	11.0	ns
Propagation delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	t_{PHL}	5.0	1.0	6.0	11.0	1.0	12.0	ns
Propagation delay CP to TC	t_{PLH}	5.0	1.0	7.0	11.5	1.0	13.5	ns
Propagation delay CP to TC	t_{PHL}	5.0	1.0	8.0	13.5	1.0	15.0	ns
Propagation delay CET to TC	t_{PLH}	5.0	1.0	5.5	9.0	1.0	10.5	ns
Propagation delay CET to TC	t_{PHL}	5.0	1.0	6.0	10.0	1.0	11.0	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT163

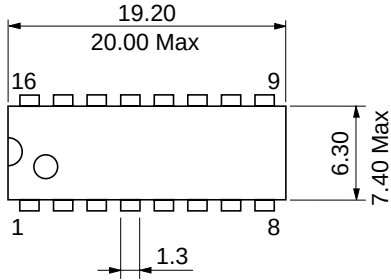
Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF	Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Typ	Guaranteed Minimum		
Set-up time, HIGH or LOW P_n to CP	t_{su}	5.0	4.0	10.0	12.0	ns
Hold time, HIGH or LOW P_n to CP	t_h	5.0	–5.0	0.5	0.5	ns
Setup time, HIGH or LOW $\overline{SR}$ to CP	t_{su}	5.0	4.0	10.0	11.5	ns
Hold time, HIGH or LOW $\overline{SR}$ to CP	t_h	5.0	–5.5	–0.5	–0.5	ns
Setup time, HIGH or LOW $\overline{PE}$ to CP	t_{su}	5.0	4.0	8.5	10.5	ns
Hold time, HIGH or LOW $\overline{PE}$ to CP	t_h	5.0	–5.5	–0.5	0	ns
Setup time, HIGH or LOW CEP or CET to CP	t_{su}	5.0	2.5	5.5	6.5	ns
Hold time, HIGH or LOW CEP or CET to CP	t_h	5.0	–3.0	0	0.5	ns
Clock pulse width (Load) HIGH or LOW	t_w	5.0	2.0	3.5	3.5	ns
Clock pulse width (Count) HIGH or LOW	t_w	5.0	2.0	3.5	3.5	ns

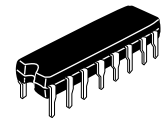
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

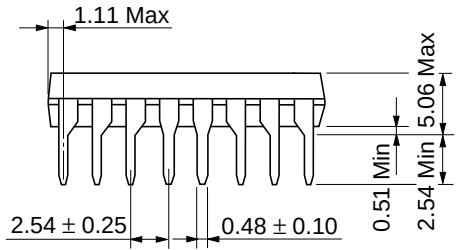
Capacitance

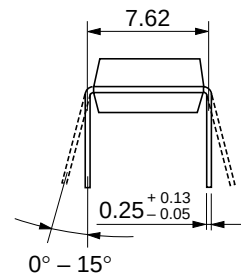
Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	45.0	pF	V_{CC} = 5.0 V

Unit: mm



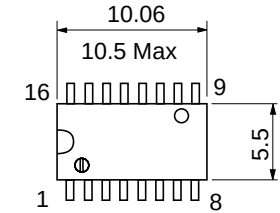


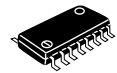


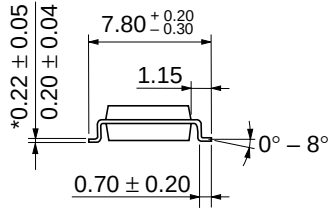


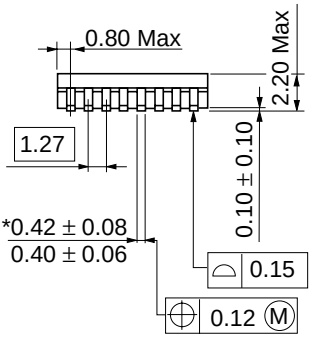
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





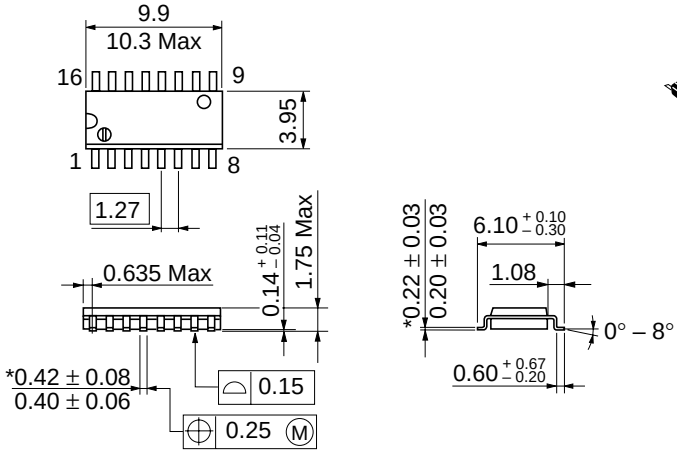


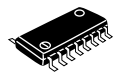


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm

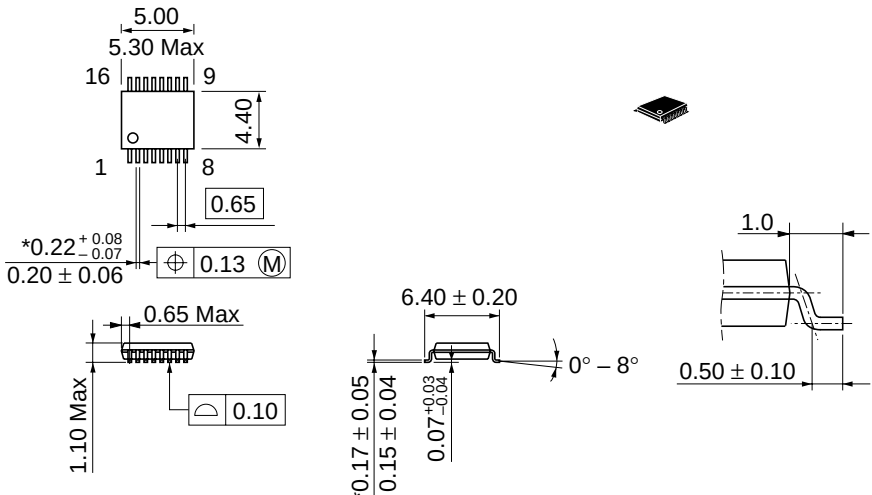




Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

*Dimension including the plating thickness
Base material dimension

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