ASM2P2310A

2.5-V TO 3.3-V High-Performance Clock Buffer

Features

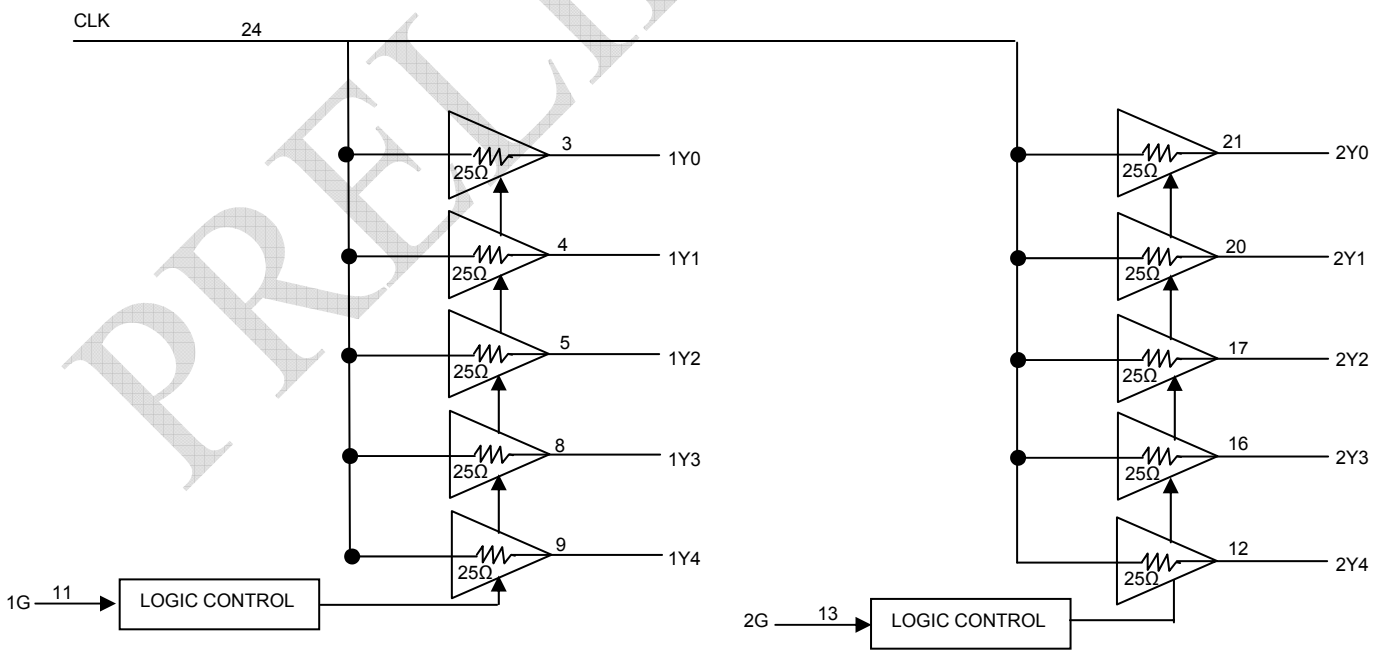
- High-Performance 1:10 Clock Driver for General Purpose applications. Operates up to 200 MHz at 3.3V Supply Voltage
- Pin-to-Pin Skew < 100 pS at 3.3V Supply Voltage
- Supply Range : 2.3V to 3.6V
- Operating Temperature Range : -40°C to 85°C
- Output Enable Glitch Suppression
- Distributes One Clock Input to Two Banks of Five Outputs
- 25Ω On Chip Series Damping Resistors
- Packaged in 24 Pin TSSOP Package

Product Description

The ASM2P2310A is a high-performance, low-skew clock buffer that operates up to 200MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5V and 3.3V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The ASM2P2310A is characterized for operation from -40°C to 85°C.

Block Diagram



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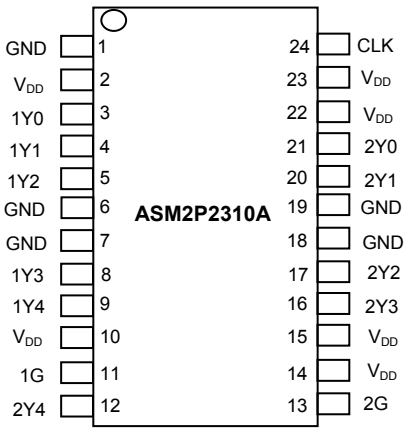
Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
1	GND	P	Ground Pin
2	V_{DD}	P	DC Power supply, 2.3 V – 3.6V
3	1Y0	O	Buffered Output Clock
4	1Y1	O	Buffered Output Clock
5	1Y2	O	Buffered Output Clock
6	GND	P	Ground Pin
7	GND	P	Ground Pin
8	1Y3	O	Buffered Output Clock
9	1Y4	O	Buffered Output Clock
10	V_{DD}	P	DC power supply, 2.3V – 3.6V
11	1G	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
12	2Y4	O	Buffered Output Clock
13	2G	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
14	V_{DD}	P	DC power supply, 2.3V – 3.6V
15	V_{DD}	P	DC power supply, 2.3V – 3.6V
16	2Y3	O	Buffered Output Clock
17	2Y2	O	Buffered Output Clock
18	GND	P	Ground Pin
19	GND	P	Ground Pin
20	2Y1	O	Buffered Output Clock
21	2Y0	O	Buffered Output Clock
22	V_{DD}	P	DC power supply, 2.3V – 3.6V
23	V_{DD}	P	DC power supply, 2.3V – 3.6V
24	CLK	I	Input reference frequency

Function Table

Input			Output	
1G	2G	CLK	1Y[0:4]	2Y[0:4]
L	L	↓	L	L
H	L	↓	CLK[1]	L
L	H	↓	L	CLK[1]
H	H	↓	CLK[1]	CLK[1]

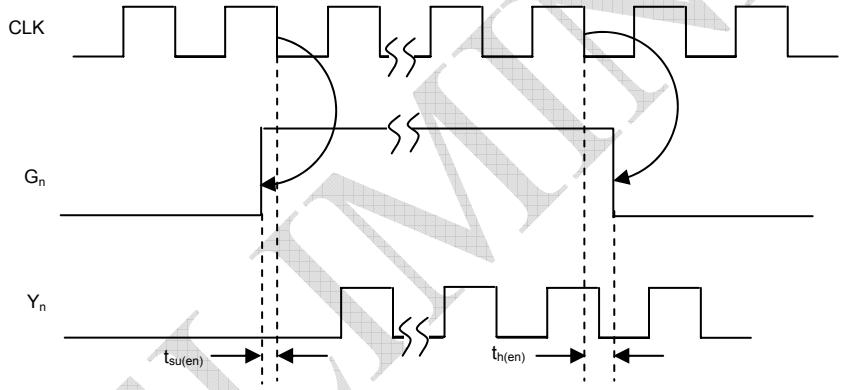
Note: 1 After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

Detailed Description

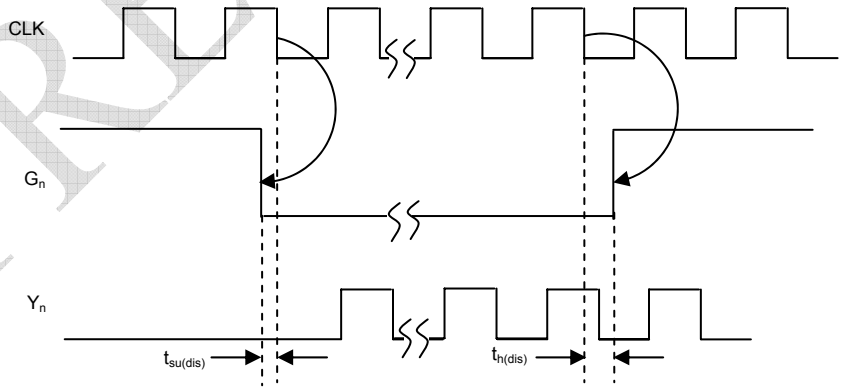
Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 1).

The G input must fulfill the timing requirements (t_{su}, t_h) according to the Switching Characteristics table for predictable operation.



a) Enable Mode



b) Disable Mode

Figure 1. Enable and Disable Mode Relative to CLK↓

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage range, V_{DD}	-0.5V to 4.6V
Input Voltage range, V_I[1,2]	-0.5 V to V_{DD} + 0.5 V
Output Voltage range, V_O[1,2]	-0.5 V to V_{DD} + 0.5 V
Continuous total output current, I_O (V_O = 0 to V_{DD})	±50 mA
Package thermal impedance, θ_{JA}[3]: PW package	120°C/W
Storage temperature range T_{stg}	-65°C to 150°C
Static Discharge Voltage , t_{DV} (As per JEDEC STD22- A114-B)	2KV
Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.	

Notes :
1 The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2 This value is limited to 4.6 V maximum.
3 The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions[1]

Parameter		Min	Typ	Max	Unit
Supply voltage, V_{DD}		2.3	2.5		V
			3.3	3.6	
Low-level input voltage, V_{IL}	V_{DD} = 3V to 3.6V			0.8	V
	V_{DD} = 2.3V to 2.7V			0.7	
High-level input voltage, V_{IH}	V_{DD} = 3V to 3.6V	2			V
	V_{DD} = 2.3V to 2.7V	1.7			
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	V_{DD} = 3V to 3.6V			12	mA
	V_{DD} = 2.3 V to 2.7V			6	
Low-level output current, I_{OL}	V_{DD} = 3V to 3.6V			12	mA
	V_{DD} = 2.3V to 2.7V			6	
Operating free-air temperature, T_A		-40		85	°C
Note:1 Unused inputs must be held high or low to prevent them from floating.					

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Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{IK}	Input voltage	V_{DD} = 3V, I_I = -18 mA			-1.2	V
I_I	Input current	V_I = 0V or V_{DD}			±5	µA
I_{DD}[2]	Static device current	CLK = 0V or V_{DD}, I_O = 0 mA			80	µA
C_I	Input capacitance	V_{DD} = 2.3V to 3.6V, V_I = 0V or V_{DD}		2.5		pF
C_O	Output capacitance	V_{DD} = 2.3V to 3.6V, V_I = 0V or V_{DD}		2.8		pF

Note: 1 All typical values are at respective nominal V_{DD}.
2 For I_{CC} over frequency, see Figure 6.

V_{DD} = 3.3 V ±0.3 V

Symbol	Parameter	Test Conditions		Min	Typ[1]	Max	Unit
V_{OH}	High-level output voltage	V_{DD} = Min to Max,	I_{OH} = -100 µA	V_{DD} - 0.2			V
		V_{DD} = 3 V	I_{OH} = -12 mA	2.1			
			I_{OH} = -6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = Min to Max,	I_{OL} = -100 µA			0.2	V
		V_{DD} = 3V	I_{OL} = 12mA			0.8	
			I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3V,	V_O = 1V	-28			mA
		V_{DD} = 3.3V,	V_O = 1.65V		-36		
		V_{DD} = 3.6V,	V_O = 3.135V			-14	
I_{OL}	Low-level output current	V_{DD} = 3V,	V_O = 1.95V	28			mA
		V_{DD} = 3.3V,	V_O = 1.65V		36		
		V_{DD} = 3.6V,	V_O = 0.4V			14	

Note: 1 All typical values are at respective nominal V_{DD}.

V_{DD} = 2.5 V ±0.2 V

Symbol	Parameter	Test Conditions		Min	Typ[1]	Max	Unit
V_{OH}	High-level output voltage	V_{DD} = Min to Max,	I_{OH} = -100 µA	V_{DD} - 0.2			V
		V_{DD} = 2.3V	I_{OH} = -6 mA	1.8			
V_{OL}	Low-level output voltage	V_{DD} = Min to Max,	I_{OL} = 100 µA			0.2	V
		V_{DD} = 2.3V	I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 2.3V,	V_O = 1V	-17			mA
		V_{DD} = 2.5V,	V_O = 1.25V		-25		
		V_{DD} = 2.7V,	V_O = 2.375V			-10	
I_{OL}	Low-level output current	V_{DD} = 2.3V,	V_O = 1.2V	17			mA
		V_{DD} = 2.5V,	V_O = 1.25V		25		
		V_{DD} = 2.7V,	V_O = 0.3V			10	

Note: 1 All typical values are at respective nominal V_{DD}.

Timing Requirements

Over recommended ranges of supply voltage and operating free-air temperature

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{clk}	Clock frequency	V_{DD} = 3 V to 3.6V	0		200	MHz
		V_{DD} = 2.3 V to 2.7V	0		170	

Switching Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

V_{DD} = 3.3 V ±0.3 V (See Figure 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} / t_{PHL}	CLK to Yn	f = 0 MHz to 200 MHz For circuit load, see Figure 2.	1.3		2.8	nS
$t_{sk(o)}$	Output skew (Ym to Yn)[1](see Figure 4)				100	pS
$t_{sk(p)}$	Pulse skew (see Figure 5)				250	pS
$t_{sk(pp)}$	Part-to-part skew				500	pS
t_r	Rise time (see Figure 3)	V_O = 0.4V to 2V	0.7		2	V/nS
t_f	Fall time (see Figure 3)	V_O = 2 V to 0.4V	0.7		2	V/nS
$t_{su(en)}$	Enable setup time,G_high before CLK↓		0.1			nS
$t_{su(dis)}$	Disable setup time, G_low before CLK↓		0.1			nS
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4			nS
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4			nS

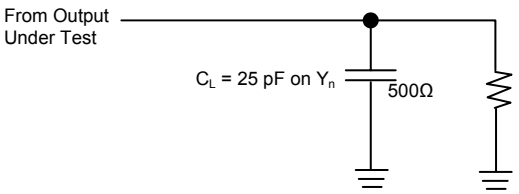
Note: 1 The $t_{sk(o)}$ specification is only valid for equal loading of all outputs

V_{DD} = 2.5 V ±0.2 V (See Figure 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} / t_{PHL}	CLK to Yn	f = 0MHz to 170MHz For circuit load, see Figure 2.	1.5		3.5	nS
$t_{sk(o)}$	Output skew (Ym to Yn)[1](see Figure 4)				170	pS
$t_{sk(p)}$	Pulse skew (see Figure 5)				400	pS
$t_{sk(pp)}$	Part-to-part skew				600	pS
t_r	Rise time (see Figure 3)	V_O = 0.4V to 1.7V	0.5		1.4	V/nS
t_f	Fall time (see Figure 3)	V_O = 1.7V to 0.4V	0.5		1.4	V/nS
$t_{su(en}$	Enable setup time,G_high before CLK↓		0.1			nS
$t_{su(dis)}$	Disable setup time, G_low before CLK↓		0.1			nS
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4			nS
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4			nS

Note: 1 The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 200 MHz, Z_O = 50Ω, t_r < 1.2 ns, t_f < 1.2 ns.

Figure 2. Test Load Circuit

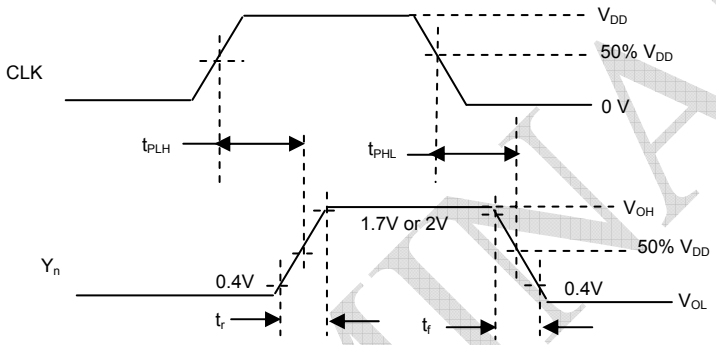


Figure 3. Voltage Waveforms Propagation Delay Times

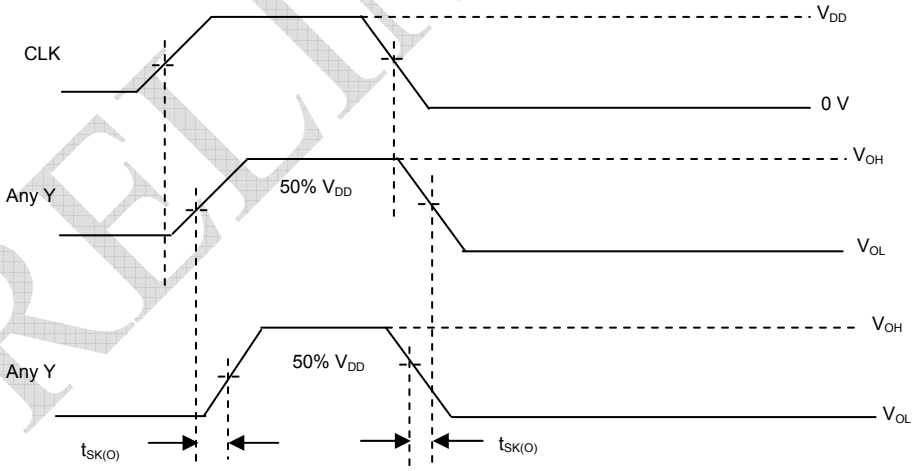


Figure 4. Output Skew

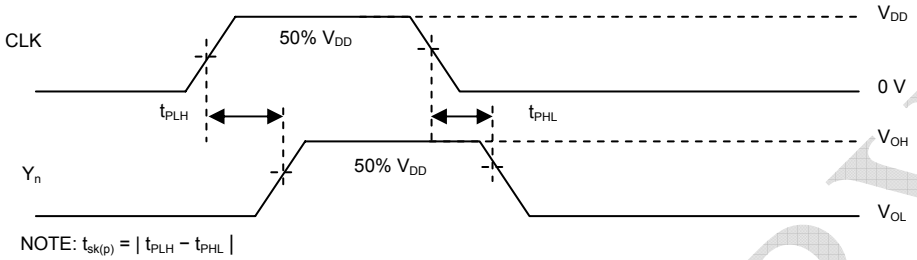


Figure 5. Pulse Skew

SUPPLY CURRENT
vs
FREQUENCY

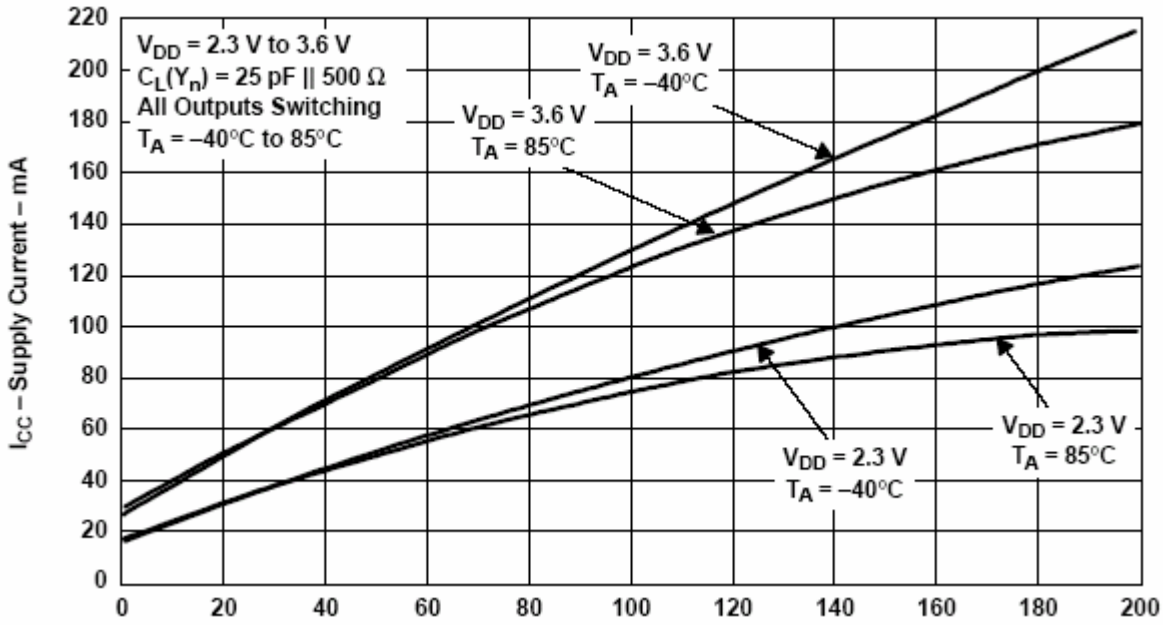
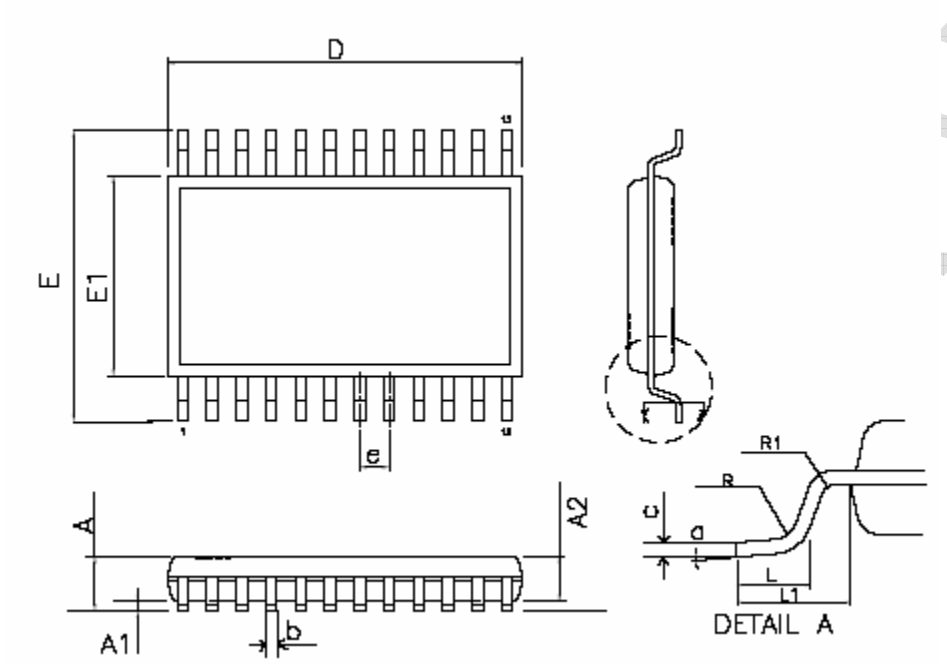


Figure 6.

Package Information

24L TSSOP (173 mil)

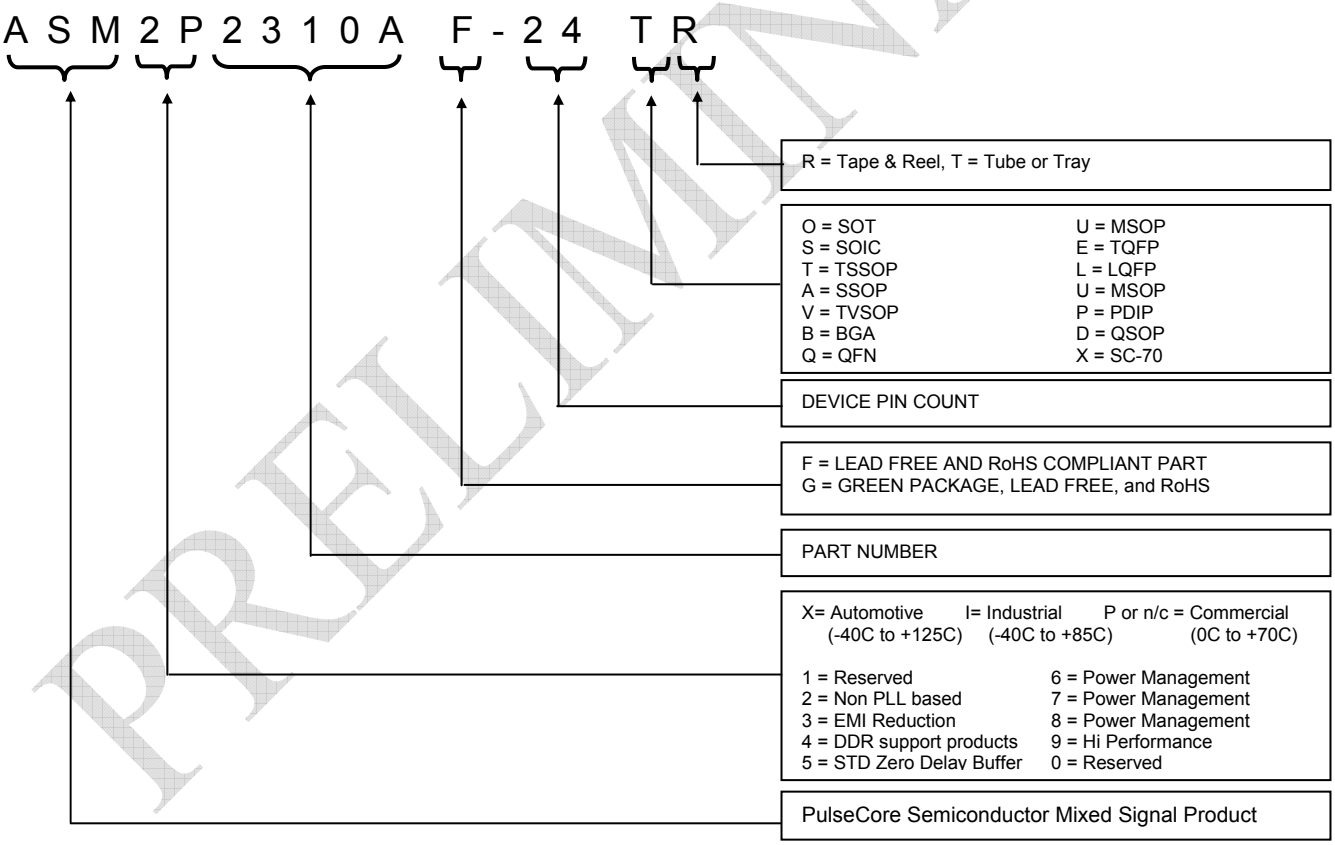


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.043	…	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.031	0.041	0.80	1.05
D	0.3031	0.311	7.70	7.90
L	0.020	0.030	0.50	0.75
E	0.252 BSC		6.40 BSC	
E1	0.169	0.177	4.30	4.50
R	0.004	….	0.09	…..
R1	0.004	….	0.09	…..
b	0.007	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
L1	0.039 REF		1.0 REF	
e	0.026 BSC		0.65 BSC	
a	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package Type	Temperature
ASM2P2310AF-24TR	2P2310AF	24-Pin TSSOP, TAPE & REEL, Pb Free	Commercial
ASM2P2310AF-24TT	2P2310AF	24-Pin TSSOP, TUBE, Pb Free	Commercial
ASM2P2310AG-24TR	2P2310AG	24-Pin TSSOP, TAPE & REEL, Green	Commercial
ASM2P2310AG-24TT	2P2310AG	24-Pin TSSOP, TUBE, Green	Commercial
ASM2I2310AF-24TR	2I2310AF	24-Pin TSSOP, TAPE & REEL, Pb Free	Industrial
ASM2I2310AF-24TT	2I2310AF	24-Pin TSSOP, TUBE, Pb Free	Industrial
ASM2I2310AG-24TR	2I2310AG	24-Pin TSSOP, TAPE & REEL, Green	Industrial
ASM2I2310AG-24TT	2I2310AG	24-Pin TSSOP, TUBE, Green	Industrial

Device Ordering Information



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003