

### Features

- Operating voltage: 2.7V~5.2V
- Built-in RC oscillator
- External 32.768kHz crystal or 32kHz frequency source input
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 64×8 patterns, 8 commons, 64 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base/WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM

- R/W address auto increment
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Cascade application

## **General Description**

HT1625 is a peripheral device specially designed for I/O type  $\mu$ C used to expand the display capability. The max. display segment of the device are 512 patterns (64×8). It also supports serial interface, buzzer sound, Watchdog Timer or time base timer functions. The HT1625 is a memory mapping and multi-function LCD controller. The software

configuration feature of the HT1625 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the HT1625. The HT162X series have many kinds of products that match various applications.

HT162X	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626	HT1627	HT16270
СОМ	4	4	8	8	8	8	16	16	16
SEG	32	32	32	32	48	64	48	64	64
Built-in Osc.		$\checkmark$	$\checkmark$		$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	
Crystal Osc.	$\checkmark$	$\checkmark$		$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$		$\checkmark$

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## Selection Table



## **Block Diagram**



### **Pin Assignment**



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## **Pad Assignment**



Chip size:  $192 \times 211 \; {\rm (mil)}^2$ 

\* The IC substrate should be connected to VDD in the PCB layout artwork.

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# **Pad Coordinates**

Pad Coo	rdinates				Unit: mil
Pad No.	X	Y	Pad No.	X	Y
1	-90.18	98.56	45	90.57	-84.53
2	-90.18	91.93	46	90.57	-77.90
3	-90.18	85.30	47	89.80	-68.13
4	-90.18	75.95	48	89.80	-61.50
5	-89.42	57.76	49	89.80	-49.51
6	-89.42	45.77	50	89.80	-42.88
7	-90.18	39.14	51	89.80	-30.90
8	-90.18	32.51	52	89.80	-24.27
9	-90.18	25.03	53	89.80	-12.28
10	-90.18	15.94	54	89.80	-5.65
11	-90.18	5.82	55	89.80	6.33
12	-90.18	-3.61	56	89.80	12.96
13	-90.18	-10.24	57	89.80	24.95
14	-90.18	-16.87	58	89.80	31.58
15	-90.18	-23.50	59	89.80	43.56
16	-90.18	-30.13	60	89.80	50.19
17	-90.18	-36.76	61	89.80	62.18
18	-90.18	-43.39	62	89.80	68.81
19	-90.18	-92.22	63	89.80	80.79
20	-83.17	-99.53	64	89.80	87.42
21	-76.54	-99.53	65	89.38	98.22
22	-69.91	-99.53	66	77.39	98.22
23	-63.28	-99.53	67	70.76	98.22
24	-56.65	-99.53	68	58.78	98.22
25	-50.02	-99.53	69	52.15	98.22
26	-43.39	-99.53	70	40.16	98.22
27	-36.76	-99.53	71	32.09	99.32
28	-30.13	-99.53	72	25.46	99.32
29	-23.50	-99.53	73	18.83	99.32
30	-16.87	-99.53	74	12.20	99.32
31	-10.24	-99.53	75	5.57	99.32
32	-3.61	-99.53	76	-1.06	99.32
33	3.02	-99.53	77	-7.69	99.32
34	9.65	-99.53	78	-14.32	99.32
35	16.28	-99.53	79	-20.95	99.32
36	22.91	-99.53	80	-27.58	99.32
37	29.54	-98.60	81	-34.21	99.32
38	41.52	-98.60	82	-40.84	99.32
39	48.15	-98.60	83	-47.47	99.32
40	60.14	-98.60	84	-54.10	99.32
41	66.77	-98.60	85	-60.73	99.32
42	78.75	-98.60	86	-67.36	99.32
	90.57	-97.79	87	-73.99	99.32
44	90.57	-91.16			

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# HT1625



# **Pad Description**

Pad No.	Pad Name	I/O	Description
1	RD	Ι	READ clock input with pull-high resistor. Data in the RAM of the HT1625 are clocked out on the rising edge of the $\overline{\text{RD}}$ signal. The clocked out data will appear on the data line. The host controller can use the next falling edge to latch the clocked out data.
2	WR	Ι	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1625 on the rising edge of the $\overline{\rm WR}$ signal.
3	DATA	I/O	Serial data input/output with pull-high resistor
4	VSS	—	Negative power supply, Ground
5	OSCI	Ι	The OSCI and OSCO pads are connected to a 32.768kHz crystal
6	OSCO	0	in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is se- lected instead, the OSCI and OSCO pads can be left open.
7	VDD		Positive power supply
8	VLCD	Ι	LCD operating voltage input pad.
9	ĪRQ	0	Time base or Watchdog Timer overflow flag, NMOS open drain output
10, 11	$BZ, \overline{BZ}$	0	2kHz or 4kHz tone frequency output pair
12~14	T1~T3	Ι	Not connected
15~22	COM0~COM7	0	LCD common outputs
23~86	SEG0~SEG63	0	LCD segment outputs
87	<del>CS</del>	Ι	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT1625 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1625 are all enabled.

## **Absolute Maximum Ratings**

Supply Voltage–0.3V to 5.5V	Storage Temperature– $50^{\circ}$ C to $125^{\circ}$ C
Input VoltageV_{SS}=0.3V to V_{DD}+0.3V	Operating Temperature–25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

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			Test Conditions		Тур.	Max.	Unit
Symbol	Parameter	VDD	Conditions	Min.			
V <sub>DD</sub>	Operating Voltage			2.7		5.2	V
т		3V	No load/LCD ON		155	310	μA
I <sub>DD1</sub>	Operating Current	5V	On-chip RC oscillator		260	420	μA
I	Operating Current		No load/LCD ON		150	310	μA
1DD2	Operating Current	5V	Crystal oscillator		250	420	μA
I <sub>DD11</sub>	Operating Current	3V	No load/LCD OFF		8	30	μΑ
1DD11	Operating Current	5V	On-chip RC oscillator		20	60	μA
Innee	Operating Current		No load/LCD OFF			20	μA
1DD22			Crystal oscillator	—		35	μA
Lowp	Standby Current	3V	No load	_	1	12	μA
<sup>1</sup> STB	Standby Current	5V	Power down mode	—	2	24	μA
V <sub>IL</sub>	Input I on Voltogo	3V		0		0.6	V
	Input Low Voltage	5V	DATA, WK, CS, KD	0		1.0	V
V	Langet II oh Valtage	3V		2.4		3	V
▼ IH	input High Voltage	5V	DATA, WK, CS, KD	4.0		5	V
Iou BZ BZ IBO		3V	$V_{OL}=0.3V$	0.9	1.8		mA
IOL1	DZ, DZ, INQ	5V	$V_{OL}=0.5V$	1.7	3		mA
I <sub>OH1</sub> BZ. BZ		3V	$V_{OH}=2.7V$	-0.9	-1.8		mA
10H1	DL, DL	5V	$V_{OH}$ =4.5V	-1.7	-3		mA
Iora			$V_{OL}=0.3V$	0.9	1.8		mA
IOL1	DAIA	5V	$V_{OL}=0.5V$	1.7	3		mA
I		3V	$V_{OH}=2.7V$	-0.9	-1.8		mA
-OH1	DATA	5V	$V_{OH}$ =4.5V	-1.7	-3		mA
Iora	LCD Common Sink Current	3V	$V_{OL}=0.3V$	80	160		μA
IOL2	LCD Common Sink Current	5V	$V_{OL}=0.5V$	180	360		μA
Lorra	LCD Common Source Current	3V	$V_{OH}=2.7V$	-40	-80		μA
1OH2		5V	$V_{OH}=4.5V$	-90	-180		μA
Inte	LCD Segment Sink Current	3V	$V_{OL}=0.3V$	50	100		μA
TOL3		5V	$V_{OL}=0.5V$	120	240		μA
т		3V	V <sub>OH</sub> =2.7V	-30	-60		μA
1 <sub>OH3</sub>	LCD Segment Source Current	5V	V <sub>OH</sub> =4.5V	-70	-140	_	μA
Bass	Dell bink Denister	3V		100	200	300	kΩ
$\kappa_{\rm PH}$	run-nign Resistor	5V	DATA, WR, US, KD	50	100	150	kΩ

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# A.C. Characteristics

Ta=25°C

General	Deven dev		Test Conditions	Ъ	-	М	<b>T</b> T •4
Symbol	Parameter	V <sub>DD</sub>	Conditions	Min.	Typ.	Max.	Unit
form	Sustan Clash	3V	On ahin PC agaillaton	22	32	40	kHz
<sup>1</sup> SYS1	System Olock		On-chip KC oscillator	24	32	40	kHz
£	former Clash		3V		32		kHz
<sup>1</sup> SYS2	System Clock	5V	External clock source	_	32		kHz
frank		3V	On shin BC sasillatan	44	64	80	Hz
<sup>1</sup> LCD1	LCD Frame Frequency	5V	On-chip RC oscillator	48	64	80	Hz
france		3V	Fotom ol ala da antesa		64		Hz
1LCD2	LCD Frame Frequency	5V	External clock source	_	64		Hz
t <sub>COM</sub>	LCD Common Period		n: Number of COM	_	n/f <sub>LCD</sub>	_	sec
£		3V		_	_	150	kHz
<sup>1</sup> CLK1	K1 Serial Data Clock (WR Pin)		Duty cycle 50%	_	_	300	kHz
£		3V		_	_	75	kHz
I <sub>CLK2</sub>	Serial Data Clock (RD Pin)	5V	Duty cycle 50%	_	_	150	kHz
t <sub>CS</sub>	Serial Interface Reset Pulse Width (Figure 3)		$\overline{\mathrm{CS}}$	_	250		ns
		3V	Write mode	3.34	_		
1	WR, RD Input Pulse Width (Figure 1)		Read mode	6.67	_	_	μs
LCLK		-37	Write mode	1.67	_		
		5V	Read mode	3.34	_		μs
+ +.	Rise/Fall Time Serial Data	3V			100		
ι <sub>r</sub> , ι <sub>f</sub>	Clock Width (Figure 1)	5V		_	120		ns
+	Setup Time for DATA to WR,	3V			190		
usu	RDClock Width(Figure 2)	5V		_	120	_	ns
t	Hold Time for DATA to $\overline{\mathrm{WR}}$ ,	3V			190		20
Un l	$\overline{\text{RD}} \operatorname{Clock} \operatorname{Width}  (\operatorname{Figure} 2)$	5V		_	120		ns
t .	Setup Time for CS to $\overline{WR}$ , $\overline{RD}$	3V			100		20
<sup>v</sup> sul	Clock Width (Figure 3)	5V			100		115
t	Hold Time for CS to $\overline{WR}$ , $\overline{RD}$	3V			100		na
t <sub>h1</sub>	Clock Width (Figure 3)	5V		-	100	—	IIS

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## **Functional Description**

#### **Display memory – RAM structure**

The static display RAM is organized into 128×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MOD-IFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

#### Time base and Watchdog Timer – WDT

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR , WDT DIS/EN/CLR and  $\overline{IRQ}$  EN/DIS are independent from each other. Once the WDT time-out occurs, the  $\overline{IRQ}$  pin will remain at logic low level until the CLR WDT or the  $\overline{IRQ}$  DIS command is issued.



**RAM** mapping

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Timer and WDT configurations

If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

#### **Buzzer tone output**

A simple tone generator is implemented in the HT1625. The tone generator can output a pair of differential driving signals on the BZ and  $\overline{\text{BZ}}$  which are used to generate a single tone.

#### **Command format**

The HT1625 can be configured by the software setting. There are two mode commands to configure the HT1625 resource and to transfer the LCD display data.

The following are the data mode ID and the command mode ID:

Operation	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the  $\overline{\text{CS}}$  pin should be set to "1" and the previous operation mode will be reset also. The  $\overline{\text{CS}}$  pin returns to "0", a new operation mode ID should be issued first.

Name	Command Code	Function
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4K	010X-XXXX-X	Turn-on tone output, tone frequency is 4kHz
TONE 2K	0110-XXXX-X	Turn-on tone output, tone frequency is 2kHz

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# **Timing Diagrams**







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#### WRITE mode (command code : 1 0 1)



### WRITE mode (successive address writing)





#### **READ-MODIFY-WRITE** mode (command code : 1 0 1)



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Command mode (command code : 1 0 0)



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# **Application Circuits**



\*Note: The connection of  $\overline{IRQ}$  and  $\overline{RD}$  pin can be selected depending on the requirement of the  $\mu C.$ The voltage applied to  $V_{LCD}$  pin must be lower than  $V_{DD}.$ Adjust VR to fit LCD display, at  $V_{DD}{=}5V, V_{LCD}{=}4V, VR{=}15k\Omega{\pm}20\%.$ Adjust R (external Pull-high resistance) to fit user's time base clock.

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# Instruction Set Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ- MODIFY- WRITE	101	A6A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	100	0000-0000-X	С	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	100	0000-0001-X	С	Turn on system oscillator	
LCD OFF	100	0000-0010-X	С	Turn off LCD display	Yes
LCD ON	100	0000-0011-X	С	Turn on LCD display	
TIMER DIS	100	0000-0100-X	С	Disable time base output	Yes
WDT DIS	100	0000-0101-X	С	Disable WDT time-out flag output	Yes
TIMER EN	100	0000-0110-X	С	Enable time base output	
WDT EN	100	0000-0111-X	С	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	С	Turn off tone outputs	Yes
CLR TIMER	100	0000-1101-X	С	Clear the contents of the time base generator	
CLR WDT	100	0000-1111-X	С	Clear the contents of the WDT stage	
RC 32K	100	0001-10XX-X	С	System clock source, on-chip RC oscillator	Yes
EXT (XTAL) 32K	100	0001-11XX-X	С	System clock source, external 32kHz clock source or crystal oscillator 32.768kHz	
TONE 4K	100	010X-XXXX-X	С	Tone frequency output: 4kHz	
TONE 2K	100	0110-XXXX-X	С	Tone frequency output: 2kHz	
<b>IRQ</b> DIS	100	100X-0XXX-X	С	Disable IRQ output	Yes
$\overline{\text{IRQ}}$ EN	100	100X-1XXX-X	С	Enable IRQ output	
F1	100	101X-0000-X	С	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	100	101X-0001-X	С	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	100	101X-0010-X	С	Time base clock output: 4Hz The WDT time-out flag after: 1s	

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Name	ID	Command Code	D/C	Function	Def.
F8	100	101X-0011-X	С	Time base clock output: 8Hz The WDT time-out flag after: 1/2 s	
F16	100	101X-0100-X	С	Time base clock output: 16Hz The WDT time-out flag after: 1/4 s	
F32	100	101X-0101-X	С	Time base clock output: 32Hz The WDT time-out flag after: 1/8 s	
F64	100	101X-0110-X	С	Time base clock output: 64Hz The WDT time-out flag after: 1/16 s	
F128	100	101X-0111-X	С	Time base clock output: 128Hz The WDT time-out flag after: 1/32 s	Yes
TEST	100	1110-0000-X	С	Test mode, user don't use.	
NORMAL	100	1110-0011-X	С	Normal mode	Yes

Note: X : Don't care

A6~A0 : RAM address

D3~D0 : RAM data

D/C : Data/Command mode

Def. : Power on reset default

All the bold forms, namely **110**, **101**, and **100**, are mode commands. Of these, **100** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1625 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1625.



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