NEC ELECTRONICS INC.

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QUARTERLY MICROPROCESSOR/MICROCOMPUTER RELIABILITY REPORT

This report contains reliability data on microprocessor and microcomputer devices fabricated at NEC Roseville and assembled at NEC Roseville or NEC Singapore.

(Signatures on file)

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Failure Rate Prediction

This report contains reliability test results of all microprocessor devices assembled in NEC Roseville that were subjected to routine Monitor Reliability Testing (MRT). It also contains failure rate predictions for these devices, calculated using the Arrhenius method shown below.

This report will be updated in September 1998.

When predicting the failure rate at a certain temperature from accelerated life test data, various values of activation energy, corresponding to failure mechanisms, should be considered. This procedure is done whenever exact causes of failures are known by performing failure analysis. In some cases, however, an average activation energy is assumed in order to accomplish a quick first-order approximation. NEC assumes an average activation energy of 0.7 eV for CMOS-4 and lesser technologies and 0.45 eV for CMOS-5 and greater technologies for such approximations. These average values have been assessed from extensive reliability test results and yield a conservative failure rate.

Since life testing at NEC is performed under high-temperature ambient conditions, the Arrhenius relationship is used to normalize failure rate predictions at a system operation temperature of 55°C. The Arrhenius model includes the effects of temperature and activation energy of the failure mechanisms. This model assumes that the degradation of a performance parameter is linear with time. The temperature dependence is taken to be an exponential function that defines the probability of occurrence.

The Arrhenius equation is:

$$A = \exp \frac{-E_A(T_{J1} - T_{J2})}{k(T_{J1})(T_{J2})} \qquad (1)$$

Where:

A ≡ Acceleration factor

E_A ≡ Activation energy

T_{J1} ≡ Junction temperature (in K) at $T_{A1} = 55°C$

T_{J2} ≡ Junction temperature (in K) at $T_{A2} = 125°C$

k ≡ Boltzmann's constant = 8.62×10^{-5} eV/K

Because temperature dependence on power dissipation of a particular device type cannot be ignored, junction temperatures (T_{J1} and T_{J2}) are used instead of ambient temperatures (T_{A1} and T_{A2}) . Also, thermal resistance of a particular device cannot be ignored. These two factors cannot be accounted for unless junction temperatures are used. We calculate junction temperatures using the following formula:

$T_J = T_A$ + (Thermal Resistance) x (Power Dissipation at T_A)

From the high-temperature operating life test results, the failure rates can be predicted at a 60% confidence level using the following equation:

$$L = \frac{X^2\, 10^5}{2T} \qquad (2)$$

Where:

L ≡ Failure rate in %/1000 hours

X^2 ≡ The tabular value of chi-squared distribution at a given confidence level and calculated degrees of freedom (2f + 2, where f = number of failures)

T ≡ T Number of equivalent device hours
= (Number of devices) x (number of test hours) x (acceleration factor)

Another method of expressing failures is as FIT (failures in time). One FIT is equal to one failure in 10^9 hours. Since L is already expressed as %/1000 hours (10^{-5} failure/hr), an easy conversion from %/1000 hours to FIT would be to multiply the value of L by 10^4.

Example

A sample of 960 pieces was subjected to 1000 hours at 125°C burn-in. One reject was observed. Given that the acceleration factor was calculated to be 34.6 using equation (1), what is the failure rate, normalized to 55°C, using a confidence level of 60%? Express the failure rate in FIT.

Solution

For n = 2f + 2 = 2(1) + 2 = 4,
$X^2 = 4.046$.

$$\text{Then } L = \frac{X^2\ 10^5}{2T} \text{ (\%/1000H)}$$

$$= \frac{X^2\ 10^5}{2 \text{ (s.s.)(test hrs)(acc. factor)}}$$

$$= \frac{(4.046)\ 10^5}{2(960)(1000)(34.6)}$$

= 0.0061 %/1000H
Therefore, FIT = $(0.0061)(10^4) = 61$

Table 1. Reliability Tests

The major reliability tests performed by NEC consist of high-temperature bias (HTB), 85°C/85% relative humidity (T/H), high-temperature storage life (HTSL), and high-humidity storage life (HHSL) tests. Additionally, various environmental and mechanical tests are performed. This table shows the conditions of the various life tests, environmental tests, and mechanical tests.

Test Item	Symbol	MIL-STD 883C Method	Condition	Remarks
High-temperature bias life	HTB	1005	T_A = 125°C, V_{CC} = 5.5 V.	**Note 1**
High-temperature storage life	HTSL	1008	T_A = 150°C.	**Note 1**
Temperature and humidity life	T/H		T_A = 85°C, RH = 85%. V_{DD} = 5.5 V, alternate pin bias.	**Notes 1, 2**
High-humidity storage life	HHSL		T_A = 85°C, RH = 85%.	**Notes 1, 2**
Pressure cooker	PCT		T_A = 125°C, RH = 100% P = 2.3 atm.	**Notes 1, 2**
Temperature cycle	T/C	1010	−65° to 150°C, 1 hour/ cycle.	**Note 1**
Lead fatigue	LI	2004	125g (DIP) 250g (QFP), three bends, 90°, without breaking.	**Note 4**
Solderability	SD	2003	T_A = 230°C, 5 sec, rosin-based flux.	**Note 5**
Soldering heat	TS	**Note 3**	260°C, 10 sec, rosin based flux. 215°C VPS 235°C, IR reflow	DIP PLCC QFP
Temperature cycle		1010	10 cycles, –65° to 150°C.	
Thermal shock		1011	15 cycles, 0° to 100°C.	**Note 1**

Notes: 1. Electrical test per data sheet is performed. Devices that exceed the data sheet limits are considered rejects.
2. Pretreatment as specified.
3. MIL-STD 750A, method 2031.
4. Broken lead is considered a reject.
5. Less than 95% coverage is considered a reject.

Table 2. Reliability Test Results

The reliability test results given in this report are representative of the following products fabricated in Roseville and assembled in Roseville or Singapore.

Fabricated in Roseville		**Assembled in Roseville**	
NMOS-4	D7720A	28-pin DIP	D7720AC
	D78H11		D77C20AC
			D77C25C
CMOS-4 CX2	D17003AH		
	D6701	40-pin DIP	D70108C
	D70108		D70116C
	D77C20A		
	D77C25	68-pin PLCC	D70208L
	D7502A		D70216L
	D7503A		
	D75004	84-pin PLC	D70320L
	D75108A		D70325L
	D75304		D70335L
	D75306		
	D75308	64-pin QFP	D7502AGF
	D75312		D7503AGF
	D75316		D75304GF
	D75328		
	D17010	80-pin QFP	D75306GF
			D75308GF
CMOS-5 CX3:	D70208		D75312GF
	D70216		D75316GF
	D70322		
	D70325	**Assembled in Singapore**	
	D70335		
	D78C10	80-pin QFP	75216AGF
	D78C11A		75308GF
	D78C14		78C10AGF
	D78213		
	D78234	64-pin LQFP	78352BG
	D78238		
	D78322		
	D937LH		

Table 3. HTB Life Test Summary and Failure Rate Predictions

This table summarizes the reliability test results of processes extensively used by most NEC microprocessor products. The failure rate predictions are based on both 125°C and 150°C high-temperature bias life test results. Failure rate predictions are shown for the current period of available data and for past periods of cumulative data.

µPD7720AC (28-pin DIP)	Jan 88–Dec 98 (cumulative)	(125°C)	448	520,000	0	17.9	9.3×10^6	
Process Type	**Process Period**	**Ambient Temp.**	**Number of Devices**	**Accum,. Device Hours**	**No. of Failures**	**Accel. Factor (Note 1)**	**Equiv. Device Hours**	**Failure Rate, 55°C and 60% Confidence Level (Note 2)**
NMOS-4 Total	Jan 88– Mar 99 (cumulative)	(125°C)	448	520,000	0	17.9	9.3×10^6	0.0098 %/1000 = 98.0 FIT
µPD77C20AC (28-pin DIP)	Jul 90– Mar 99 (cumulative)	(125°C)	432	432,000	0	32.6	1.41×10^7	
µPD77C25C (28-pin DIP)	Jul 90– Mar 99 (cumulative)	(125°C)	96	96,000	0	32.6	3.13×10^6	
µPD70108C (40-pin DIP)	Jan 90– Mar 99 (cumulative)	(125°C)	24	24,000	0	32.6	7.82×10^5	
µPD7503A (64-pin QFP)	Jan 97– Mar 99 (cumulative)	(125°C)	168	168,000	0	32.6	5.48×10^6	
µPD75304 (80-pin QFP)	Apr 92– Mar 99 (cumulative)	(125°C)	384	384,000	0	32.6	1.25×10^7	
µPD75306 (80-pin QFP)	Apr 92– Mar 99 (cumulative)	(125°C)	120	120,000	0	32.6	2.35×10^6	
µPD75308 (80-pin QFP)	Jan 90– Mar 99 (cumulative)	(125°C)	360	360,000	0	32.6	8.61×10^6	
µPD75312 (80-pin QFP)	Jul 94– Mar 99 (cumulative)	(125°C)	312	311,168	1	32.6	9.39×10^6	
µPD75316 (80-pin QFP)	Jul 94– Mar 99 (cumulative)	(125°C)	552	552,000	0	32.6	1.80×10^7	
µPD17010 (80-pin QFP)	Oct 94– Mar 99 (cumulative)	(125°C)	72	72,000	0	32.6	2.35×10^6	
µPD78C10 (80-pin QFP)	Jan 92– Mar 99 (cumulative)	(125°C)	24	24,000	0	32.6	7.82×10^5	
Singapore Assembly								
µPD75216 (80-pin QFP)	Jan 92– Mar 99 (cumulative)	(125°C)	144	144,000	0	32.6	4.69×10^6	
Singapore Assembly								
µPD75308 (80-pin QFP)	Jan 92– Mar 99 (cumulative)	(125°C)	120	120,000	0	32.6	3.91×10^6	
Singapore Assembly								
CMOS-4 Total	Jan 89– Mar 99 (cumulative)	(125°C)	2808	2,812,168	1	32.6	9.17×10^7	0.0022%/1000 = 22FIT
µPD70208 (68-pin PLCC)	Jan 92– Mar 99 (cumulative)	(125°C)	748	736,000	0	11.3	$805. \times 10^6$	
∝PD70216 (68-pin PLCC)	Apr 93– Mar 99 (cumulative)	(125°C)	936	936,000	0	11.3	1.06×10^7	
µPD70320 (84-pin PLCC)	Jul 91– Mar 99 (cumulative)	(125°C)	508	508,000	0	11.3	3.30×10^6	
µPD70325 (84-pin PLCC)	Jan 92– Mar 99 (cumulative)	(125°C)	644	644,000	1	11.3	5.65×10^6	

Table 3. HTB Life Test Summary and Failure Rate Predictions (continued)

Process Type	Process Period	Ambient Temp.	Number of Devices	Accum,. Device Hours	No. of Failures	Accel. Factor (Note 1)	Equiv. Device Hours	Failure Rate, 55°C and 60% Confidence Level (Note 2)
µPD70335 (84-pin PLCC)	Jan 94- Mar 99 (cumulative)	(125°C)	532	532,000	0	11.3	6.01×10^6	
CMOS-5 Total	Apr 88– Mar 99 (cumulative)	(125°C)	3368	3,356,000	1	11.3	3.79×10^7	0.0053%/1000H = 53FIT
µPD78352 (64-pin LQFP)	Oct 94– Mar 99 (cumulative)	(125°C)	192	192,000	0	–	–	
CMOS-8 Total	Oct 94– Mar 99 (cumulative)	(125°C)	192	192,000	0	–	–	**Note 3**

Notes: 1. The acceleration factor was calculated using the Arrhenius mathematical model.

2. FIT was derived from HTB data for all available time periods.

3. Some of the above FIT rates were not calculated. Due to small sample sizes in these cases, the FIT rates would not be meaningful. NEC expects a FIT rate of less than 100 for micro device types (target not to exceed 150).

Table 4. Other Life Test Summaries (HTSL, HHSL, T/H)

This table summarizes the reliability test results of the different process types during 150°C/175°C/200°C storage and 85°C/85% RH storage and bias tests. The data is summarized for the current period of available data and for past periods of cumulative data.

Process Type	Process Period	HTSL Failures				HHSL Failures				T/H Failures			
			Hours				Hours				Hours		
		Qty	168	500	1000	Qty	168	500	1000	Qty	168	500	1000
µPD7720AC (28-pin DIP)	Jan 88– Mar 99 (cumulative)	380	0	0	0	0	-	-	-	448	0	0	0
NMOS-4 Total	Jan 88– Mar 99 (cumulative)	380	0	0	0	0	-	-	-	448	0	0	0
µPD77C20AC (28-pin DIP)	Jul 88– Mar 99 (cumulative)	360	0	0	0	0	-	-	-	432	0	0	0
µPD77C25C (28-pin DIP)	Jul 90– Mar 99 (cumulative)	80	0	0	0	0	-	-	-	96	0	0	0
µPD70108C (40-pin DIP)	Jan 90– Mar 99 (cumulative)	20	0	0	0	0	-	-	-	24	0	0	0
µPD70116C (40-pin QFP)	Jul 88– Mar 99 (cumulative)	100	0	0	0	0	-	-	-	120	0	0	0
µPD7503A (64-pin QFP)	Jul 90– Mar 99 (cumulative)	180	0	0	0	0	-	-	-	216	0	0	0
µPD75304 (80-pin QFP)	Jan 90– Mar 99 (cumulative)	324	0	0	0	0	-	-	-	380	0	0	2
µPD75306 (80-pin QFP)	Jul 88– Mar 99 (cumulative)	80	0	0	0	0	-	-	-	96	0	0	0
µPD75308 (80-pin QFP)	Jul 90– Mar 99 (cumulative)	300	0	0	0	0	-	-	-	384	0	0	0
µPD75312 (80-pin QFP)	Jan 90– Mar 99 (cumulative)	260	0	0	0	1	-	-	-	312	0	0	1
µPD75316 (80-pin QFP)	Jul 88– Mar 99 (cumulative)	500	0	0	1	0	-	-	-	520	0	1	0
µPD17010 (80-pin QFP)	Jul 90– Mar 99 (cumulative)	40	0	0	0	0	-	-	-	72	0	0	0
µPD78C10 (80-pin QFP)	Jan 90– Mar 99 (cumulative)	0	-	-	-	0	-	-	-	204	0	0	0
µPD75216 (80-pin QFP)	Jul 88– Mar 99 (cumulative)	0	-	-	-	0	-	-	-	260	0	0	0
µPD75308 (80-pin QFP)	Jul 90– Mar 99 (cumulative)	0	-	-	-	0	-	-	-	220	0	0	0
CMOS-4 Total	Jan 90– Mar 99 (cumulative)	2244	0	0	1	0	-	-	-	3336	0	1	4
µPD70208 (68-pin PLCC)	Jul 88– Mar 99 (cumulative)	604	0	0	0	0	-	-	-	620	0	0	0
µPD70216 (68-pin PLCC)	Jul 90– Mar 99 (cumulative)	804	0	0	0	0	-	-	-	912	0	0	0
µPD70320 (84-pin PLCC)	Jan 90– Mar 99 (cumulative)	476	0	0	0	0	-	-	-	528	0	0	0
µPD70325 (84-pin PLCC)	Jul 88– Mar 99 (cumulative)	584	0	0	0	0	-	-	-	692	0	0	0
µPD70335 (84-pin PLCC)	Jul 90– Mar 99 (cumulative)	516	0	0	0	0	-	-	-	528	0	0	0
CMOS-5 Total	Jul 88– Mar 99 (cumulative)	2984	0	0	0	0	-	-	-	3280	0	0	0
µPD78352 (64-pin LQFP)	Jul 90– Mar 99 (cumulative)	0	-	-	-	0	-	-	-	192	0	0	0

CMOS-8 Total	Jan 90– Mar 99 (cumulative)	0	-	-	-	0	-	-	-	192	0	0	0

Table 5. Environmental and Mechanical Test Summaries (TS, T/C, PCT)

Process Type	Process Period	Qty	TS Failures	T/C Failures			PCT Failures		
				Qty	100 Cycles	300 Cycles	Qty	96 Hours	102 Hours
µPD7720AC (28-pin DIP)	Jan 88– Mar 99 (cumulative)	261	0	380	0	0	380	0	0
NMOS-4 Total	Jan 88- Mar 99 (cumulative)	261	0	460	0	0	380	0	0
µPD77C20AC (28-pin DIP)	Jul 88– Mar 99 (cumulative)	342	0	450	0	0	360	0	0
µPD77C25C (28-pin DIP)	Jul 90– Mar 99 (cumulative)	72	0	100	0	0	100	0	1
µPD70108C (40-pin DIP)	Jan 90– Mar 99 (cumulative)	18	0	24	0	0	20	0	0
µPD70116C (40-pin DIP)	Jul 88– Mar 99 (cumulative)	54	0	125	0	0	100	0	0
µPD7503A (64-pin QFP)	Jul 90– Mar 99 (cumulative)	90	0	225	0	0	180	0	0
µPD75304 (80-pin QFP)	Jan 90– Mar 99 (cumulative)	234	0	400	0	0	320	0	0
µPD75306 (80-pin QFP)	Jul 88– Mar 99 (cumulative)	54	2	125	0	0	100	0	0
µPD75308 (80-pin QFP)	Jul 90– Mar 99 (cumulative)	224	0	350	0	0	300	0	0
µPD75312 (80-pin QFP)	Jan 90– Mar 99 (cumulative)	162	0	300	0	1	240	0	0
µPD75316 (80-pin QFP)	Jul 88– Mar 99 (cumulative)	332	0	500	0	0	400	0	0
µPD17010 (80-pin QFP)	Jul 90– Mar 99 (cumulative)	54	0	75	0	1	60	0	0
µPD78C10 (80-pin QFP)	Jan 90– Mar 99 (cumulative)	0	-	0	-	-	180	0	0
µPD75216 (80-pin QFP)	Jul 88– Mar 99 (cumulative)	0	-	0	-	-	120	0	0
µPD75308 (80-pin QFP)	Jul 90– Mar 99 (cumulative)	0	-	0	-	-	100	0	0
CMOS-4 Total	Jan 90– Mar 99 (cumulative)	1636	2	2674	0	2	2580	0	1
µPD70208 (68-pin PLCC)	Jul 88– Mar 99 (cumulative)	324	1	800	0	1	600	0	0
µPD70216 (68-pin PLCC)	Jul 90– Mar 99 (cumulative)	468	0	975	0	0	820	0	0
µPD70320 (84-pin PLCC)	Jan 90– Mar 99 (cumulative)	180	1	525	0	3	419	0	0
µPD70325 (84-pin PLCC)	Jul 88– Mar 99 (cumulative)	144	0	675	0	1	580	0	0
µPD70335 (84-pin PLCC)	Jul 90– Mar 99 (cumulative)	306	0	600	0	1	460	0	0
CMOS-5 Total	Jul 88– Mar 99 (cumulative)	1422	2	3575	0	6	2879	0	0
µPD78352 (64-pin LQFP)	Jul 90– Mar 99 (cumulative)	0	0	60	0	0	180	0	0
CMOS-8 Total	Jan 90– Mar 99 (cumulative)	0	0	60	0	0	180	0	0

Table 6. Failure Summaries

CMOS-4

Test Item	Duration	Period	Failure
T/C	300 cyc.	Jul 94–Oct 94	1 PC DC Failure
T/C	300 cyc.	Jan 95–Mar 95	1 PC DC Failure
PCT	192 hrs.	Jan 92–Apr 92	1 PC DC Failure
HTB	168 hrs.	Oct 95–Dec 95	1 PC FUN Failure
T/H	1000 hrs.	Jan 96–Mar 96	1 PC DC Failure
T/H	1000 hrs.	Oct 95–Dec 95	1 PC FUN Failure
T/H	1000 hrs.	Jan 92–Apr 92	1 PC FUN Failure
HTSL	1000 hrs.	Apr 96–Jun 96	1 PC DC Failure
HHBT	1000 hrs.	Oct-Dec 96	1 PC FUN Failure
TS	-	Jul-Sep 97	2PC DC Failure
T/H	168 hrs.	Apr-Jun 98	1 PC DC Failure
HTSL	1000 hrs	Sep-Dec 98	1 PC DC Failure

CMOS-5

Test Item	Duration	Period	Failure
HTB	1000 hrs.	Jul 92–Sep 92	1 PC DC Failure
T/C	300 cyc.	Apr 92–Jun 92	1 PC DC Failure
T/C	300 cyc.	Jul 95–Sep 95	1 PC FUN Failure
T/S	15 cyc.	Apr 96–Jun 96	1 PC FUN Failure
HTB	168 hrs.	Jan 97–Jun 97	1 PC DC Failure
T/C	300 cyc.	Apr 97–Jun 97	1 PC DC Failure
T/C	300 cyc.	Apr 97–Jun 97	1 PC DC Failure
T/C	300 cyc.	Jul–Sep 97	1PC DC Failure

Table 7. CMOS-4 Process Family, Quarterly Reliability Data (Jan-Mar 99)

Life Tests

Device Type	Assembly Month	HTB Failures				T/H Failures				HTSL Failures/			
			Hours				Hours				Hours		
		Qty	168	500	1000	Qty	168	500	1000	Qty	168	500	1000
µPD7503A (80-pin QFP)	Jan- Mar 99	24	0	0	0	24	0	0	0	20	0	0	1

Environmental Tests

Device Type	Assembly Month	T/C Failures			PCT Failures					TS Failures
			Cycles			Hours					
		Qty	100	300	Qty	96	192	288	Qty	
µPD75312 (80-pin QFP)	Jan-Mar 99	25	0	0	20	0	0	0	18	-

Table 8. CMOS-5 Process Family, Quarterly Reliability Data (Jan-Mar 99)

Life Tests

Device Type	Assembly Month	HTB Failures				T/H Failures				HTSL Failures			
			Hours				Hours				Hours		
		Qty	168	500	1000	Qty	168	500	1000	Qty	168	500	1000
µPD70216 (68-pin PLCC)	Jan– Mar 99	24	0	0	0	24	0	0	0	20	0	0	0
µPD70335 (84-pin PLCC)	Jan– Mar 99	24	0	0	0	24	0	0	0	20	0	0	0

Environmental Tests

Device Type	Assembly Month	T/C Failures			PCT Failures				TS	
			Cycles			Hours				
		Qty	100	300	Qty	96	192	288	Qty	Failures
µPD70216 (68-pin PLCC)	Jan– Mar 99	25	0	0	20	0	0	0	18	0
µPD70335 (84-pin PLCC)	Jan– Mar 99	25	0	0	20	0	0	0	18	0