



# 2149H 1024 x 4-BIT STATIC RAM

|                                   | 2149H-1 | 2149H-2 | 2149H-3 | 2149H | 2149HL |
|-----------------------------------|---------|---------|---------|-------|--------|
| Max. Address Access Time (ns)     | 35      | 45      | 55      | 70    | 70     |
| Max. Chip Select Access Time (ns) | 20      | 20      | 25      | 30    | 30     |
| Max. Active Current (mA)          | 150     | 150     | 150     | 150   | 125    |

- Improved Performance Margins
- Fast Chip Select Access Time—20 ns Maximum
- Equal Access and Cycle Times
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range
- HMOS\* III Technology
- Common Data Input and Output
- Three-State Output
- Single +5V Supply
- Automatic Power-Down 2148H Available
- High Reliability Plastic or CERDIP Package

(See Packaging Spec. Order #231369)

The Intel 2149H is 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS III, an ultra high-performance MOS technology. It provides a maximum chip select access time as low as 20 ns instead of an automatic power-down feature. This fast chip select access time feature increases system throughput. An automatic power-down companion, the 2148H, is available for power critical applications.

The 2149H is assembled in an 18-pin package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible and in all respects: inputs, outputs and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data.

\*HMOS is a patented process of Intel Corporation.

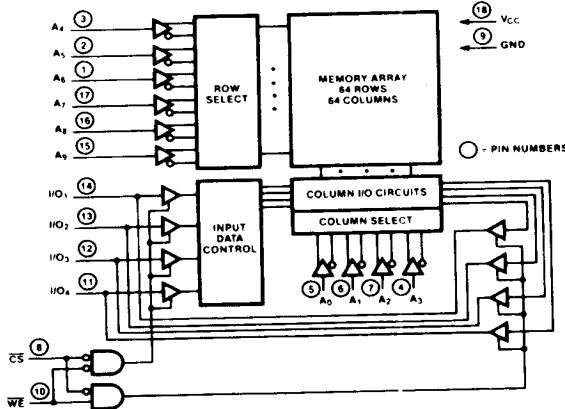


Figure 1. 2149 Block Diagram

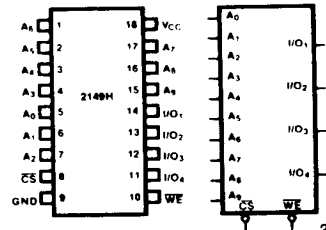


Figure 2. 2149 Pin Diagram

### Pin Names

|                                    |                   |
|------------------------------------|-------------------|
| A <sub>0</sub> –A <sub>9</sub>     | Address Inputs    |
| WE                                 | Write Enable      |
| CS                                 | Chip Select       |
| I/O <sub>0</sub> –I/O <sub>4</sub> | Data Input/Output |
| V <sub>CC</sub>                    | Power (+5V)       |
| GND                                | Ground            |

### Truth Table

| CS | WE | Mode         | I/O              |
|----|----|--------------|------------------|
| H  | X  | Not Selected | HIGH-Z           |
| L  | L  | Write        | D <sub>IN</sub>  |
| L  | H  | Read         | D <sub>OUT</sub> |

**ABSOLUTE MAXIMUM RATINGS\***

|  |                 |
|--|-----------------|
| Temperature Under Bias .....                       | -10°C to +85°C  |
| Storage Temperature CERDIP ...                     | -65°C to +150°C |
| Storage Temperature Plastic ....                   | -65°C to +125°C |
| Voltage on Any Pin with<br>Respect to Ground ..... | -3.5V to +7V    |
| D.C. Continuous Output Current .....               | 20 mA           |
| Power Dissipation .....                            | 1.2W            |

\*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. AND OPERATING CHARACTERISTICS(1)**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$  unless otherwise noted.

| Symbol         | Parameter                              | 2149H/H-1/H-2/H-3 |           |           | 2149HL |           |           | Unit          | Test Conditions   |
|----------------|--|-------------------|-----------|-----------|--------|-----------|-----------|---------------|---|
|                |  | Min               | Typ(2)    | Max       | Min    | Typ(2)    | Max       |               |   |
| $I_{LI}$       | Input Load Current<br>(All Input Pins) |                   | 0.01      | 1.0       |        | 0.01      | 1.0       | $\mu\text{A}$ | $V_{CC} = \text{max}$ ,<br>$V_{IN} = \text{GND to } 5.5\text{V}$                            |
| $I_{LO}$       | Output Leakage<br>Current              |                   | 0.1       | 10        |        | 0.1       | 10        | $\mu\text{A}$ | $\overline{CS} = V_{IH}$ , $V_{CC} = 5.5\text{V}$<br>$V_{OUT} = \text{GND to } 5.5\text{V}$ |
| $I_{CC}$       | Operating Current                      |                   | 100       | 150       |        | 70        | 125       | mA            | $V_{CC} = \text{max}$ , $\overline{CS} = V_{IL}$<br>Outputs Open                            |
| $V_{IL}$       | Input Low Voltage                      | -3.0              |           | 0.8       | -3.0   |           | 0.8       | V             |   |
| $V_{IH}$       | Input High Voltage                     | 2.0               |           | 6.0       | 2.0    |           | 6.0       | V             |   |
| $V_{OL}$       | Output Low Voltage                     |                   |           | 0.4       |        |           | 0.4       | V             | $I_{OL} = 8\text{ mA}$  |
| $V_{OH}$       | Output High Voltage                    | 2.4               |           |           | 2.4    |           |           | V             | $I_{OH} = -4.0\text{ mA}$   |
| $I_{OS}^{(4)}$ | Output Short Circuit<br>Current        |                   | $\pm 200$ | $\pm 275$ |        | $\pm 200$ | $\pm 275$ | mA            | $V_{OUT} = \text{GND to } V_{CC}$   |

**A.C. Test Conditions**

|                                       |               |
|---------------------------------------|---------------|
| Input pulse levels .....              | GND to 3.0V   |
| Input rise and fall times .....       | 5 ns          |
| *Output timing reference levels ..... | 0.8V and 2.0V |
| Output load .....                     | See Load A.   |

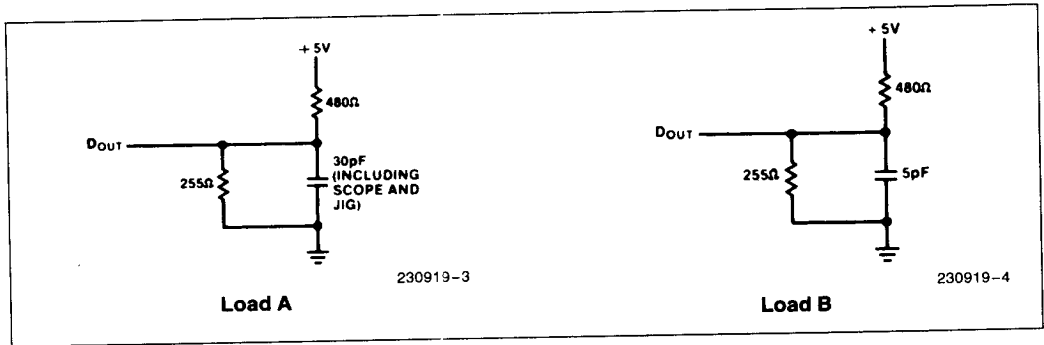
**CAPACITANCE(5)**

$T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$

| Symbol   | Parameter                      | Max | Unit | Conditions            |
|----------|--------------------------------|-----|------|-----------------------|
| $C_{IN}$ | Address/Control<br>Capacitance | 5   | pF   | $V_{IN} = 0\text{V}$  |
| $C_{IO}$ | Input/Output<br>Capacitance    | 7   | pF   | $V_{OUT} = 0\text{V}$ |

**NOTES:**

- The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:  
For CERDIP  $\theta_{JA}(@400\text{ fPM air flow}) = 40^\circ\text{C/W}$  For Plastic  $\theta_{JA}(@400\text{ fPM air flow}) = 50^\circ\text{C/W}$   
 $\theta_{JA}(\text{still air}) = 70^\circ\text{C/W}$   $\theta_{JA}(\text{still air}) = 80^\circ\text{C/W}$   
 $\theta_{JC} = 25^\circ\text{C/W}$   $\theta_{JC} = 30^\circ\text{C/W}$
  - Typical limits are at  $V_{CC} = 5\text{V}$ ,  $T_A = +25^\circ\text{C}$ , and Load A.
  - For Output Leakage tests, Data I/O pins are treated as outputs.
  - Outputs shorted for no more than 1 second. No more than one output shorted at a time.
  - This parameter is sampled and not 100% tested.
- \*improved performance margins

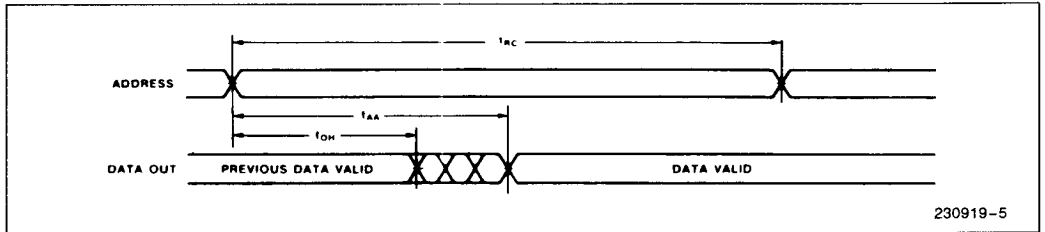
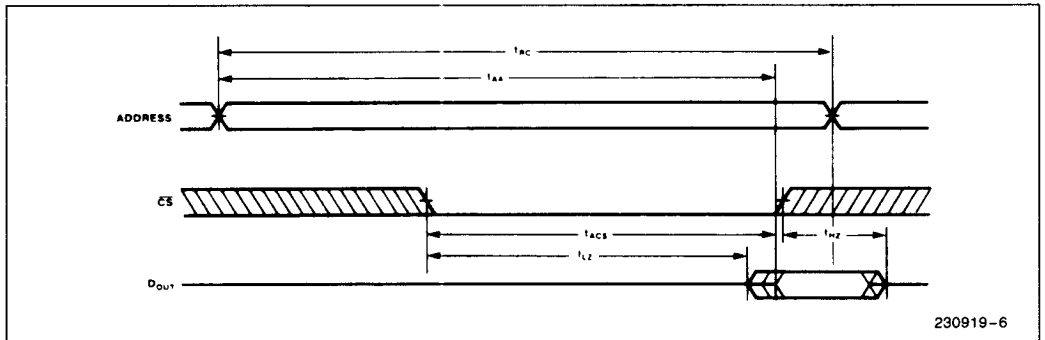


**A.C. CHARACTERISTICS**

$T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$  unless otherwise noted.

**READ CYCLE**

| Symbol    | Parameter                            | 2149H-1 |     | 2149H-2 |     | 2149H-3 |     | 2149H/HL |     | Unit | Test Conditions |
|-----------|--------------------------------------|---------|-----|---------|-----|---------|-----|----------|-----|------|-----------------|
|           |                                      | Min     | Max | Min     | Max | Min     | Max | Min      | Max |      |                 |
| $t_{RC}$  | Read Cycle Time                      | 35      |     | 45      |     | 55      |     | 70       |     | ns   |                 |
| $t_{AA}$  | Address Access Time                  |         | 35  |         | 45  |         | 55  |          | 70  | ns   |                 |
| $t_{ACS}$ | Chip Select Access Time              |         | 20  |         | 20  |         | 25  |          | 30  | ns   |                 |
| $t_{OH}$  | Output Hold from Address Change      | 5       |     | 5       |     | 5       |     | 5        |     | ns   |                 |
| $t_{LZ}$  | Chip Selection Output in Low Z       | 5       |     | 5       |     | 5       |     | 5        |     | ns   | (Notes 3, 4)    |
| $t_{HZ}$  | Chip Deselection to Output in High Z | 0       | 15  | 0       | 15  | 0       | 15  | 0        | 15  | ns   | (Notes 3, 4)    |

**WAVEFORMS**
**READ CYCLE NO. 1(1, 2)**

**READ CYCLE NO. 2(3)**

**NOTES:**

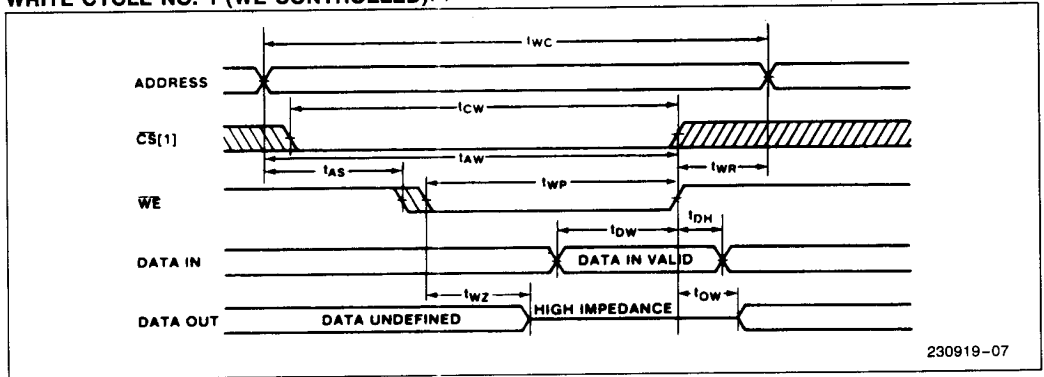
1.  $\overline{WE}$  is high for Read Cycles.
2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .
3. At any given temperature and voltage condition,  $t_{HZ}$  max. is less than  $t_{LZ}$  min. both for a given device and from device to device.
4. Transition is measured  $\pm 500$  mV from high impedance voltage with Load B.

**WRITE CYCLE**

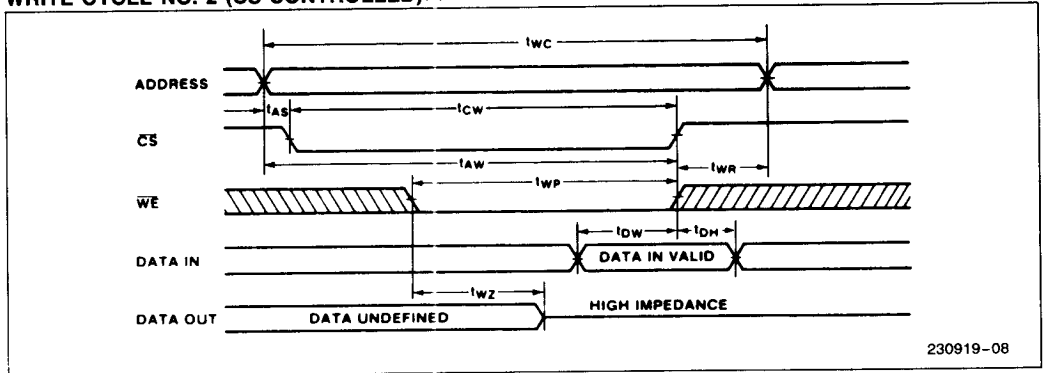
| Symbol   | Parameter                         | 2149H-1 |     | 2149H-2 |     | 2149H-3 |     | 2149H/HL |     | Unit | Test Conditions |
|----------|-----------------------------------|---------|-----|---------|-----|---------|-----|----------|-----|------|-----------------|
|          |                                   | Min     | Max | Min     | Max | Min     | Max | Min      | Max |      |                 |
| $t_{WC}$ | Write Cycle Time                  | 35      |     | 45      |     | 55      |     | 70       |     | ns   |                 |
| $t_{CW}$ | Chip-Selection to End of Write    | 30      |     | 40      |     | 50      |     | 65       |     | ns   |                 |
| $t_{AW}$ | Address Valid to End of Write     | 30      |     | 40      |     | 50      |     | 65       |     | ns   |                 |
| $t_{AS}$ | Address Setup Time                | 0       |     | 0       |     | 0       |     | 0        |     | ns   |                 |
| $t_{WP}$ | Write Pulse Width                 | 30      |     | 35      |     | 40      |     | 50       |     | ns   |                 |
| $t_{WR}$ | Write Recovery Time               | 5       |     | 5       |     | 5       |     | 5        |     | ns   |                 |
| $t_{DW}$ | Data Valid to End of Write        | 20      |     | 20      |     | 20      |     | 25       |     | ns   |                 |
| $t_{DH}$ | Data Hold Time                    | 0       |     | 0       |     | 0       |     | 0        |     | ns   |                 |
| $t_{WZ}$ | Write Enabled to Output in High Z | 0       | 15  | 0       | 15  | 0       | 20  | 0        | 25  | ns   | (Note 2)        |
| $t_{OW}$ | Output Active from End of Write   | 0       |     | 0       |     | 0       |     | 0        |     | ns   | (Note 2)        |

WAVEFORMS

WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED)<sup>(3)</sup>



WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED)<sup>(3)</sup>



NOTES:

1. If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance state.
2. Transition is measured  $\pm 500$  mV from high impedance voltage with Load B.
3.  $\overline{CS}$  or  $\overline{WE}$  must be high during address transitions.