

PRESETTABLE SYNCHRONOUS 4-BIT BINARY COUNTER; SYNCHRONOUS RESET

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION

The 74HC/HCT163 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT163 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting.

Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).

The outputs (Q<sub>0</sub> to Q<sub>3</sub>) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D<sub>0</sub> to D<sub>3</sub>) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

For the "163" the clear function is synchronous.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> CP to TC CET to TC	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	17	20	ns
			21	25	ns
			11	14	ns
f <sub>max</sub>	maximum clock frequency		51	50	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	33	35	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz                      C<sub>L</sub> = output load capacitance in pF

f<sub>o</sub> = output frequency in MHz                      V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

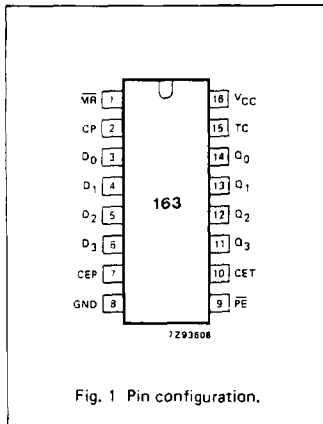


Fig. 1 Pin configuration.

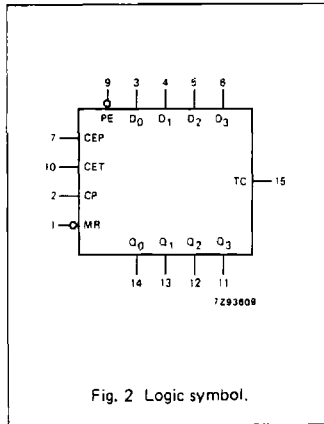


Fig. 2 Logic symbol.

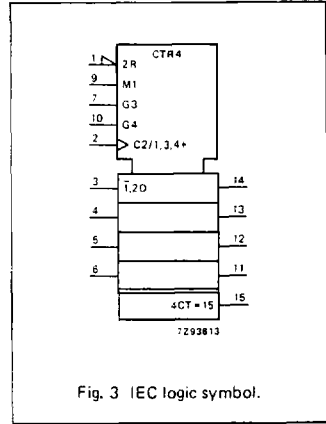


Fig. 3 IEC logic symbol.

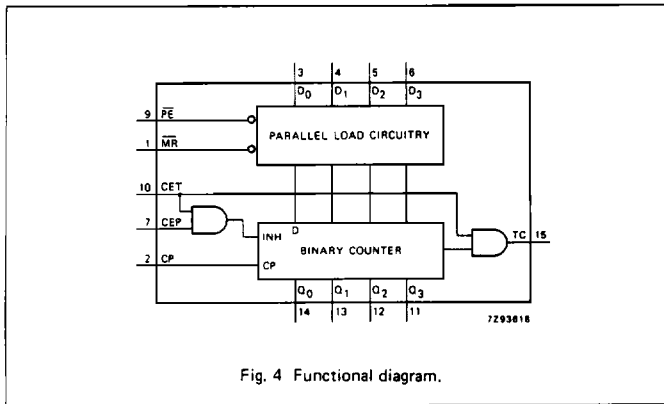


Fig. 4 Functional diagram.

**GENERAL DESCRIPTION (Cont'd)**

A LOW level at the master reset input ( $\overline{MR}$ ) sets all four outputs of the flip-flops ( $Q_0$  to  $Q_3$ ) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for  $\overline{MR}$  are met). This action occurs regardless of the levels at  $\overline{PE}$ , CET and CEP inputs.

This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of  $Q_0$ . This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{\max} = \frac{1}{t_{p(\max)}(\text{CP to TC}) + t_{SU}(\text{CEP to CP})}$$

**PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	$D_0$ to $D_3$	data inputs
7	CEP	count enable input
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14, 13, 12, 11	$Q_0$ to $Q_3$	flip-flop outputs
15	TC	terminal count output
16	V <sub>CC</sub>	positive supply voltage

**FUNCTION TABLE**

OPERATING MODE	INPUTS					OUTPUTS		
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	$D_n$	$Q_n$	TC
reset (clear)	l	↑	X	X	X	X	L	L
parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
count	h	↑	h	h	h	X	count	*
hold (do nothing)	h	X	l	X	h	X	$q_n$	*
	h	X	X	l	h	X	$q_n$	L

**Note to function table**

\* The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition

X = don't care

↑ = LOW-to-HIGH CP transition

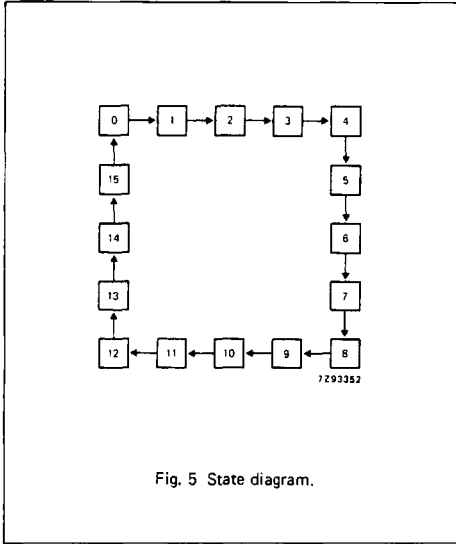


Fig. 5 State diagram.

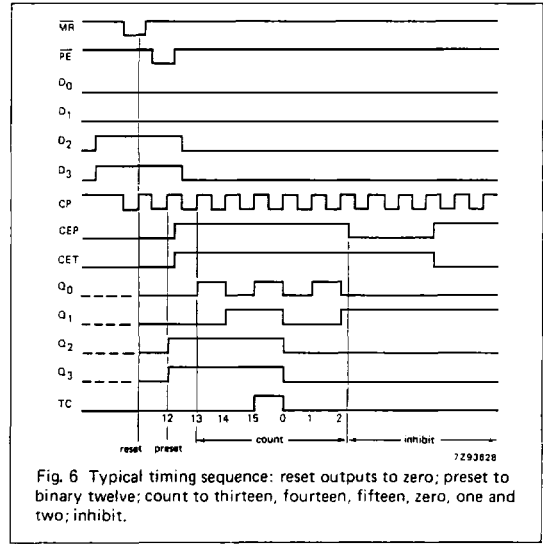


Fig. 6 Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

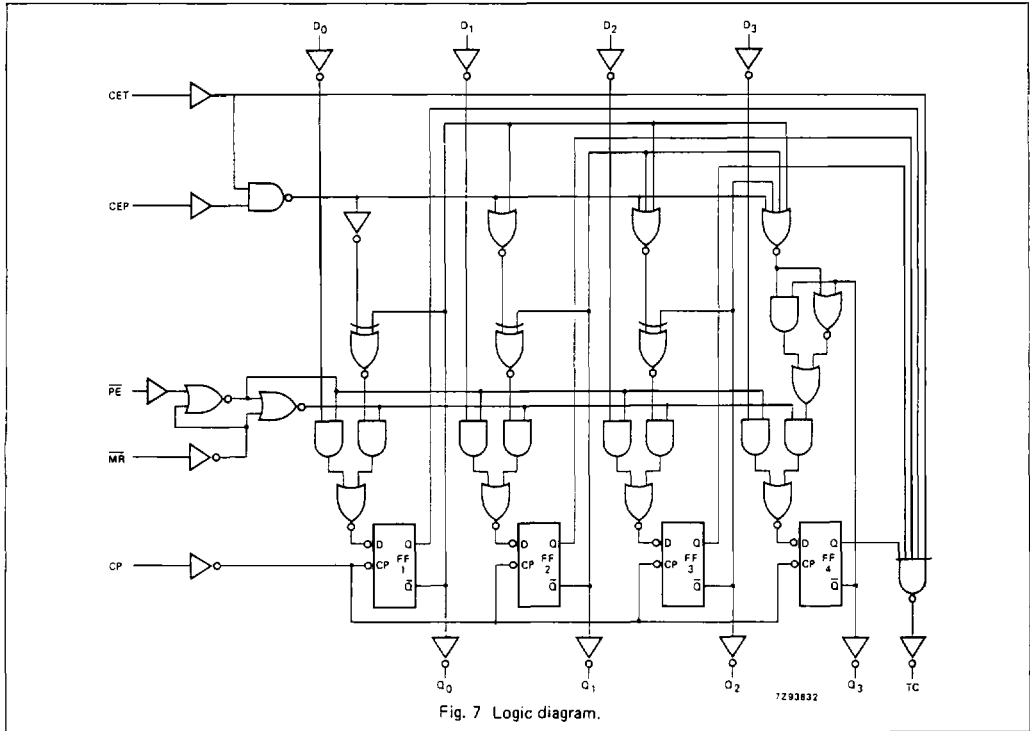


Fig. 7 Logic diagram.

**74HC/HCT163**  
MSI

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard  
I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		55 20 16	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		69 25 20	215 43 37		270 54 46		320 85 55	ns	2.0 4.5 6.0	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		36 13 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 8 and 9
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t <sub>su</sub>	set-up time MR, D <sub>n</sub> to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 10 and 11
t <sub>su</sub>	set-up time PE to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 10
t <sub>su</sub>	set-up time CEP, CET to CP	175 35 30	58 21 17		220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 12
t <sub>h</sub>	hold time D <sub>n</sub> , PE, CEP, CET, MR to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Figs 10, 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	5 27 32	15 46 55		4 22 26		4 18 21		MHz	2.0 4.5 6.0	Fig. 8

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT	INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95	D <sub>n</sub>	0.25
CP	1.10	CET	0.75
CEP	0.25	PE	0.30

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> V	WAVEFORMS	
		+25		-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		23	39		49		59	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to TC		29	49		61		74	ns	4.5	Fig. 8
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CET to TC		17	32		44		48	ns	4.5	Fig. 9
t <sub>THL</sub> / t <sub>T LH</sub>	output transition time		7	15		19		22	ns	4.5	Figs 8 and 9
t <sub>w</sub>	clock pulse width HIGH or LOW	20	6		25			30	ns	4.5	Fig. 8
t <sub>su</sub>	set-up time $\overline{MR}$ , D <sub>n</sub> to CP	20	9		25			30	ns	4.5	Figs 10 and 11
t <sub>su</sub>	set-up time PE to CP	20	11		25			30	ns	4.5	Fig. 10
t <sub>su</sub>	set-up time CEP, CET to CP	40	24		50			60	ns	4.5	Fig. 12
t <sub>h</sub>	hold time D <sub>n</sub> , PE, CEP, CET, $\overline{MR}$ to CP	0	-5		0			0	ns	4.5	Figs 10, 11 and 12
f <sub>max</sub>	maximum clock pulse frequency	26	45		21			17	MHz	4.5	Fig. 8

AC WAVEFORMS

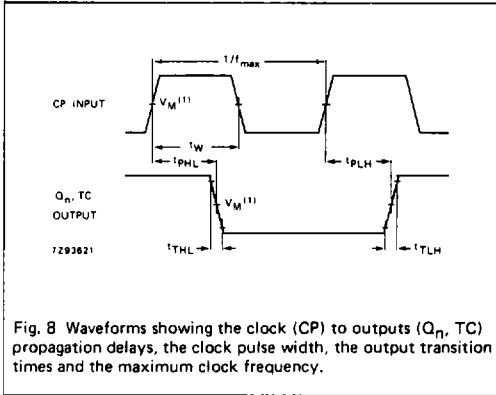


Fig. 8 Waveforms showing the clock (CP) to outputs ( $Q_n$ , TC) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

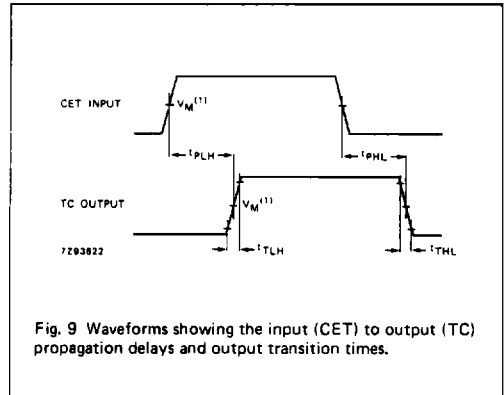


Fig. 9 Waveforms showing the input (CET) to output (TC) propagation delays and output transition times.

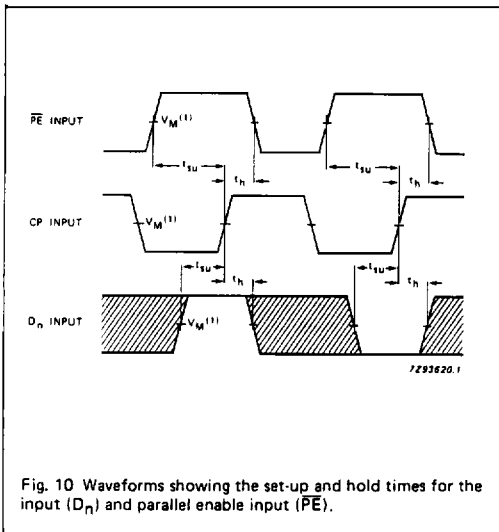


Fig. 10 Waveforms showing the set-up and hold times for the input ( $D_n$ ) and parallel enable input ( $\overline{PE}$ ).

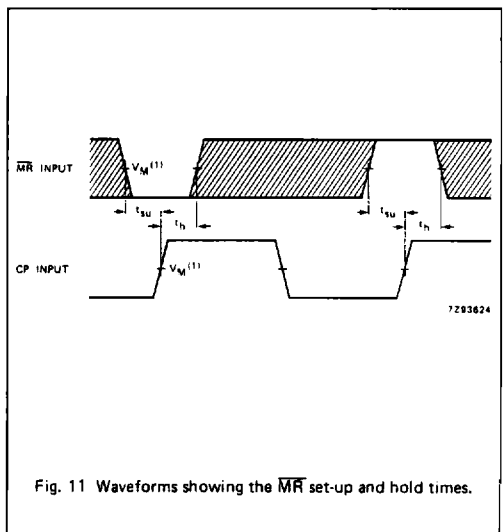


Fig. 11 Waveforms showing the  $\overline{MR}$  set-up and hold times.

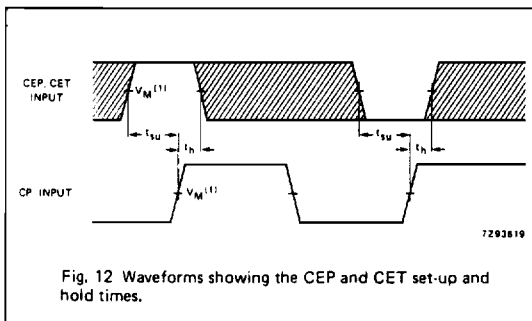


Fig. 12 Waveforms showing the CEP and CET set-up and hold times.

Note to Figs 10, 11 and 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_I = GND$  to  $V_{CC}$ .  
HCT:  $V_M = 1.3V$ ;  $V_I = GND$  to  $3V$ .

**APPLICATION INFORMATION**

The HC/HCT163 facilitate designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous reset.

