HIGH-VOLTAGE MIXED-SIGNAL IC

UC1606

65COM x 132SEG Matrix LCD Controller-Driver

Product Specifications
Version 1.32

September 24, 2003

ULTRACHIP

The Coolest LCD Driver. Ever.!

HOST INTERFACE

As summarized in the table below, UC1606 supports two 8-bit parallel bus protocols and two serial bus protocols. Designers can choose either the 8-bit parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules and minimize connector pins.

Bus Type		8080	6800	SPI (S8)	SPI(S9)
Control & Data Pins	PS[1:0]	10b	11b	00b	01b
	CS[1:0]	Chip Select			
	CD	Control/Data			–
	WR0	$\overline{WR}$	R/$\overline{W}$	0	0
	WR1	$\overline{RD}$	EN	0	0
	Access	Read/Write		Write Only	
	D[7:0]	8-bit bus (Tri-state)		D0=SCK, D2=SDA	

* Connect unused control pins to V_{DD} or V_{SS}.

Table 4: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1606 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that, every time memory address is modified, either in parallel mode or serial mode, by either *Set CA* or *Set PA* command, a dummy read cycle need to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

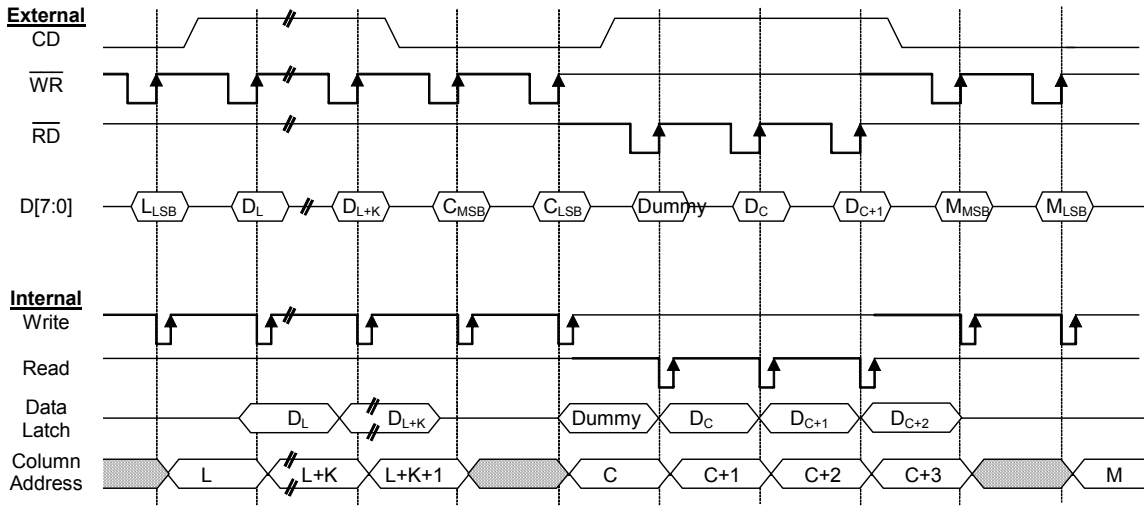


Figure 4: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1606 supports two serial modes, 4-wire mode (PS="LL"), and 3-wire mode (PS="LH"). The mode of interface is determined during power-up process by the value of PS[1:0].

4-WIRE SERIAL INTERFACE (S8)

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

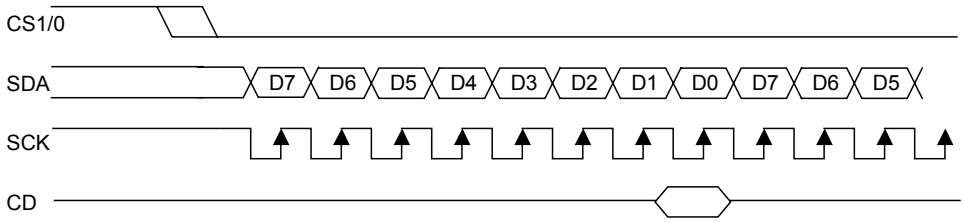


Figure 5.a: 4-wire Serial Interface (S8)

3-WIER SERIAL INTERFACE (S9)

Only write operations are supported in 3-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}.

The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

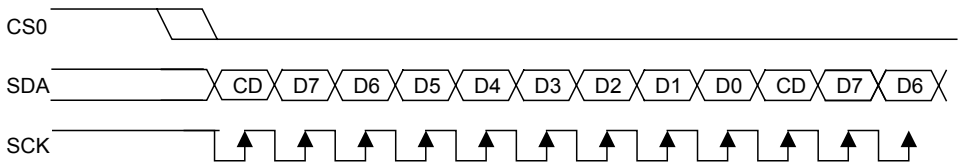


Figure 5.b: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

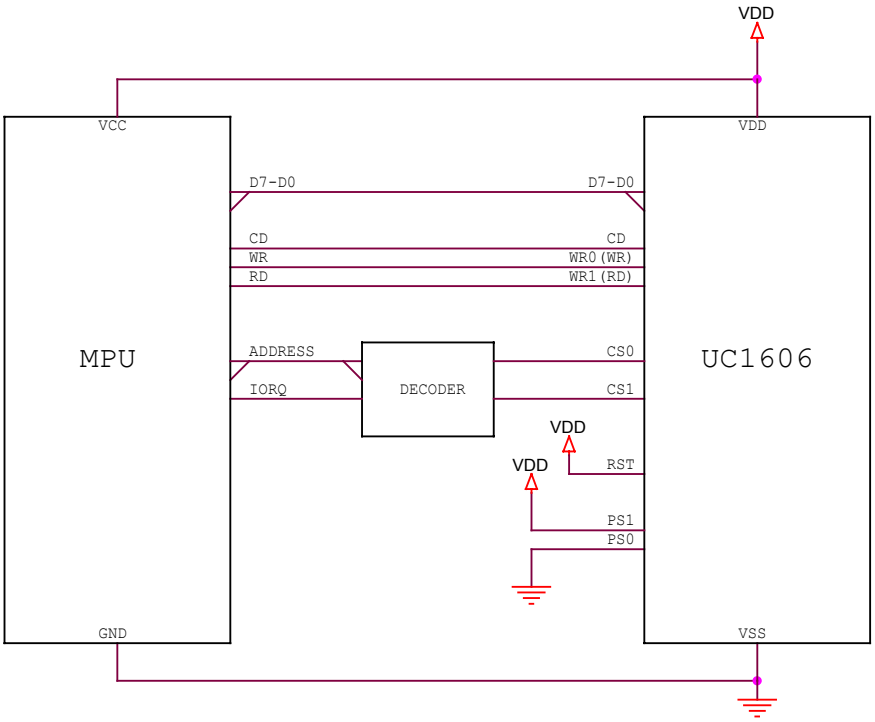


FIGURE 6: 8080/8bit parallel mode reference circuit

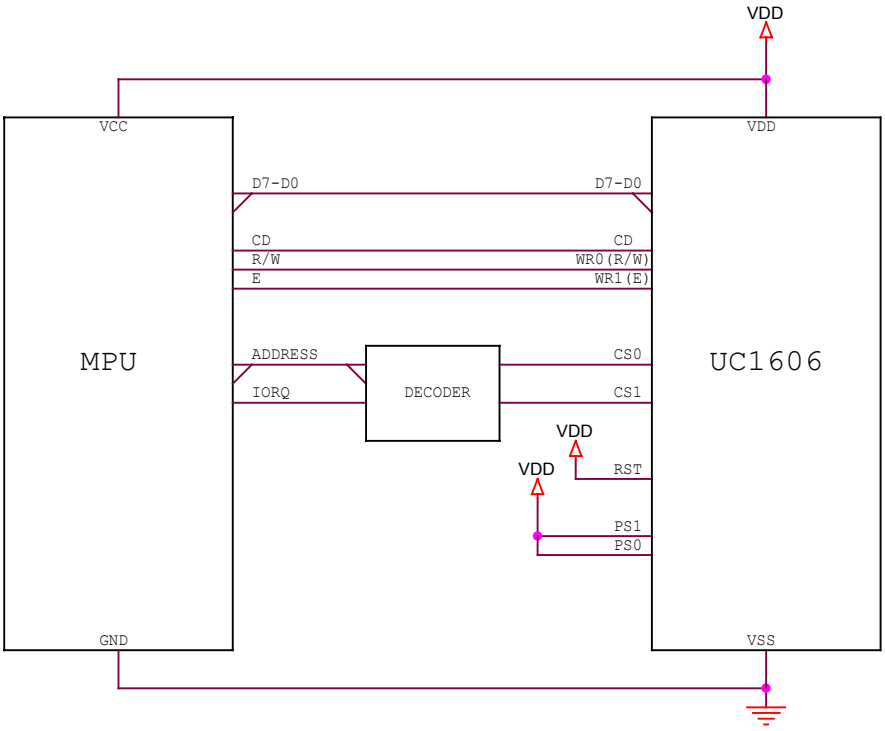


FIGURE 7: 6800/8bit parallel mode reference circuit

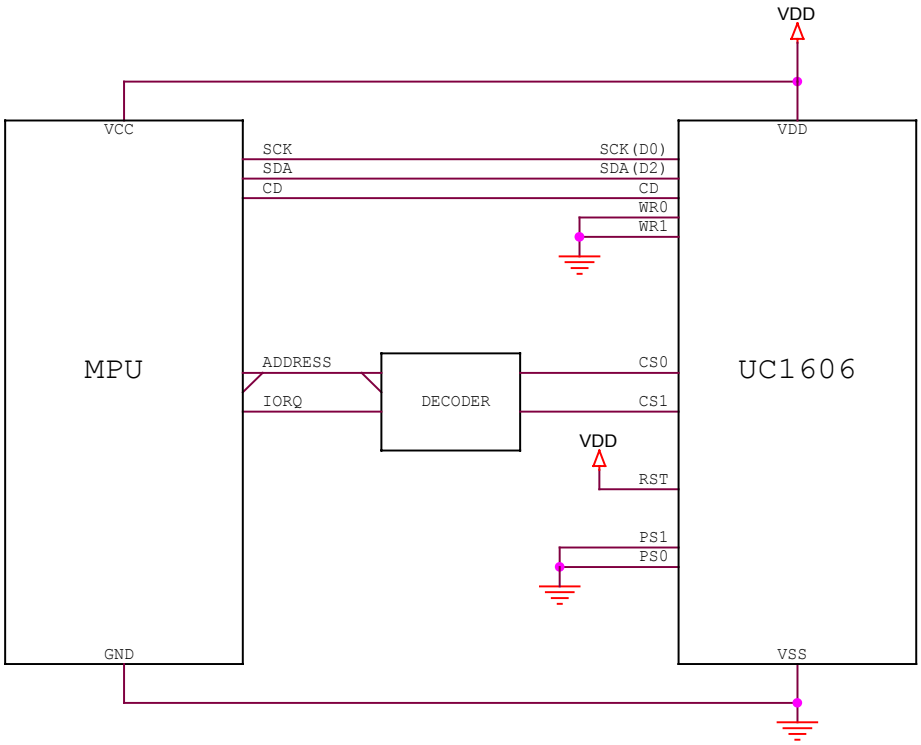


FIGURE 8: Serial-8 serial mode reference circuit

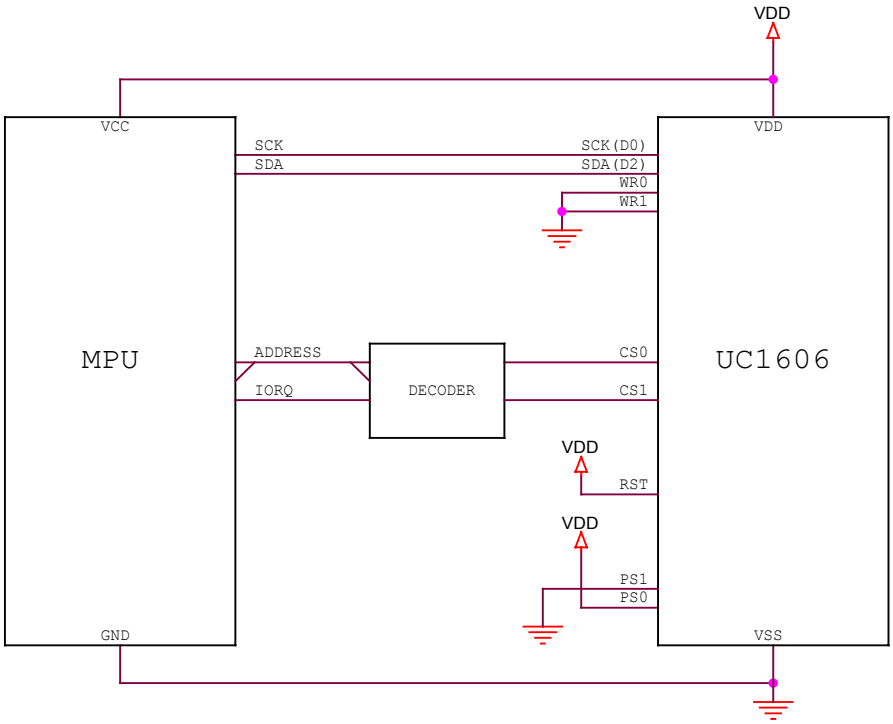


FIGURE 9: Serial-9 serial mode reference circuit

Note: RST pin is optional. When RST pin is not used, connect the pin to VDD.

DISPLAY DATA RAM

DATA ORGANIZATION

The display data is 1-bit per pixel and stored in a dual port static RAM (RAM, for Display Data RAM). The RAM size is 65 x 132 for UC1606. This array of data bits is further organized into pages of 8 bit slices to facilitate parallel bus interface.

When Mirror X (MX, LC[2]) is OFF, the 1st column of LCD pixels will correspond to the bits of the first byte of each page, the 2nd column of LCD pixels correspond to the bits of the second byte of each page, etc.

MSB FIRST OR LSB FIRST

There are two options to map D[7:0] to RAM, MSB first (MSF=1), or LSB first (MSF=0), as illustrated in next page.

DISPLAY DATA RAM ACCESS

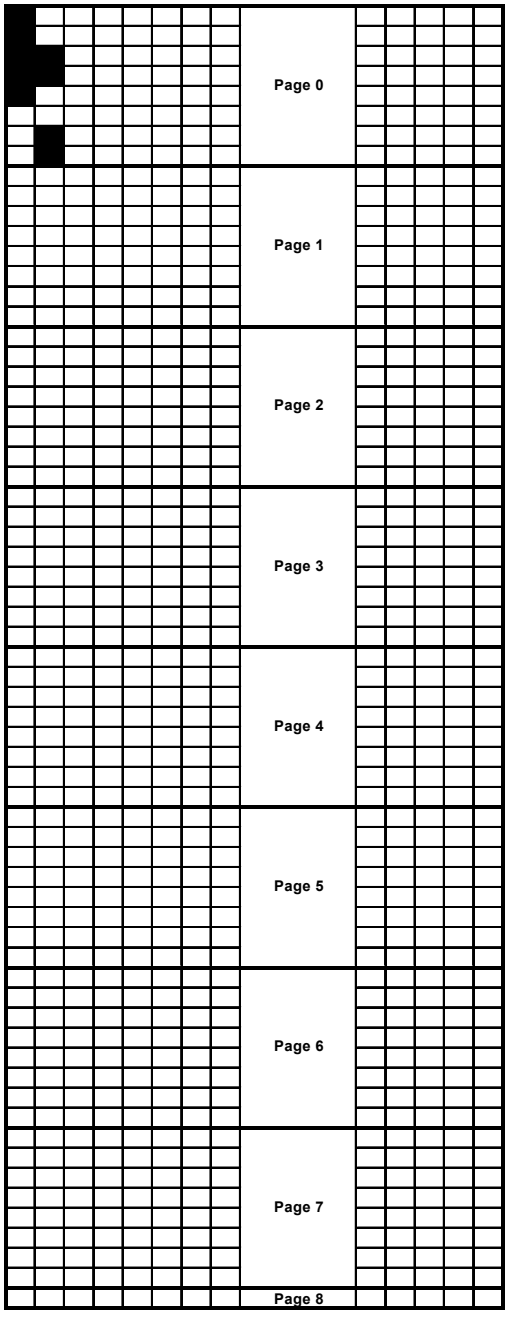
The memory used in UC1606 Display Data RAM (RAM) is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of page , and system programmers need to set the values of PA and CA explicitly.

PA[3:0]	MSF 0	MSF 1	Line AddeCss
0000	D0	D7	00H
	D1	D6	01H
	D2	D5	02H
	D3	D4	03H
	D4	D3	04H
	D5	D2	05H
	D6	D1	06H
	D7	D0	07H
0001	D0	D7	08H
	D1	D6	09H
	D2	D5	0AH
	D3	D4	0BH
	D4	D3	0CH
	D5	D2	0DH
	D6	D1	0EH
	D7	D0	0FH
0010	D0	D7	10H
	D1	D6	11H
	D2	D5	12H
	D3	D4	13H
	D4	D3	14H
	D5	D2	15H
	D6	D1	16H
	D7	D0	17H
0011	D0	D7	18H
	D1	D6	19H
	D2	D5	1AH
	D3	D4	1BH
	D4	D3	1CH
	D5	D2	1DH
	D6	D1	1EH
	D7	D0	1FH
0100	D0	D7	20H
	D1	D6	21H
	D2	D5	22H
	D3	D4	23H
	D4	D3	24H
	D5	D2	25H
	D6	D1	26H
	D7	D0	27H
0101	D0	D7	28H
	D1	D6	29H
	D2	D5	2AH
	D3	D4	2BH
	D4	D3	2CH
	D5	D2	2DH
	D6	D1	2EH
	D7	D0	2FH
0110	D0	D7	30H
	D1	D6	31H
	D2	D5	32H
	D3	D4	33H
	D4	D3	34H
	D5	D2	35H
	D6	D1	36H
	D7	D0	37H
0111	D0	D7	38H
	D1	D6	39H
	D2	D5	3AH
	D3	D4	3BH
	D4	D3	3CH
	D5	D2	3DH
	D6	D1	3EH
	D7	D0	3FH
1000	D0	D7	40H



MX															
0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG125	SEG126	SEG127	SEG128	SEG129	SEG130	SEG131	SEG132
1	SEG132	SEG131	SEG130	SEG129	SEG128	SEG127	SEG126	SEG125		SEG5	SEG4	SEG3	SEG2	SEG1			

MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=0	MY=1 SL=25	MY=1 SL=25
C1	C49	C64	C48	C25	C9
C2	C50	C63	C47	C24	C8
C3	C51	C62	C46	C23	C7
C4	C52	C61	C45	C22	C6
C5	C53	C60	C44	C21	C5
C6	C54	C59	C43	C20	C4
C7	C55	C58	C42	C19	C3
C8	C56	C57	C41	C18	C2
C9	C57	C56	C40	C17	C1
C10	C58	C55	C39	C16	---
C11	C59	C54	C38	C15	---
C12	C60	C53	C37	C14	---
C13	C61	C52	C36	C13	---
C14	C62	C51	C35	C12	---
C15	C63	C50	C34	C11	---
C16	C64	C49	C33	C10	---
C17	C1	C48	C32	C9	---
C18	C2	C47	C31	C8	---
C19	C3	C46	C30	C7	---
C20	C4	C45	C29	C6	---
C21	C5	C44	C28	C5	---
C22	C6	C43	C27	C4	---
C23	C7	C42	C26	C3	---
C24	C8	C41	C25	C2	---
C25	C9	C40	C24	C1	---
C26	C10	C39	C23	C64	C48*
C27	C11	C38	C22	C63	C47
C28	C12	C37	C21	C62	C46
C29	C13	C36	C20	C61	C45
C30	C14	C35	C19	C60	C44
C31	C15	C34	C18	C59	C43
C32	C16	C33	C17	C58	C42
C33	C17	C32	C16	C57	C41
C34	C18	C31	C15	C56	C40
C35	C19	C30	C14	C55	C39
C36	C20	C29	C13	C54	C38
C37	C21	C28	C12	C53	C37
C38	C22	C27	C11	C52	C36
C39	C23	C26	C10	C51	C35
C40	C24	C25	C9	C50	C34
C41	C25	C24	C8	C49	C33
C42	C26	C23	C7	C48	C32
C43	C27	C22	C6	C47	C31
C44	C28	C21	C5	C46	C30
C45	C29	C20	C4	C45	C29
C46	C30	C19	C3	C44	C28
C47	C31	C18	C2	C43	C27
C48	C32	C17	C1	C42	C26
C49	C33	C16	---	C41	C25
C50	C34	C15	---	C40	C24
C51	C35	C14	---	C39	C23
C52	C36	C13	---	C38	C22
C53	C37	C12	---	C37	C21
C54	C38	C11	---	C36	C20
C55	C39	C10	---	C35	C19
C56	C40	C9	---	C34	C18
C57	C41	C8	---	C33	C17
C58	C42	C7	---	C32	C16
C59	C43	C6	---	C31	C15
C60	C44	C5	---	C30	C14
C61	C45	C4	---	C29	C13
C62	C46	C3	---	C28	C12
C63	C47	C2	---	C27	C11
C64	C48	C1	---	C26	C10
CIC	CIC	CIC	CIC	CIC	CIC
		65	49	65	49
		MUX			

Example for memory mapping: let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1: 00011111b
⇒ Page 0 SEG 2: 11001100b

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (64–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW SCANNING

For each field, the scanning starts at COM1 through COMx, where x depends on the setting of MR.

COM electrode scanning (row scanning) orders are not affected by Start Line (SL) or Mirror Y (MY, LC[3]). When MY is 0, the effect of SL having a value *K* is to change the mapping of COM1 to the *K*-th bit slice of data stored in display RAM. Visually, SL having a non-zero value is equivalent to scrolling LCD display up by SL rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed Row scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, *64*)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

Effects such as page scrolling, page swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MUX-1*, *64*)
where MUX = 25, 33, 49, or 65.

Otherwise
Line = Mod(*Line-1* , *64*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1606 has two different types of Reset:
Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~20mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1606 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Read Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1606 has three operating modes (OM):
Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	OFF	OFF

Table 5: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0}, C_{B1}, and C_L. To drain these capacitors, use Reset command to activate the on-chip draining circuit.

Action	Mode	OM
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11
Reset command or RST_ pin pulled "L" Power ON Reset	Reset	00

Table 6: OM changes

Even though UC1606 consumes very little energy in Sleep mode (typically 5uA or less), since all capacitors are still charged, the leakage through COM drivers may damage the LCD over the long term. It is therefore recommended to use Sleep mode only for brief Display OFF operations, such as full-frame screen updates, and to use RESET for extended screen OFF operations.

EXITING SLEEP MODE

UC1606 contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset Mode, COM and SEG drivers will not be activated until UC1606 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1606 power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 20~30 ms before the CPU starting to issue commands to UC1606. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

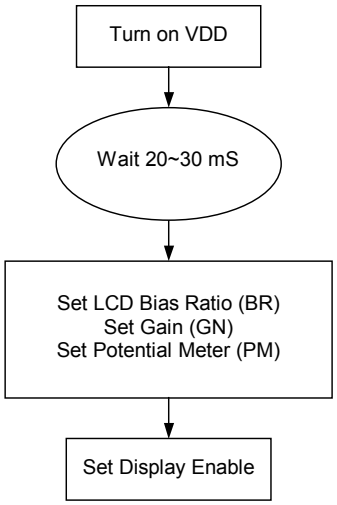


Figure 10: Reference Power-up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+}, C_{BX-}, and C_L from damaging the LCD when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for V_{LCD} and *1.5 x RC* for V_{B+}. For example, if C_L is 10nF, then the draining time required for V_{LCD} is 3~5mS.

When internal V_{LCD} is not used, UC1606 will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

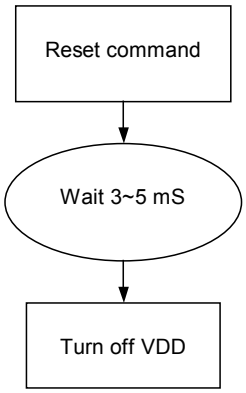


Figure 11: Reference Power-Down Sequence

SAMPLE POWER COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

Type Required: These items are required
Customer: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~30ms after V_{DD} is ON
C	0	0	1	1	0	0	#	#	0	#	(16) Set LCD Mapping	Set up LCD specific parameters such as format, MX, MY, MSF, etc.
C	0	0	1	1	1	0	1	0	#	#	(19) Set Bias Ratio	
R	0	0	0	0	1	0	0	#	#	#	(5) Set Gain	
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(10) Set PM	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	(15) Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(17) System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait 3~5ms before V_{DD} OFF

BRIEF DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	(15) Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	(15) Set Display Enable	

* This is only recommended for very brief display OFF (under 10mS).
If image becomes unstable use the *Extended Display OFF* approach shown below.

EXTENDED DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(17) System Reset.	C_{B1}, C_{B1}, C_{LCD} discharged.
–	–	–	–	–	–	–	–	–	–	–		Extended display OFF *Z z z z . . .*
–	–	–	–	–	–	–	–	–	–	–		System waking up
C	0	0	1	1	0	0	#	#	0	#	(16) Set LCD Mapping	Set up LCD specific parameters such as format, MX, MY, MSF, etc.
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the RESET state.)
C	0	0	1	1	1	0	1	0	#	#	(19) Set Bias Ratio	
R	0	0	0	0	1	0	0	#	#	#	(5) Set Gain	
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(10) Set PM	
R	0	0	1	0	1	0	1	1	1	1	(17) Set Display Enable	

* The sequence is basically the same as the power up sequence, except *Power-ON RESET* is replaced by *System RESET* command, and an extended idle time in between.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+5.5	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+5.5	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+5.5	V
V_{LCD}	LCD Generated voltage	-0.3	+15.5	V
V_{IN}	Any Input Voltage	-0.3	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.4	3.0	5.0	V
$V_{DD2/3}$	Supply for bias & pump		2.4	3.0	5.0	V
V_{LCD}	Charge pump output	$V_{DD2/3}$ >= 2.4V, 25^{O}C		9.5	13.5	V
V_D	LCD data voltage	$V_{DD2/3}$ >= 2.4V, 25^{O}C			1.2	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 9V		3	4	kΩ
$R_{0(COM)}$	COM output impedance	V_{LCD} = 9V		3.5	4.5	kΩ
f_{CLK}	Internal clock frequency		183	190	196	kHz

POWER CONSUMPTION

VDD = 2.8, Bias Ratio = 9.33, Gain = 1.43, PM = 32, PL = Regular LCD loading, MR = 65, Bus mode = 6800, C_L = 20nF, CB = 1uF. All outputs are open-circuit.

Display Pattern	Conditions	Typ.(μA)	Max.(μA)
All-OFF	Bus = idle	249	600
2-pixel checker	Bus = idle	451	600

AC CHARACTERISTICS

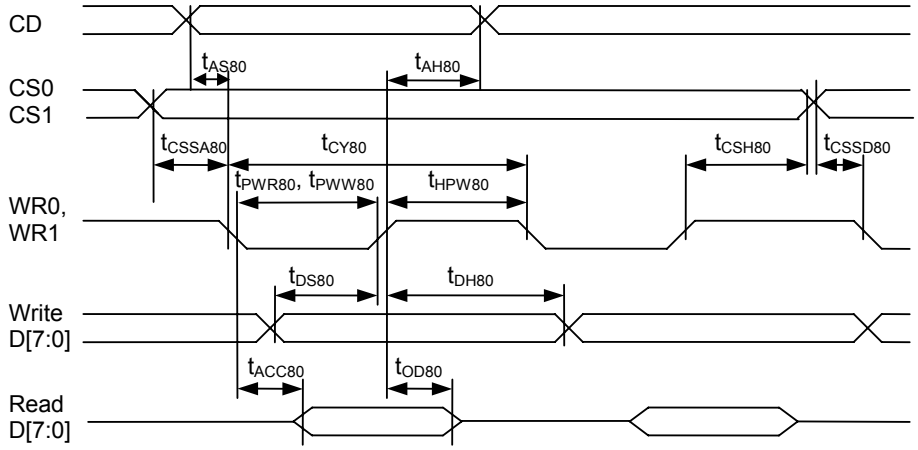


Figure 12: Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		25 50	–	ns
t_{CY80}		System cycle time		300	–	ns
t_{PWR80}	WR1	Pulse width (read)		85	–	ns
t_{PWW80}	WR0	Pulse width (write)		85	–	ns
t_{HPW80}	WR0, WR1	High pulse width		85	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		40 15	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	140 100	ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		15 15 30		ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		20 45	–	ns
t_{CY80}		System cycle time		166	–	ns
t_{PWR80}	WR1	Pulse width (read)		65	–	ns
t_{PWW80}	WR0	Pulse width (write)		65	–	ns
t_{HPW80}	WR0, WR1	High pulse width		65	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	65 45	ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

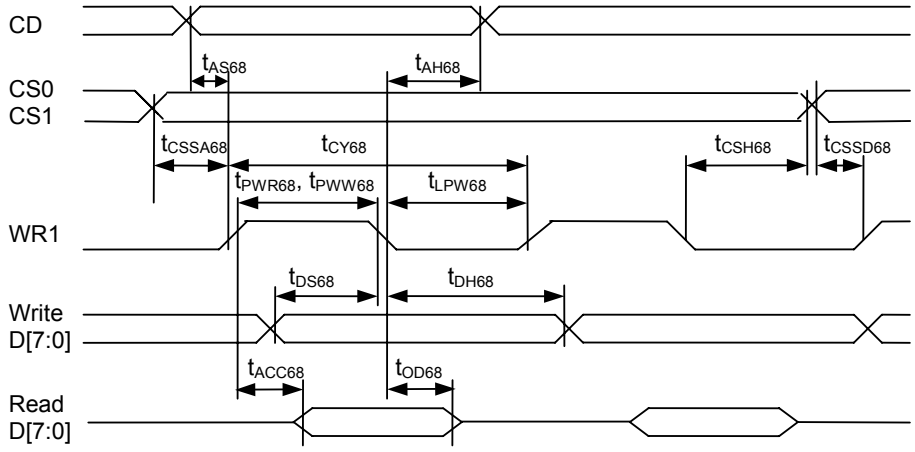


Figure 13: Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		25 50	–	ns
t_{CY68}		System cycle time		300	–	ns
t_{PWR68}	WR1	Pulse width (read)		85	–	ns
t_{PWW68}		Pulse width (write)		85	–	ns
t_{LPW68}		Low pulse width		85	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		40 15	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	140 100	ns
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		15 15 30		ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		20 45	–	ns
t_{CY68}		System cycle time		166	–	ns
t_{PWR68}	WR1	Pulse width (read)		65	–	ns
t_{PWW68}		Pulse width (write)		65	–	ns
t_{LPW68}		Low pulse width		65	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	70 50	ns
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

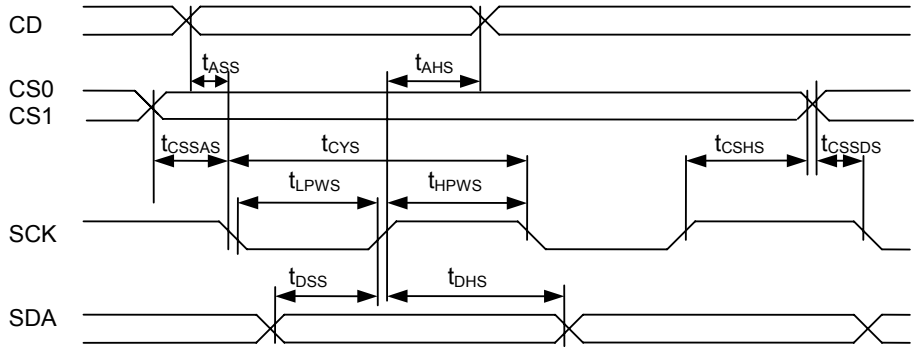


Figure 14: Serial Bus Timing Characteristics

(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS}	CD	Address setup time		15	–	ns
t_{AHS}		Address hold time		40	–	ns
t_{CYS}	SCK	System cycle time		250	–	ns
t_{LPWS}		Low pulse width		100	–	ns
t_{HPWS}		High pulse width		100	–	ns
t_{DSS} t_{DHS}	SDA	Data setup time Data hold time		90 90	–	ns
t_{CSSAS} t_{CSSDS} t_{CSHS}	CS1/CS0	Chip select setup time		10 10 150		ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS}	CD	Address setup time		10	–	ns
t_{AHS}		Address hold time		20	–	ns
t_{CYS}	SCK	System cycle time		200	–	ns
t_{LPWS}		Low pulse width		75	–	ns
t_{HPWS}		High pulse width		75	–	ns
t_{DSS} t_{DHS}	SDA	Data setup time Data hold time		50 50	–	ns
t_{CSSAS} t_{CSSDS} t_{CSHS}	CS1/CS0	Chip select setup time		10 10 100		ns

Figure 15: Reset Characteristics

(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		240	–	ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		200	–	ns

PHYSICAL DIMENSIONS

DIE SIZE:
9.862 mm x 1.647 mm

DIE THICKNESS:

0.625mm

BUMP HEIGHT:
17µm ±1µm (within die)

AU BUMP SIZE:

86 x 46µm^2 (Typ.)
66 x 49µm^2 (Typ.)

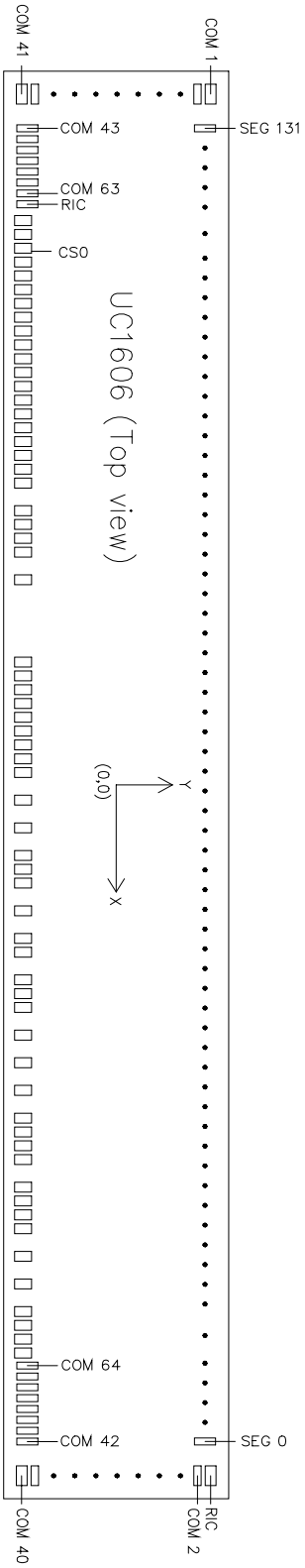
MINIMUM BUMP PITCH:
70µm (Typ.)

MINIMUM BUMP GAP:
24µm (Typ.)

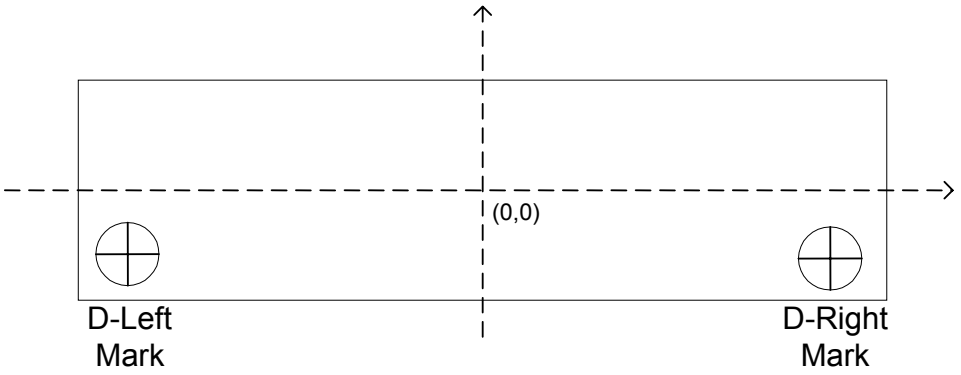
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

(Drawings and coordinates are in the circuit/bump view)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:

NOTE:

Alignment mark is on Metal3 under Passivation.

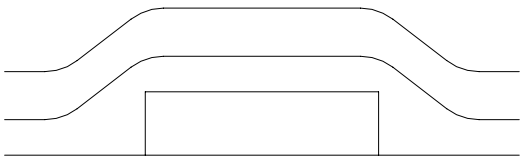
COORDINATES:

D-Left Mark Center		D-Right Mark Center	
X	Y	X	Y
-4610.0	-430.7	4610.0	-430.7

SIZE:

R: 18.0 μm; r: 9.0 μm

TOP METAL AND PASSIVATION:



FOR NON-OTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Name	X	Y	W	H
1	COM1	-4813	698	86	46
2	COM3	-4813	628	86	46
3	COM5	-4813	558	86	46
4	COM7	-4813	488	86	46
5	COM9	-4813	418	86	46
6	COM11	-4813	348	86	46
7	COM13	-4813	278	86	46
8	COM15	-4813	208	86	46
9	COM17	-4813	138	86	46
10	COM19	-4813	68	86	46
11	COM21	-4813	-2	86	46
12	COM23	-4813	-72	86	46
13	COM25	-4813	-142	86	46
14	COM27	-4813	-212	86	46
15	COM29	-4813	-282	86	46
16	COM31	-4813	-352	86	46
17	COM33	-4813	-422	86	46
18	COM35	-4813	-492	86	46
19	COM37	-4813	-562	86	46
20	COM39	-4813	-632	86	46
21	COM41	-4813	-702	86	46
22	COM43	-4612	-706	46	86
23	COM45	-4542	-706	46	86
24	COM47	-4472	-706	46	86
25	COM49	-4402	-706	46	86
26	COM51	-4332	-706	46	86
27	COM53	-4262	-706	46	86
28	COM55	-4192	-706	46	86
29	COM57	-4122	-706	46	86
30	COM59	-4052	-706	46	86
31	COM61	-3982	-706	46	86
32	COM63	-3912	-706	46	86
33	CIC	-3842	-706	46	86
34	NC	-3764	-706	46	86
35	EO	-3694	-706	46	86
36	VDDX	-3624	-706	46	86
37	CS0	-3554	-706	46	86
38	CS1	-3484	-706	46	86
39	TST4	-3414	-706	46	86
40	RST	-3344	-706	46	86
41	CD	-3274	-706	46	86
42	WR0	-3204	-706	46	86
43	WR1	-3134	-706	46	86
44	D0	-3064	-706	46	86
45	D1	-2994	-706	46	86
46	D2	-2924	-706	46	86
47	D3	-2854	-706	46	86
48	D4	-2784	-706	46	86
49	D5	-2714	-706	46	86

#	Name	X	Y	W	H
50	D6	-2644	-706	46	86
51	D7	-2574	-706	46	86
52	VDD	-2394	-723	86	46
53	VDD	-2287	-723	86	46
54	VDD	-2180	-723	86	46
55	VDD	-2074	-723	86	46
56	VDD	-1967	-723	86	46
57	VDD2	-1769	-723	86	46
58	VDD2	-1663	-723	86	46
59	VDD2	-1556	-723	86	46
60	VDD2	-1449	-723	86	46
61	VDD3	-1343	-723	86	46
62	VSS	-1054	-723	86	46
63	VSS	-947	-723	86	46
64	VSS	-841	-723	86	46
65	VSS	-734	-723	86	46
66	VSS	-627	-723	86	46
67	VSS2	-430	-723	86	46
68	VSS2	-323	-723	86	46
69	VSS2	-216	-723	86	46
70	VSS2	-110	-723	86	46
71	VB1+	125	-723	86	46
72	VB1+	231	-723	86	46
73	VB1+	338	-723	86	46
74	TP3	436	-724	66	49
75	TP2	526	-724	66	49
76	TP1	616	-724	66	49
77	PS0	764	-706	46	86
78	PS1	904	-706	46	86
79	VDDX	974	-706	46	86
80	MR0	1114	-706	46	86
81	MR1	1254	-706	46	86
82	VB1-	1394	-706	46	86
83	VB1-	1464	-706	46	86
84	VB1-	1534	-706	46	86
85	VB1-	1604	-706	46	86
86	VB0-	1744	-706	46	86
87	VB0-	1814	-706	46	86
88	VB0-	1884	-706	46	86
89	VB0-	1954	-706	46	86
90	BR0	2094	-706	46	86
91	BR1	2234	-706	46	86
92	VDDX	2304	-706	46	86
93	TC0	2444	-706	46	86
94	TC1	2584	-706	46	86
95	VB0+	2724	-706	46	86
96	VB0+	2794	-706	46	86
97	VB0+	2864	-706	46	86
98	VB0+	2934	-706	46	86

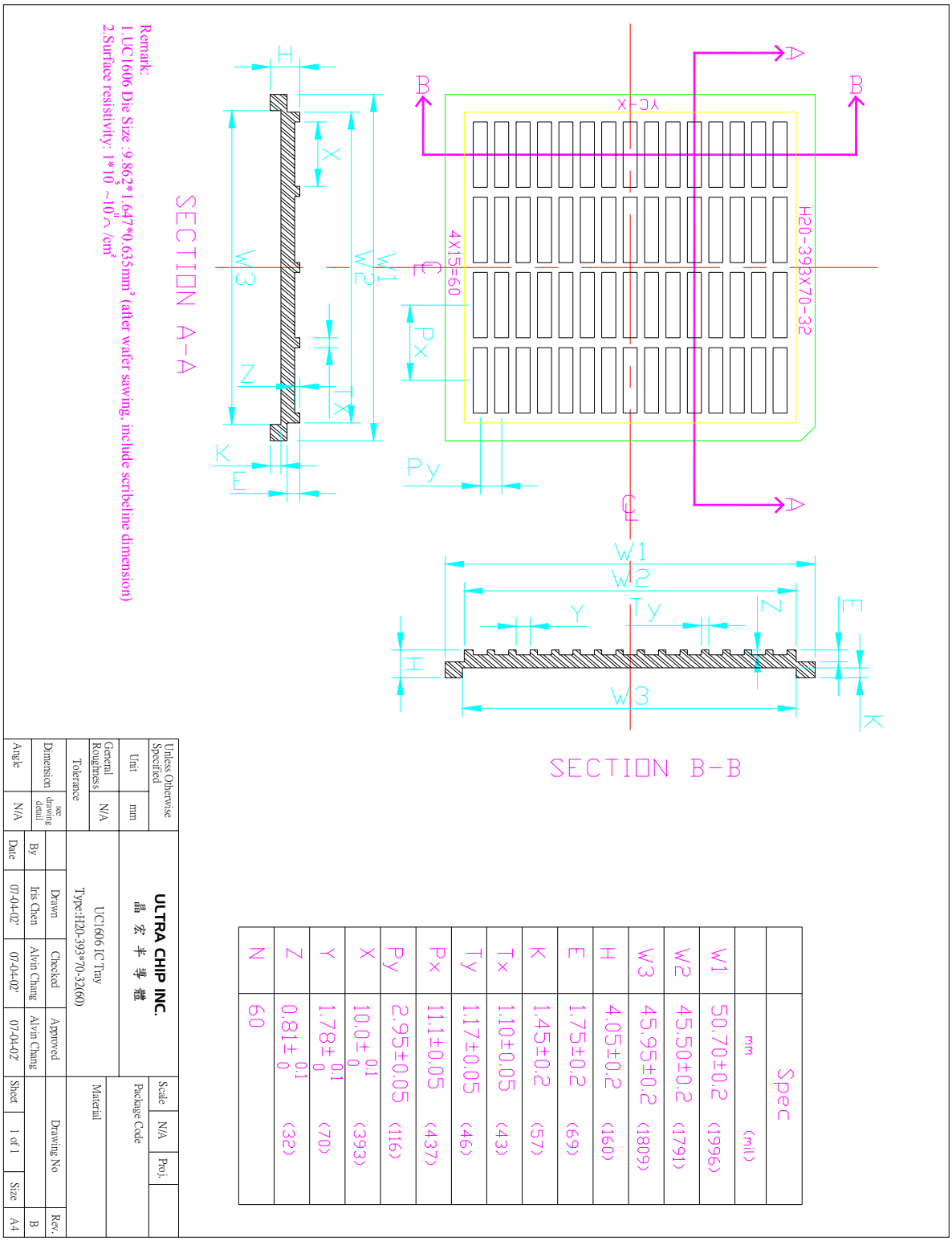
#	Name	X	Y	W	H
99	TST1	3074	-706	46	86
100	TST2	3144	-706	46	86
101	TST3	3214	-706	46	86
102	VLCDIN	3354	-706	46	86
103	VLCDOUT	3424	-706	46	86
104	VLCDIN	3494	-706	46	86
105	VLCDOUT	3634	-706	46	86
106	VDD2	3704	-706	46	86
107	VDD2	3774	-706	46	86
108	COM64	3844	-706	46	86
109	COM62	3914	-706	46	86
110	COM60	3984	-706	46	86
111	COM58	4054	-706	46	86
112	COM56	4124	-706	46	86
113	COM54	4194	-706	46	86
114	COM52	4264	-706	46	86
115	COM50	4334	-706	46	86
116	COM48	4404	-706	46	86
117	COM46	4474	-706	46	86
118	COM44	4544	-706	46	86
119	COM42	4614	-706	46	86
120	COM40	4813	-702	86	46
121	COM38	4813	-632	86	46
122	COM36	4813	-562	86	46
123	COM34	4813	-492	86	46
124	COM46	4813	-422	86	46
125	COM30	4813	-352	86	46
126	COM28	4813	-282	86	46
127	COM26	4813	-212	86	46
128	COM24	4813	-142	86	46
129	COM22	4813	-72	86	46
130	COM20	4813	-2	86	46
131	COM18	4813	68	86	46
132	COM16	4813	138	86	46
133	COM14	4813	208	86	46
134	COM12	4813	278	86	46
135	COM10	4813	348	86	46
136	COM8	4813	418	86	46
137	COM6	4813	488	86	46
138	COM4	4813	558	86	46
139	COM2	4813	628	86	46
140	CIC	4813	698	86	46
141	SEG1	4585	706	46	86
142	SEG2	4515	706	46	86
143	SEG3	4445	706	46	86
144	SEG4	4375	706	46	86
145	SEG5	4305	706	46	86
146	SEG6	4235	706	46	86
147	SEG7	4165	706	46	86
148	SEG8	4095	706	46	86
149	SEG9	4025	706	46	86

#	Name	X	Y	W	H
150	SEG10	3955	706	46	86
151	SEG11	3885	706	46	86
152	SEG12	3815	706	46	86
153	SEG13	3745	706	46	86
154	SEG14	3675	706	46	86
155	SEG15	3605	706	46	86
156	SEG16	3535	706	46	86
157	SEG17	3465	706	46	86
158	SEG18	3395	706	46	86
159	SEG19	3325	706	46	86
160	SEG20	3255	706	46	86
161	SEG21	3185	706	46	86
162	SEG22	3115	706	46	86
163	SEG23	3045	706	46	86
164	SEG24	2975	706	46	86
165	SEG25	2905	706	46	86
166	SEG26	2835	706	46	86
167	SEG27	2765	706	46	86
168	SEG28	2695	706	46	86
169	SEG29	2625	706	46	86
170	SEG30	2555	706	46	86
171	SEG31	2485	706	46	86
172	SEG32	2415	706	46	86
173	SEG33	2345	706	46	86
174	SEG34	2275	706	46	86
175	SEG35	2205	706	46	86
176	SEG36	2135	706	46	86
177	SEG37	2065	706	46	86
178	SEG38	1995	706	46	86
179	SEG39	1925	706	46	86
180	SEG40	1855	706	46	86
181	SEG41	1785	706	46	86
182	SEG42	1715	706	46	86
183	SEG43	1645	706	46	86
184	SEG44	1575	706	46	86
185	SEG45	1505	706	46	86
186	SEG46	1435	706	46	86
187	SEG47	1365	706	46	86
188	SEG48	1295	706	46	86
189	SEG49	1225	706	46	86
190	SEG50	1155	706	46	86
191	SEG51	1085	706	46	86
192	SEG52	1015	706	46	86
193	SEG53	945	706	46	86
194	SEG54	875	706	46	86
195	SEG55	805	706	46	86
196	SEG56	735	706	46	86
197	SEG57	665	706	46	86
198	SEG58	595	706	46	86
199	SEG59	525	706	46	86
200	SEG60	455	706	46	86

#	Name	X	Y	W	H
201	SEG61	385	706	46	86
202	SEG62	315	706	46	86
203	SEG63	245	706	46	86
204	SEG64	175	706	46	86
205	SEG65	105	706	46	86
206	SEG66	35	706	46	86
207	SEG67	-35	706	46	86
208	SEG68	-105	706	46	86
209	SEG69	-175	706	46	86
210	SEG70	-245	706	46	86
211	SEG71	-315	706	46	86
212	SEG72	-385	706	46	86
213	SEG73	-455	706	46	86
214	SEG74	-525	706	46	86
215	SEG75	-595	706	46	86
216	SEG76	-665	706	46	86
217	SEG77	-735	706	46	86
218	SEG78	-805	706	46	86
219	SEG79	-875	706	46	86
220	SEG80	-945	706	46	86
221	SEG81	-1015	706	46	86
222	SEG82	-1085	706	46	86
223	SEG83	-1155	706	46	86
224	SEG84	-1225	706	46	86
225	SEG85	-1295	706	46	86
226	SEG86	-1365	706	46	86
227	SEG87	-1435	706	46	86
228	SEG88	-1505	706	46	86
229	SEG89	-1575	706	46	86
230	SEG90	-1645	706	46	86
231	SEG91	-1715	706	46	86
232	SEG92	-1785	706	46	86
233	SEG93	-1855	706	46	86
234	SEG94	-1925	706	46	86
235	SEG95	-1995	706	46	86
236	SEG96	-2065	706	46	86
237	SEG97	-2135	706	46	86
238	SEG98	-2205	706	46	86
239	SEG99	-2275	706	46	86
240	SEG100	-2345	706	46	86
241	SEG101	-2415	706	46	86
242	SEG102	-2485	706	46	86
243	SEG103	-2555	706	46	86
244	SEG104	-2625	706	46	86
245	SEG105	-2695	706	46	86
246	SEG106	-2765	706	46	86
247	SEG107	-2835	706	46	86
248	SEG108	-2905	706	46	86
249	SEG109	-2975	706	46	86
250	SEG110	-3045	706	46	86
251	SEG111	-3115	706	46	86

#	Name	X	Y	W	H
252	SEG112	-3185	706	46	86
253	SEG113	-3255	706	46	86
254	SEG114	-3325	706	46	86
255	SEG115	-3395	706	46	86
256	SEG116	-3465	706	46	86
257	SEG117	-3535	706	46	86
258	SEG118	-3605	706	46	86
259	SEG119	-3675	706	46	86
260	SEG120	-3745	706	46	86
261	SEG121	-3815	706	46	86
262	SEG122	-3885	706	46	86
263	SEG123	-3955	706	46	86
264	SEG124	-4025	706	46	86
265	SEG125	-4095	706	46	86
266	SEG126	-4165	706	46	86
267	SEG127	-4235	706	46	86
268	SEG128	-4305	706	46	86
269	SEG129	-4375	706	46	86
270	SEG130	-4445	706	46	86
271	SEG131	-4515	706	46	86
272	SEG132	-4585	706	46	86

TRAY INFORMATION



	Spec
	mm (mil)
W1	50.70±0.2 (1996)
W2	45.50±0.2 (1791)
W3	45.95±0.2 (1809)
H	4.05±0.2 (160)
E	1.75±0.2 (69)
K	1.45±0.2 (57)
Tx	1.10±0.05 (43)
Ty	1.17±0.05 (46)
Px	11.1±0.05 (437)
Py	2.95±0.05 (116)
X	$10.0^{+0.1}_{0}$ (393)
Y	$1.78^{+0.1}_{0}$ (70)
Z	$0.81^{+0.1}_{0}$ (32)
N	60

REVISION HISTORY

Version	Contents	Date of Rev.
1.0	First release	Jul. 06, 2001
1.1	Frame rate increased, AC/DC Characteristics update, Product naming rule added	Oct. 30, 2001
1.2	Operation Voltage up to 5.0V	Dec. 18, 2001
1.3	Over All revision	Aug. 16, 2002
	(1) Recommended C_L value is adjusted to 5nF ~ 20nF (Page 5)	
	(2) VDD1 is renamed to VDD (Page 5)	
	(3) TP3 is renamed to TST4 (Page 7)	
	(4) TP[2:0] is renamed to TP[3:1] (Page 7)	
	(5) C[0:131] is renamed to SEG[1:132] (Page 7)	
	(6) R[1~64] is renamed to COM[1~64] (Page 7)	
	(7) RIC is renamed to CIC (Page 7)	
	(8) Application circuits are added. (Page 18, 23, 24)	
	(9) Alignment Mark Information is presented (Page 39)	
	(10) Tray Information is presented. (Page 43)	
	(11) Power Consumption table is presented (Page 33)	
1.31	(1) The direction on dealing with unused bus pins is corrected as leaving open-circuit; instead of connecting to V_{DD}/V_{SS}. (Section “Pin Description”, page 6; “Host Interface”, page 21.)	Jun. 18, 2003
	(2) Figures 8 and 9, reference circuit for S8/S9, are corrected to present SDA=D2, instead of D3. (Section “Host interface reference circuit”, Page 24)	
	(3) “Power Consumption” table is filled with data. (Section “Specifications”, Page 33)	
	(4) Figures 12, 13 and 14 are patched by adding pulse CS1. (Section ”AC Characteristics”, Pp 33-35)	

Version	Contents	Date of Rev.
1.32	(1) Section “Table of Revision History” is renamed as “Revision History” and moved to the rear of the datasheet.	Sep. 24, 2003
	(2) Recommended CB value has been modified: ~ 100x → 150 ~ 250x (Section “Pin Description”, page 4)	
	(3) In the “Bits” column, number of bit is updated from “PIN” to “2” (Section “Control Registers” – “MR” entry, page 7)	
	(4) In the “Default” column, the default values are updated: “00H” → “0H” (Section “Control Registers” – entries “DC”, “AC”, and “LC”, page 8)	
	(5) In the “Default value” column, the default value is updated: “0011b” → “011b” (Section “Command Table” – (5) Set Gain, page 9)	
	(6) Description of PC[2:1] is modified: 00b: 4x → 01b: 4x (Section “Control Register”, page 9; “Command Description”, page 11)	
	(7) The description for MX is updated: MX: Status of register LC[1] → LC[2] (Section “Command Description” – (3) Get Status, page 10)	
	(8) In the Action column, pin specifying is updated: Set APC[1:0] → APC[0] (Section “Command Description” – (7) Set Advance Product Configuration, page 11)	
	(9) The value of pins D[7:4] is corrected: 0110 → 1011 (Section “Command Description” – (9) Set Page Address, page 11)	
	(10) The values of WR0/WR1 of SPI(S8)/SPI(S9) are updated: “-“ → “0” (Section “Host Interface” - Table 4, page 20)	
	(11) Figure 6/7: 8080/8bit and 6800/8bit parallel mode reference circuit is modified by showing RST pin. Figure 8/9: Serial-8/9 serial mode reference circuit is modified as following: SDA(D3) → SDA(D2) (Section “Host interface reference circuit”, Pp 22 - 23)	
	(12) Power consumption table is added. (Section “Specifications”, page 32)	
	(13) Die Size is updated. (Section “Physical Dimensions”, page 37)	
	(14) Alignment Mark Information is updated. (Section “Alignment Mark Dimension”, page 38)	